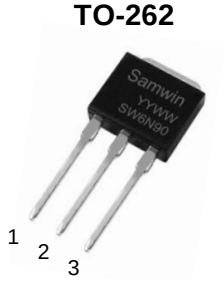
N-channel TO-262 MOSFET

Features

- High ruggedness
- $R_{DS(ON)}$ (Max 2.3 **Ω**)@V_{GS}=10V
- Gate Charge (Typical 40nC)
- Improved dv/dt Capability
- 100% Avalanche Tested

TO-262

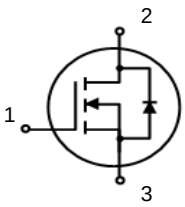


1. Gate 2. Drain 3. Source

BV_{DSS} : 900V

I_D : 6.0A

$R_{DS(ON)}$: 2.3ohm



General Description

This power MOSFET is produced with advanced VDMOS technology of SAMWIN. This technology enable power MOSFET to have better characteristics, such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. It is mainly suitable for half bridge or full bridge resonant topology like a electronic ballast, and also low power switching mode power appliances.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW U 6N90	SW6N90	TO-262	TUBE

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		900	V
I_D	Continuous Drain Current (@T_C=25°C)		6.0*	A
	Continuous Drain Current (@T_C=100°C)		3.78*	A
I_{DM}	Drain current pulsed	(note 1)	24	A
V_{GS}	Gate to Source Voltage		±30	V
E_{AS}	Single pulsed Avalanche Energy	(note 2)	550	mJ
E_{AR}	Repetitive Avalanche Energy	(note 1)	150	mJ
dv/dt	Peak diode Recovery dv/dt	(note 3)	5	V/ns
P_D	Total power dissipation (@T_C=25°C)		231	W
	Derating Factor above 25°C		1.85	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature		-55 ~ + 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	°C

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	0.54	°C/W
R_{thcs}	Thermal resistance, Case to Sink	-	°C/W
R_{thja}	Thermal resistance, Junction to ambient	65	°C/W

Electrical characteristic (T_C = 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	900			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25ºC		0.91		V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=900V, V_{GS}=0V			1	uA
		V_{DS}=720V, T_C=125ºC			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	3.0		5.0	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 3A		1.8	2.3	Ω
Gfs	Forward Transconductance	V_{DS} = 40 V, I_D = 3 A	6			S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		1400		pF
C_{oss}	Output capacitance			120		
C_{rss}	Reverse transfer capacitance			35		
$t_{d(on)}$	Turn on delay time	V_{DS}=450V, I_D=6A, R_G=25Ω (note 4, 5)		23	50	ns
tr	Rising time			26	60	
$t_{d(off)}$	Turn off delay time			58	120	
t_f	Fall time			24	50	
Q_g	Total gate charge	V_{DS}=720V, V_{GS}=10V, I_D=6A (note 4, 5)		40	90	nC
Q_{gs}	Gate-source charge			8		
Q_{gd}	Gate-drain charge			19		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			6.0	A
I_{SM}	Pulsed source current				24.0	A
V_{SD}	Diode forward voltage drop.	I_S=6.0A, V_{GS}=0V			1.5	V
T_{rr}	Reverse recovery time	I_S=6.0A, V_{GS}=0V, dI_F/dt=100A/us		436		ns
Q_{rr}	Reverse recovery Charge			5.2		uC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 30mH, I_{AS} = 6.0A, V_{DD} = 50V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 6.0A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

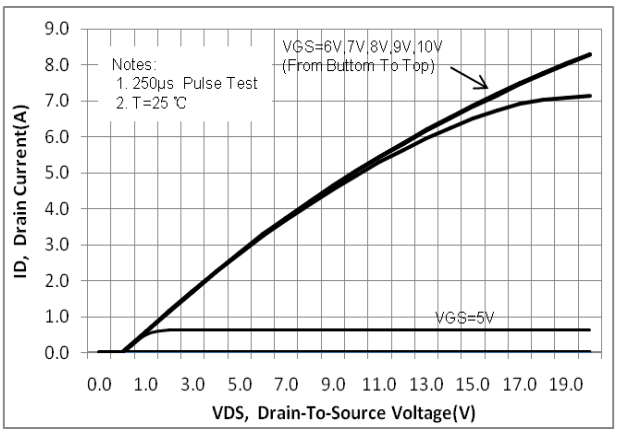


Fig. 2. On-resistance variation vs. drain current and gate voltage

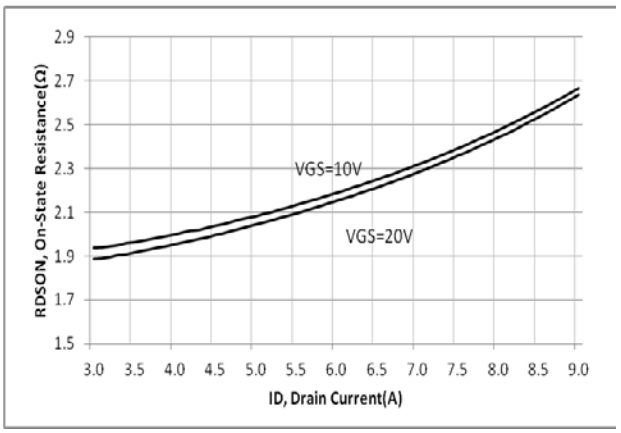


Fig. 3. Gate charge characteristics

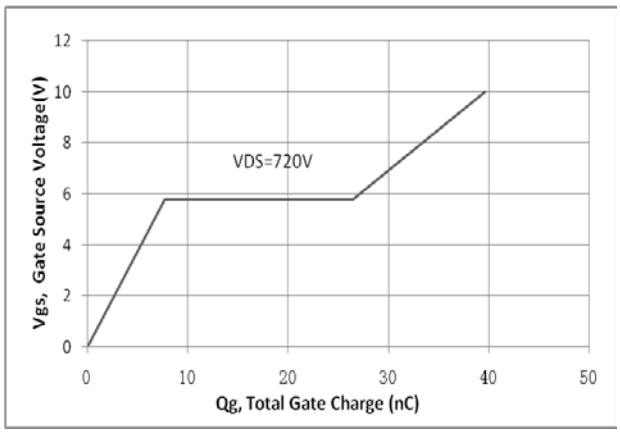


Fig. 4. On state current vs. diode forward voltage

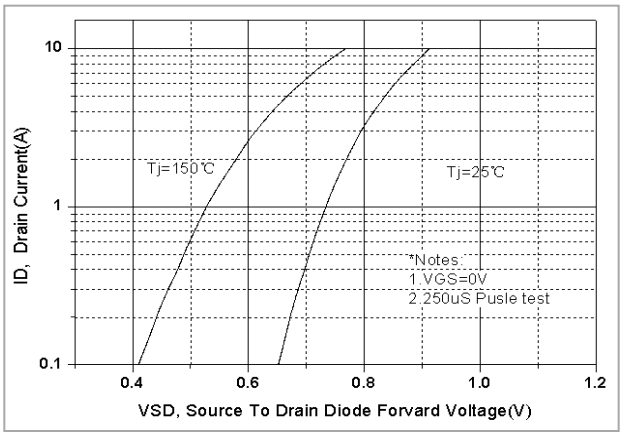


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

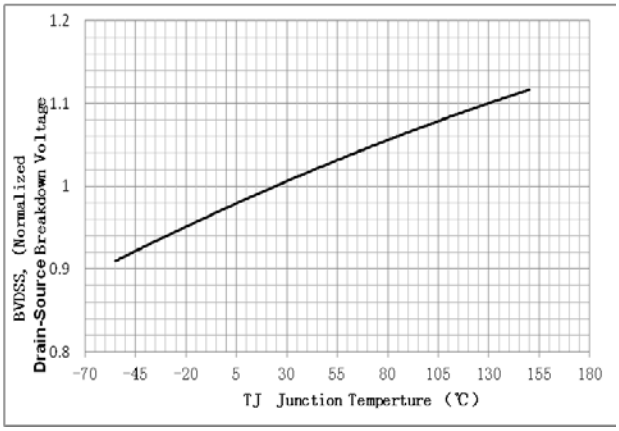


Fig. 6. On resistance variation vs. junction temperature

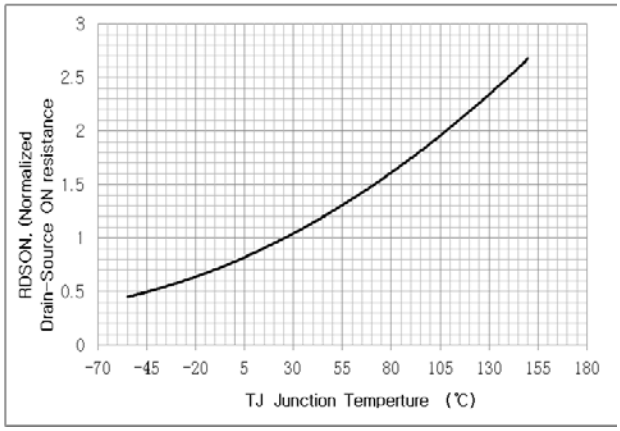


Fig. 7. Maximum safe operating area

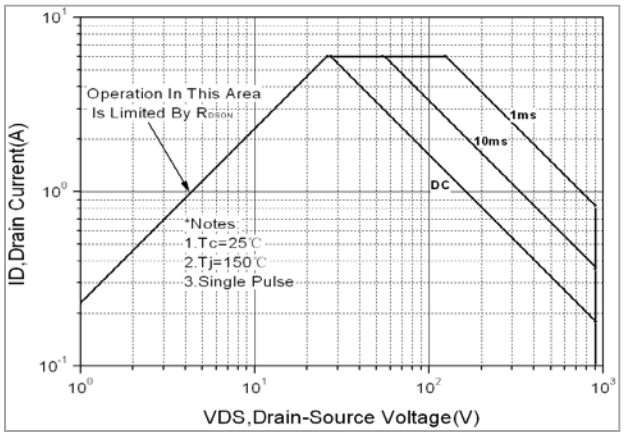


Fig. 8. Transient thermal response curve

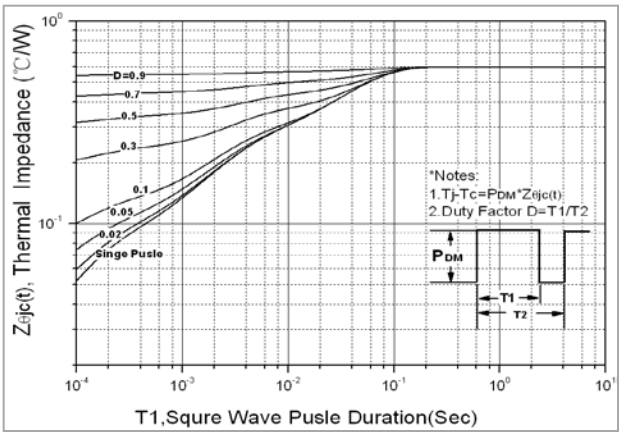


Fig. 9. Gate charge test circuit & waveform

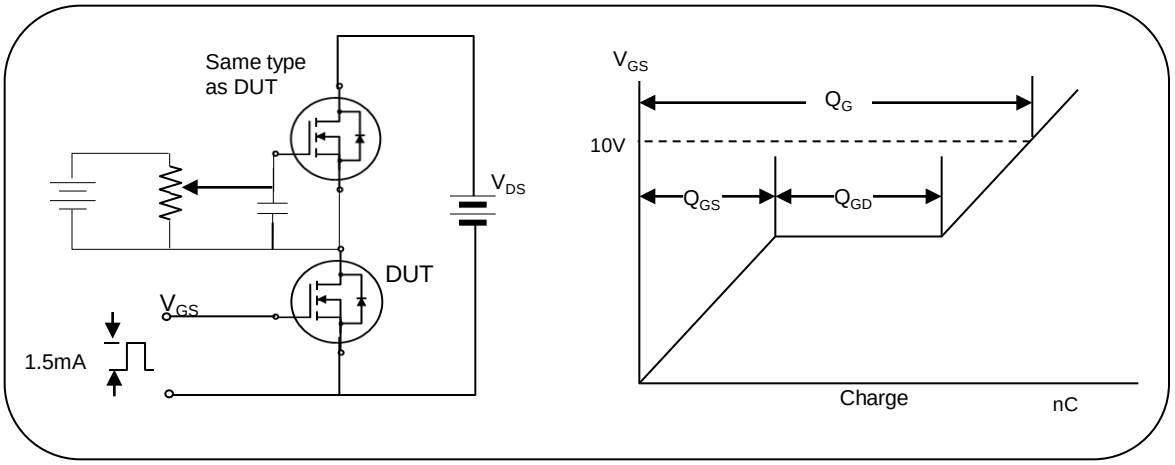


Fig. 10. Switching time test circuit & waveform

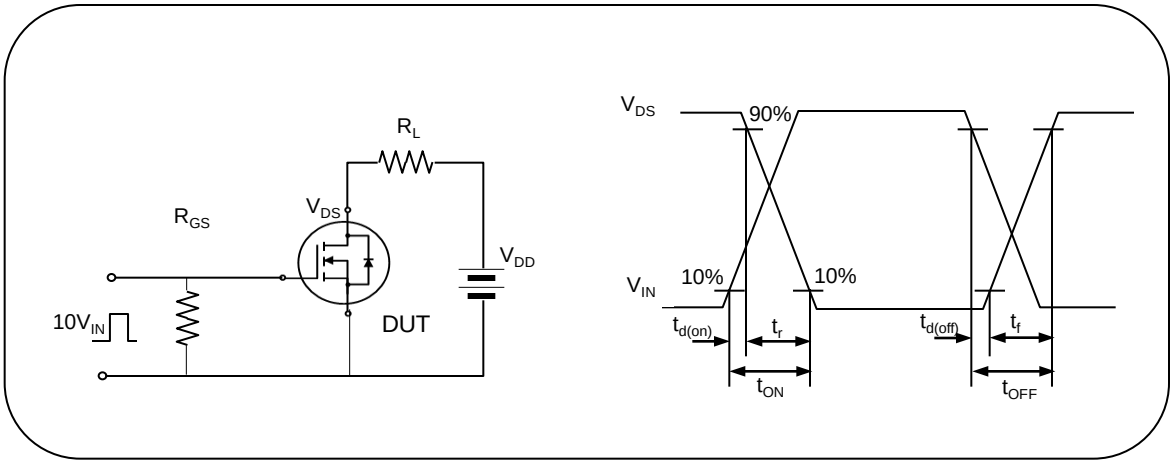


Fig. 11. Unclamped Inductive switching test circuit & waveform

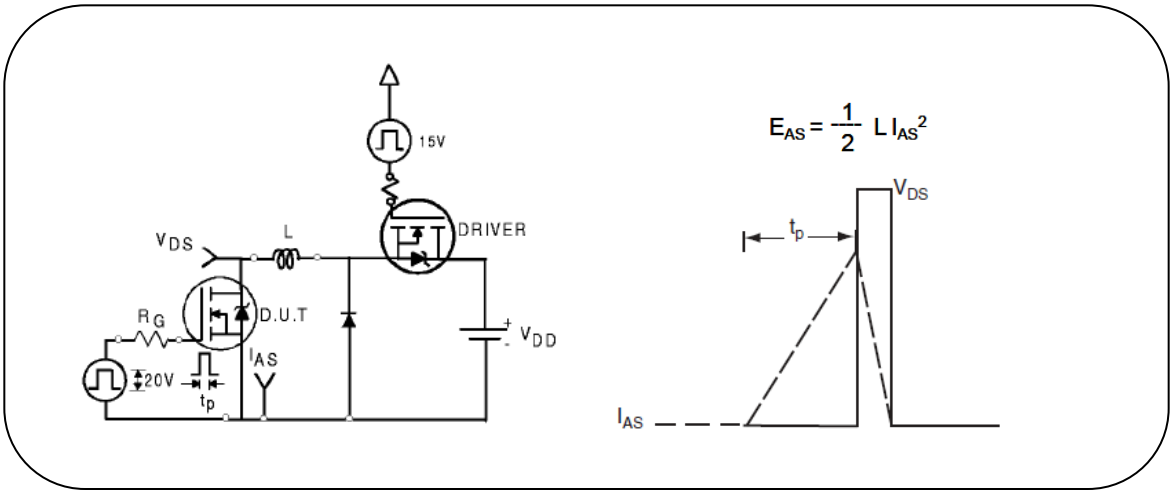


Fig. 12. Peak diode recovery dv/dt test circuit & waveform