

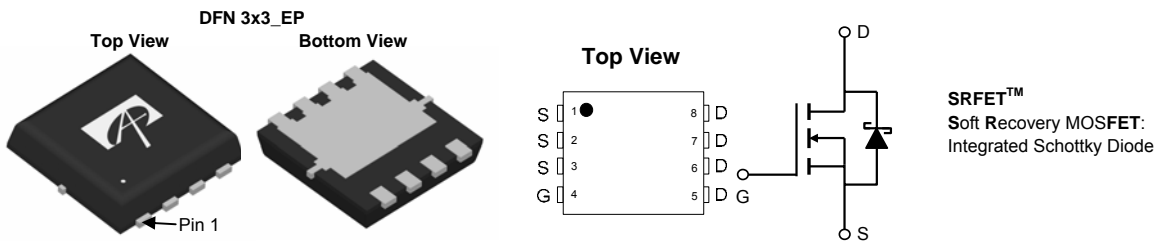
### General Description

SRFET™ AON7788 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent  $R_{DS(ON)}$  and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

### Product Summary

$V_{DS}$	30V
$I_D$ (at $V_{GS}=10V$ )	40A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 4.5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	< 5.3m $\Omega$

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	40
		$T_C=100^\circ\text{C}$	31
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	150	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	20
		$T_A=70^\circ\text{C}$	16
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	35	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	61	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	36
		$T_C=100^\circ\text{C}$	14
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	30	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A D</sup>		60	75	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	2.8	3.4	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =125°C			0.5 100	mA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±12V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.2	1.6	2	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	150			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		3.7 5.5	4.5 6.6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		4.2	5.3	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		115		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.4	0.7	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				40	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz	2730	3415	4100	pF
C <sub>oss</sub>	Output Capacitance		240	340	440	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		140	232	325	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.6	1.2	1.8	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(4.5V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A	19	24	29	nC
Q <sub>gs</sub>	Gate Source Charge		6.6			nC
Q <sub>gd</sub>	Gate Drain Charge		10			nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		9		ns
t <sub>r</sub>	Turn-On Rise Time		4.5			ns
t <sub>D(off)</sub>	Turn-Off Delay Time		47			ns
t <sub>f</sub>	Turn-Off Fall Time		5.5			ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	8	10	12	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	12	15	18	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

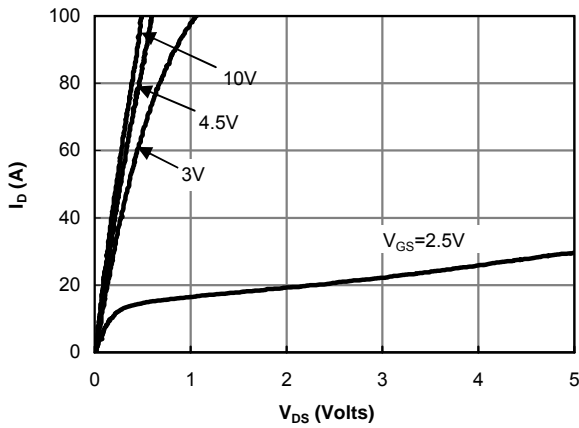
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

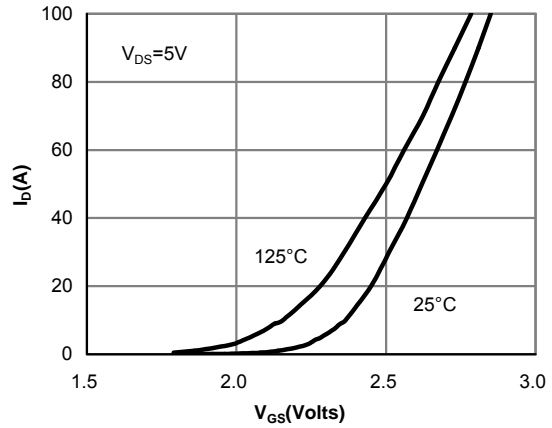
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

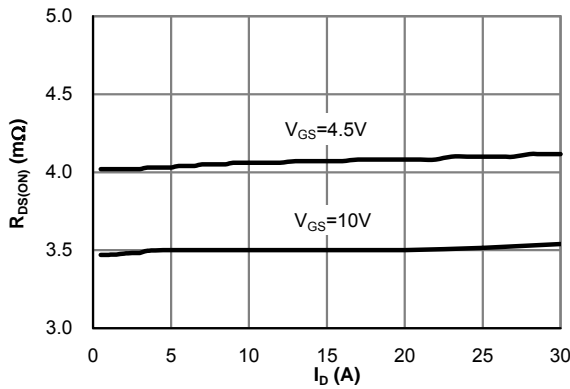
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



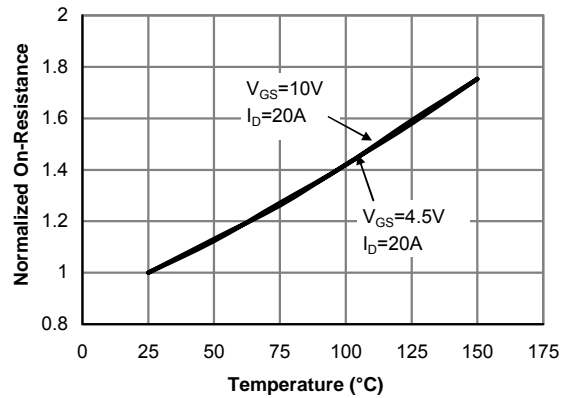
**Figure 1: On-Region Characteristics (Note E)**



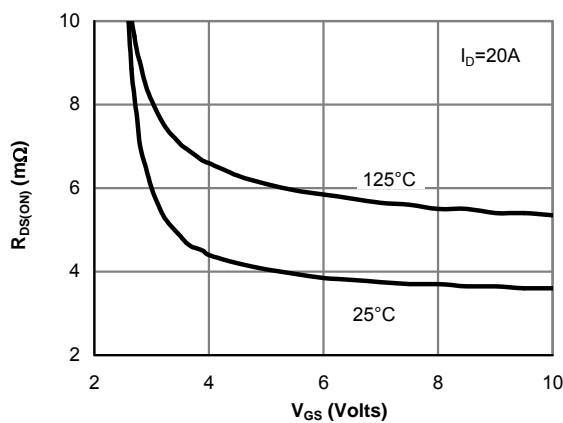
**Figure 2: Transfer Characteristics (Note E)**



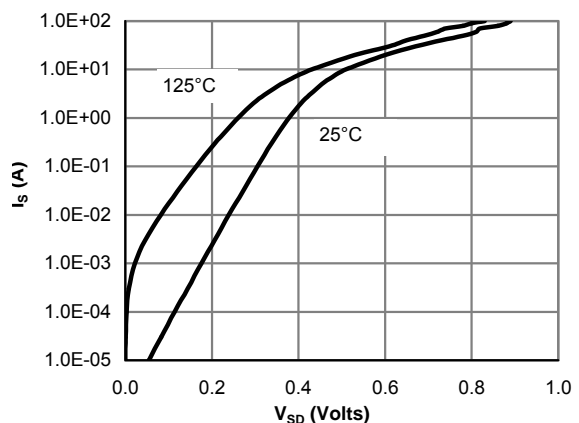
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

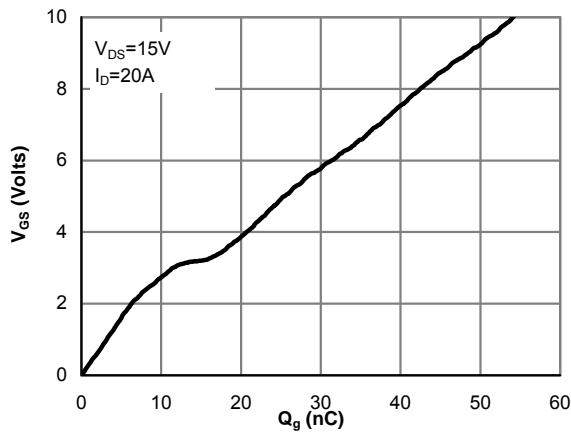


Figure 7: Gate-Charge Characteristics

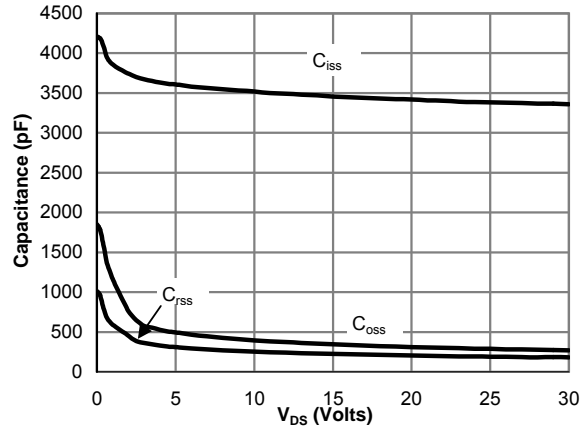


Figure 8: Capacitance Characteristics

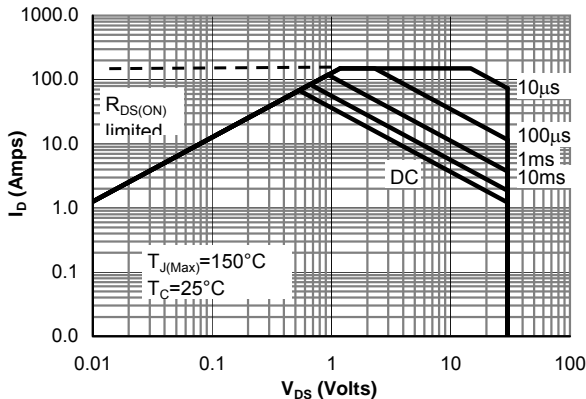


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

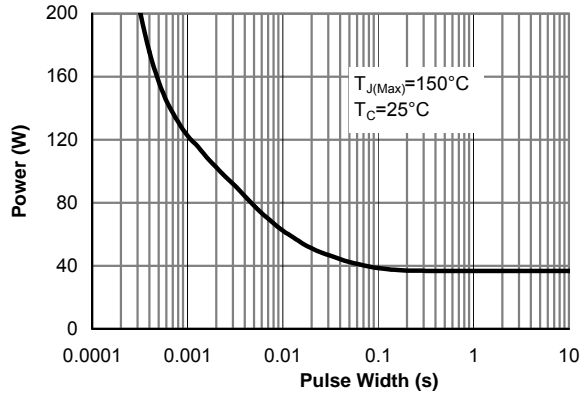


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

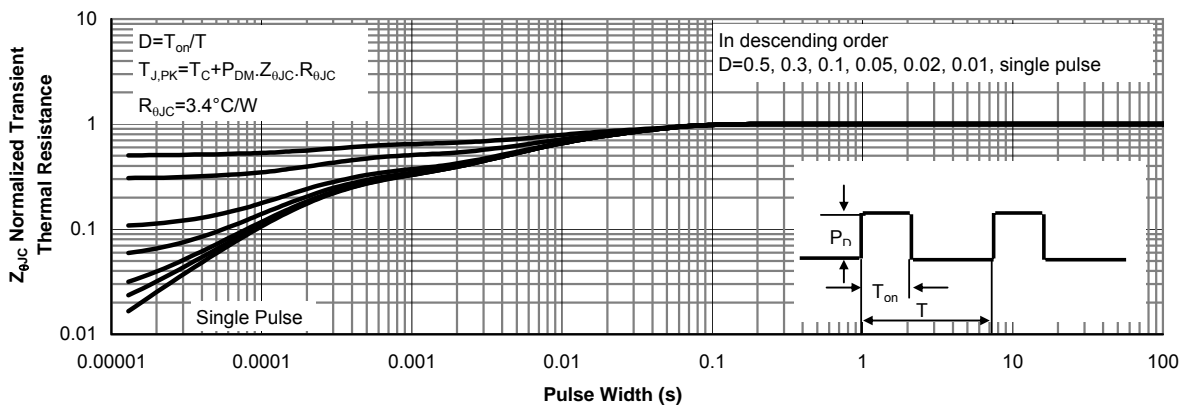
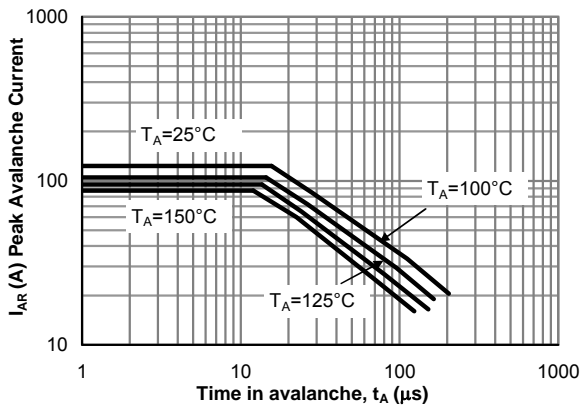
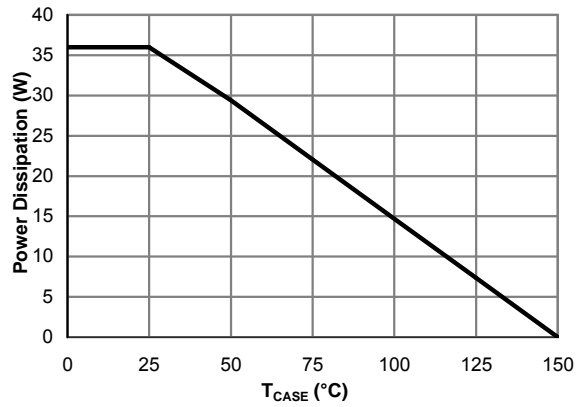


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

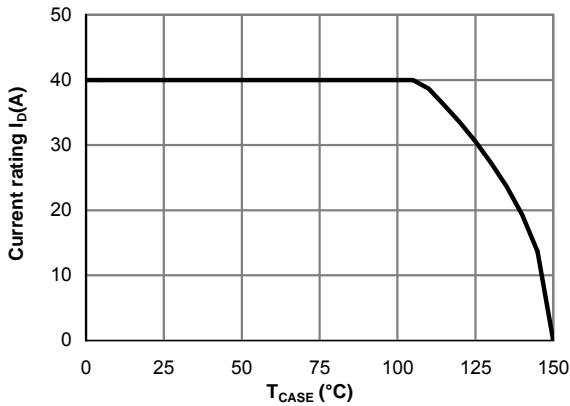
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



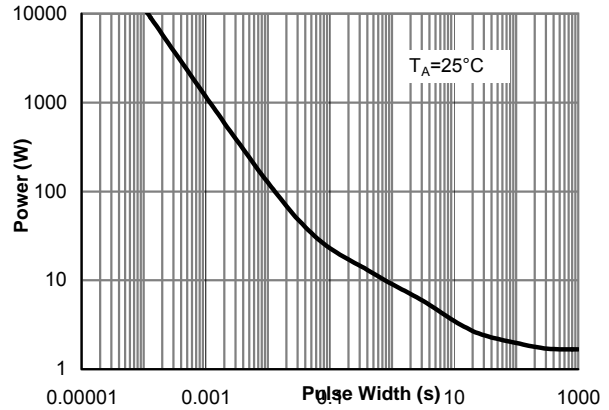
**Figure 12: Single Pulse Avalanche capability (Note C)**



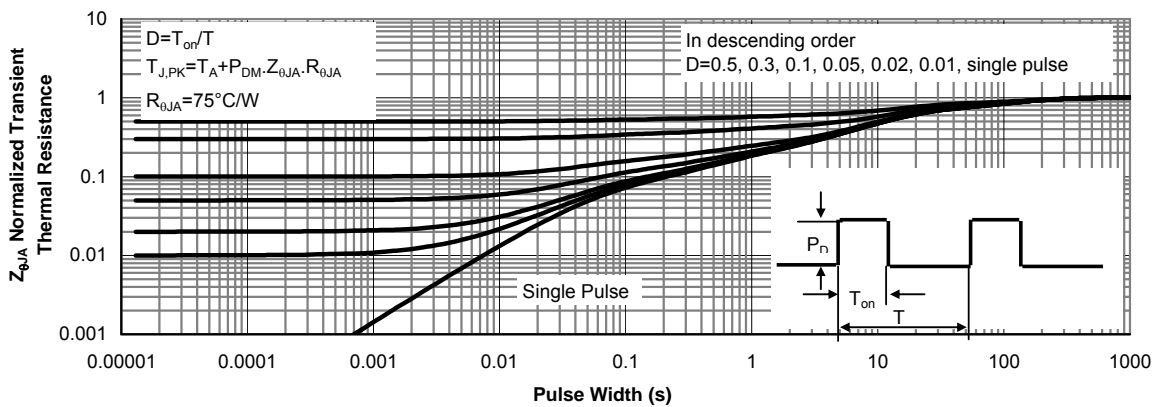
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

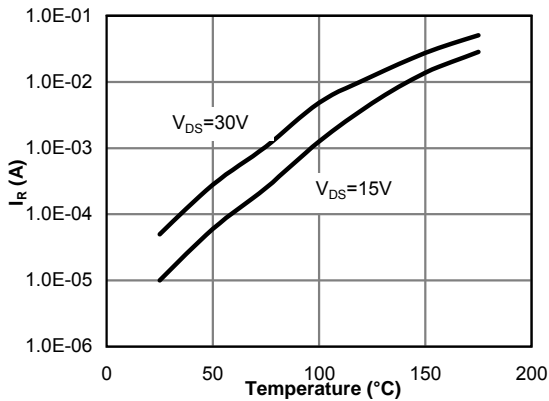


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

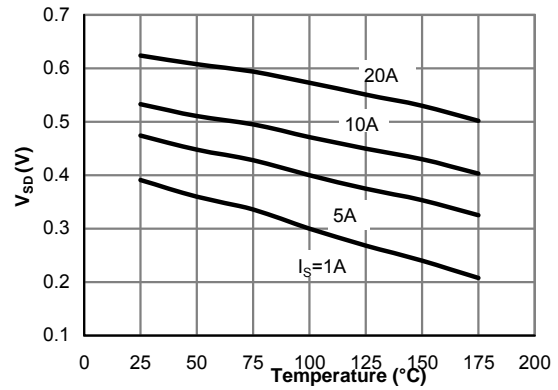


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

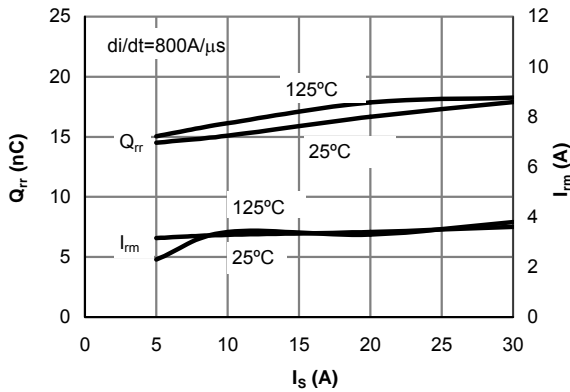
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



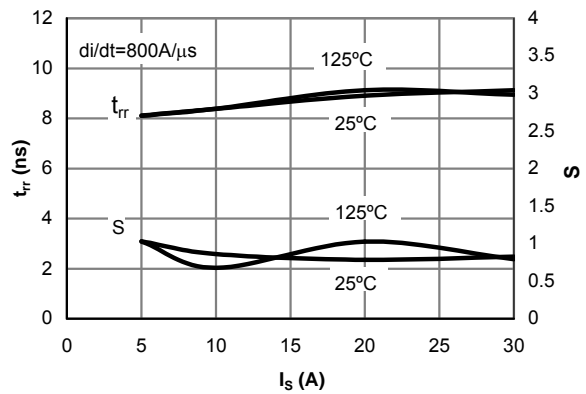
**Figure 17: Diode Reverse Leakage Current vs. Junction Temperature**



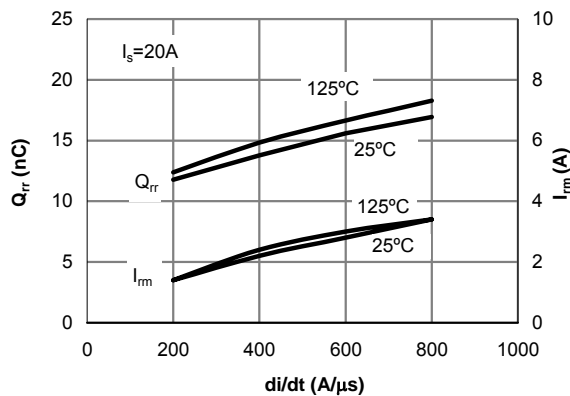
**Figure 18: Diode Forward Voltage vs. Junction Temperature**



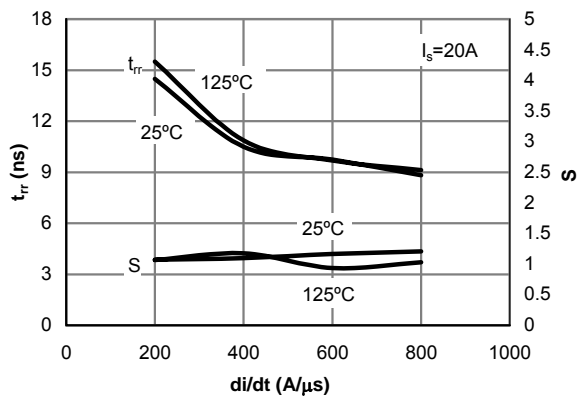
**Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**



**Figure 20: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

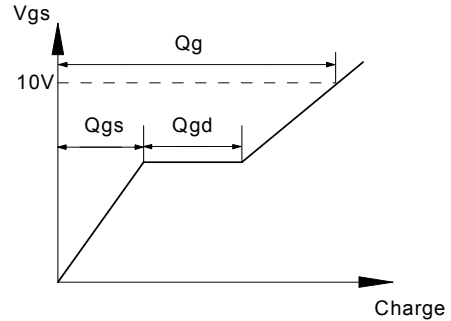
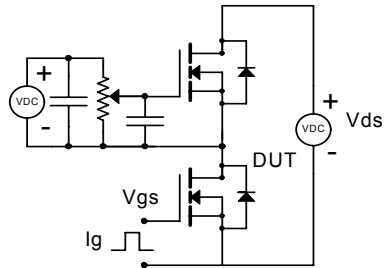


**Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

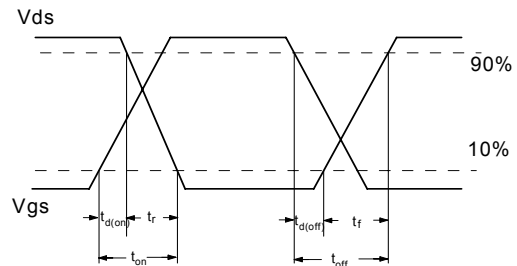
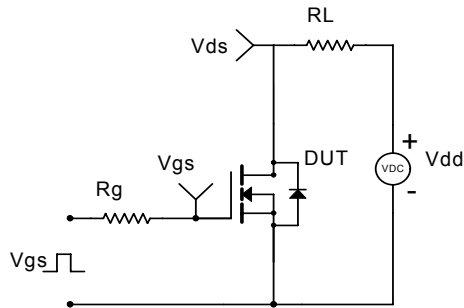


**Figure 22: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

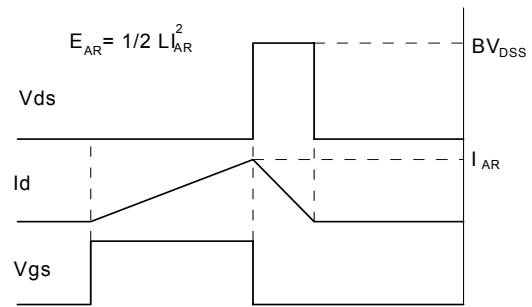
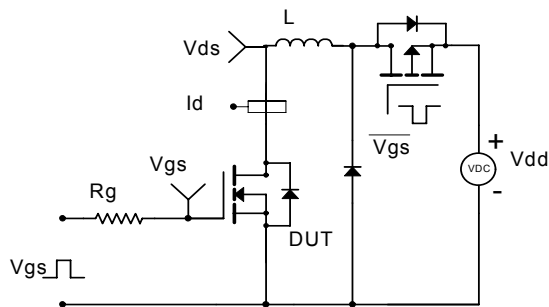
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

