Designer's Data Sheet
Power Field Effect Transistor
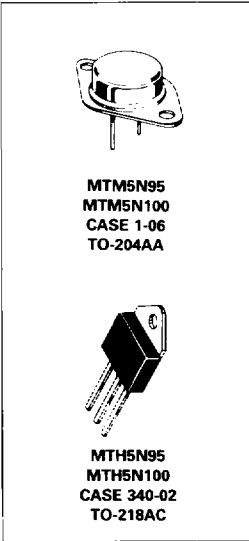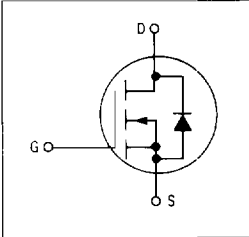**N-Channel Enhancement-Mode**
Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS

| MTH5N95 |
| MTH5N100 |
| MTM5N95 |
| MTM5N100 |

TMOS POWER FETs
5 AMPERES
$r_{DS(on)} = 3$ OHMS
950 and 1000 VOLTS

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM		Unit
		5N95	5N100	
Drain-Source Voltage	V_{DSS}	950	1000	Vdc
Drain-Gate Voltage ($R_{GS} = 1$ MΩ)	V_{DGR}	950	1000	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leqslant 50$ μs)	V_{GSM}	±40		Vpk
Drain Current Continuous	I_D	5		Adc
Pulsed	I_{DM}	17		
Total Power Dissipation @ $T_C = 25°C$	P_D	150		Watts
Derate above 25°C		1.2		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.83	°C/W
— Junction to Ambient	$R_{\theta JA}$	30	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

MTM5N95
MTM5N100
CASE 1-06
TO-204AA

MTH5N95
MTH5N100
CASE 340-02
TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MOTOROLA TMOS POWER MOSFET DATA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$		—	Vdc
(V_{GS} = 0, I_D = 0.25 mA) MTH/MTM5N95		950	—	
MTH/MTM5N100		1000	—	
Zero Gate Voltage Drain Current	I_{DSS}			mAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	0.2	
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$r_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 5 Adc)		—	15	
(I_D = 2.5 Adc, T_J = 100°C)		—	12.5	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	g_{FS}	2	—	mhos

DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0,	C_{iss}	—	2600	pF
Output Capacitance	f = 1 MHz)	C_{oss}	—	350	
Reverse Transfer Capacitance	See Figure 10	C_{rss}	—	200	

SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time		$t_{d(on)}$	—	70	ns
Rise Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D	t_r	—	250	
Turn-Off Delay Time	R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(off)}$	—	500	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS},	Q_g	110 (Typ)	140	nC
Gate-Source Charge	I_D = Rated I_D, V_{GS} = 10 V)	Q_{gs}	60 (Typ)	—	
Gate-Drain Charge	See Figure 11	Q_{gd}	50 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time	V_{GS} = 0)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-218)				
Internal Drain Inductance	L_d		—	nH
(Measured from the contact screw on tab to center of die)		4 (Typ)	—	
(Measured from the drain lead 0.25" from package to center of die)		5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

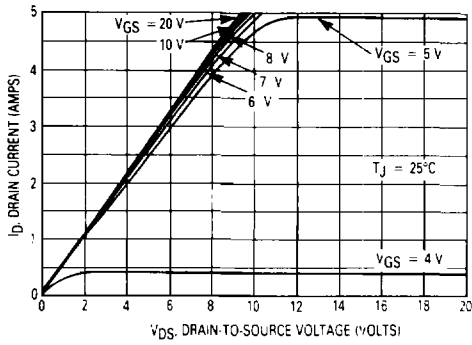## TYPICAL ELECTRICAL CHARACTERISTICS

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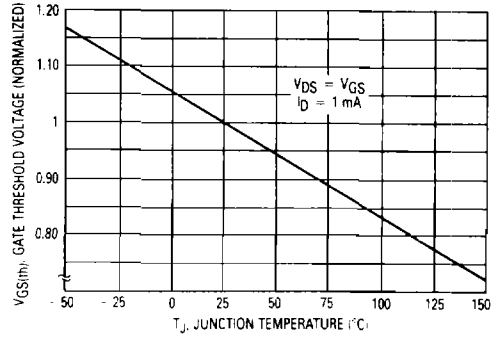**Figure 1. On-Region Characteristics**

Figure 2. Gate-Threshold Voltage Variation With Temperature
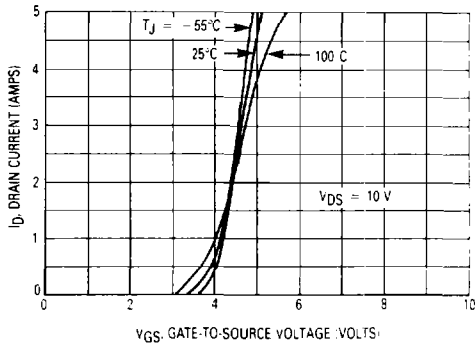

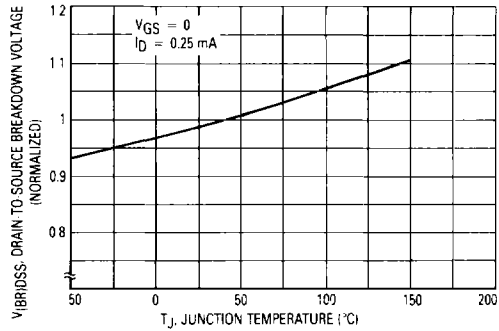**Figure 3. Transfer Characteristics**

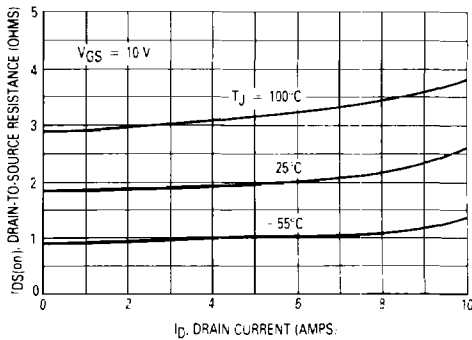**Figure 4. Breakdown Voltage Variation With Temperature**
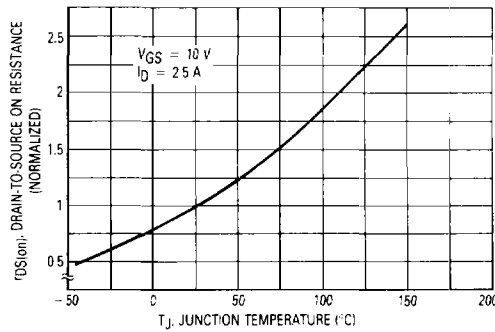

Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature
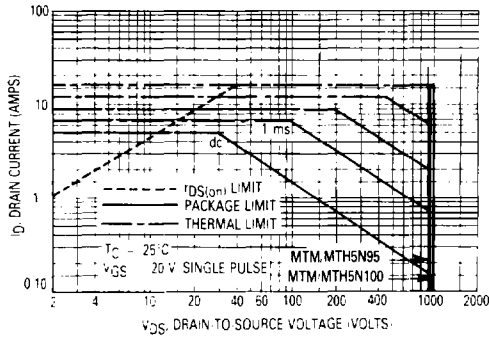
SAFE OPERATING AREA INFORMATION

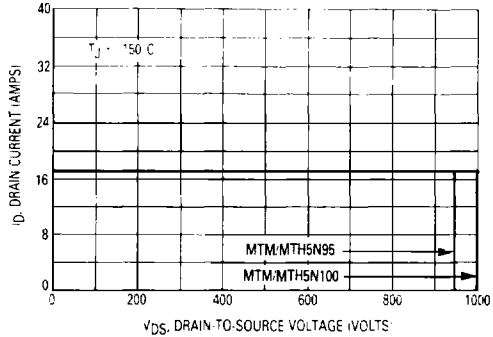**Figure 7. Maximum Rated Forward Biased
Safe Operating Area**

**Figure 8. Maximum Rated Switching
Safe Operating Area**

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

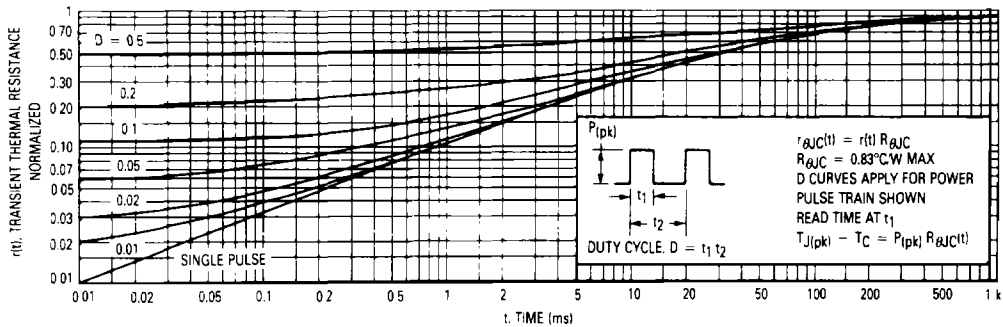$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$
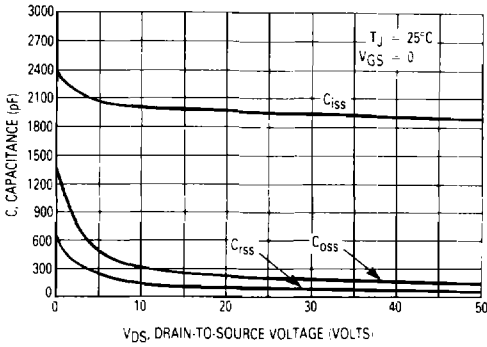

Figure 9. Thermal Response
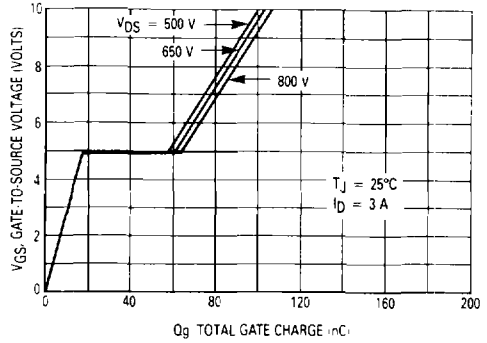
Figure 10. Capacitance Variation

Figure 11. Gate Charge versus Gate-To-Source Voltage
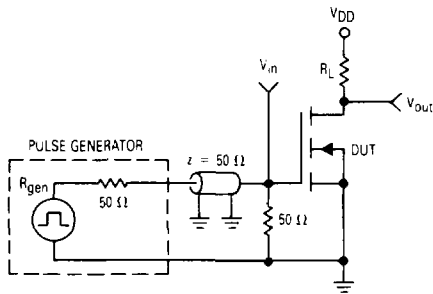
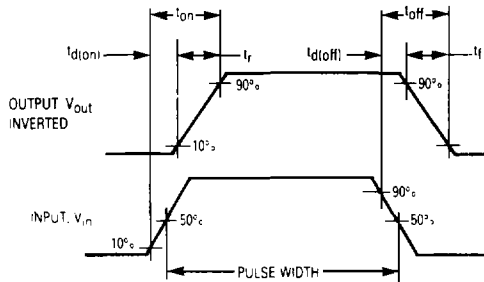## RESISTIVE SWITCHING

Figure 12. Switching Test Circuit

Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.32 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3
PIN 1 GATE
2 SOURCE
CASE DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
2. CONTROLLING DIMENSION INCH
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO 204AA OUTLINE SHALL APPLY

CASE 340-02
TO-218AC

STYLE 2
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION (INCH.)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

3