



# STL8N10LF3

N-channel 100 V, 25 mΩ typ., 7.8 A STripFET™ III  
Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet — production data

## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL8N10LF3	100 V	35 mΩ	7.8 A <sup>(1)</sup>

1. The value is rated according to R<sub>thj-pcb</sub>

- Logic level V<sub>GS(th)</sub>
- 175 °C maximum junction temperature
- 100% avalanche rated

## Applications

- Switching applications
- Automotive

## Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

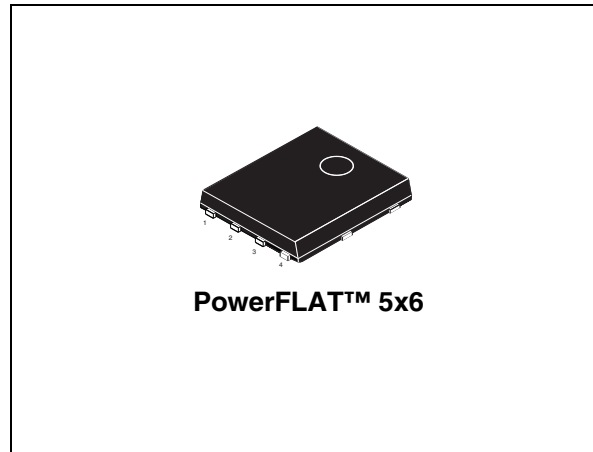


Figure 1. Internal schematic diagram

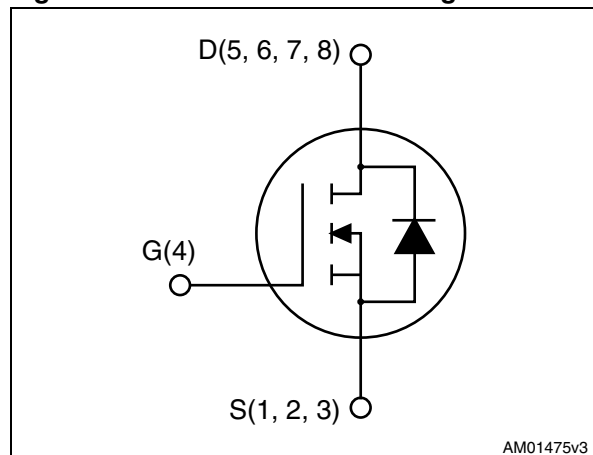


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8N10LF3	8N10LF3	PowerFLAT™ 5x6	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1),(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	20	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	7.8	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$	5.5	A
$I_{DM}^{(3),(4)}$	Drain current (pulsed)	31.2	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	70	W
$P_{TOT}^{(4)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4.3	W
$I_{AV}$	Not-repetitive avalanche current	7.8	A
$E_{AS}^{(5)}$	Single pulse avalanche energy	190	mJ
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an  $R_{thJC} = 2.1^\circ\text{C/W}$  the chip is able to carry 32 A at  $25^\circ\text{C}$ .
3. Pulse width limited by safe operating area.
4. When mounted on FR-4 board of  $1\text{inch}^2$ , 2oz Cu,  $t < 10\text{ sec}$
5. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 7.8\text{ A}$ ,  $V_{DD} = 25\text{ V}$ .

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.1	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

1. When mounted on FR-4 board of  $1\text{inch}^2$ , 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage (V <sub>GS</sub> = 0)	I <sub>D</sub> = 250 μA	100			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 100 V			1	μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		3	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A V <sub>GS</sub> = 5 V, I <sub>D</sub> = 4 A		25 40	35 50	mΩ mΩ

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	-	970	-	pF
C <sub>oss</sub>	Output capacitance			115		
C <sub>rss</sub>	Reverse transfer capacitance			11.5		
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7.8 A	-	20.5	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 10 V		4		
Q <sub>gd</sub>	Gate-drain charge	<a href="#">Figure 13</a>		5		
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz open drain		3.65		Ω

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7.8 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V <a href="#">Figure 12</a>	-	8.7	-	ns
t <sub>r</sub>	Rise time			9.6		
t <sub>d(off)</sub>	Turn-off delay time			50.6		
t <sub>f</sub>	Fall time			5.2		

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		7.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		31.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7.8 \text{ A}, V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7.8 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 48 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	42.5		ns
$Q_{rr}$	Reverse recovery charge			87		nC
$I_{RRM}$	Reverse recovery current			4.08		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

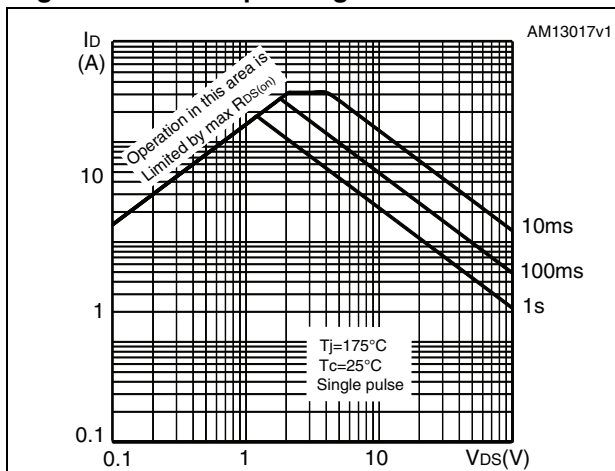


Figure 3. Thermal impedance

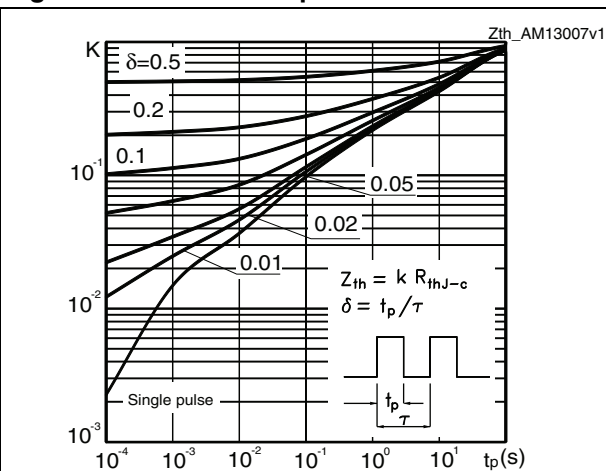


Figure 4. Output characteristics

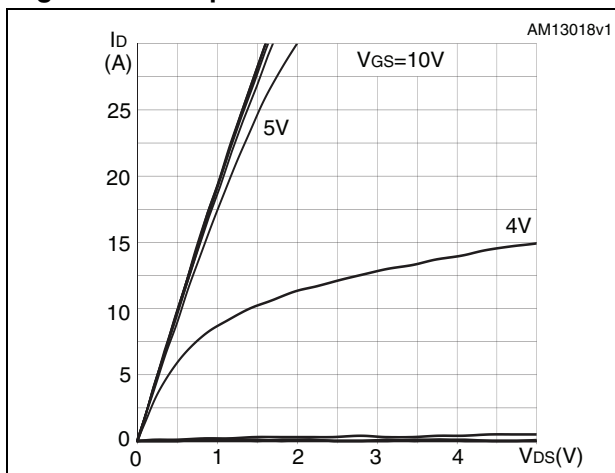


Figure 5. Transfer characteristics

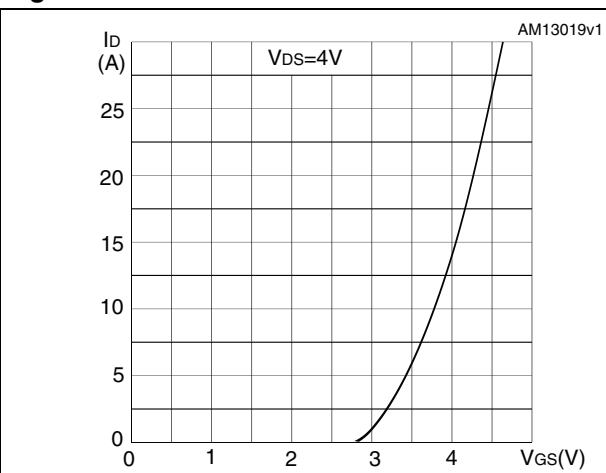


Figure 6. Normalized  $V_{DS}$  vs temperature

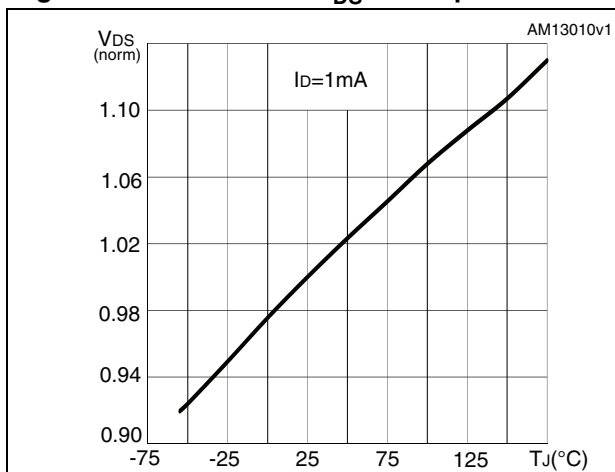


Figure 7. Static drain-source on-resistance

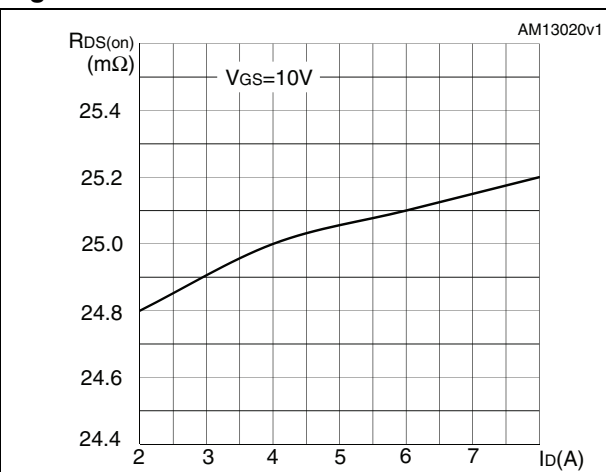


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

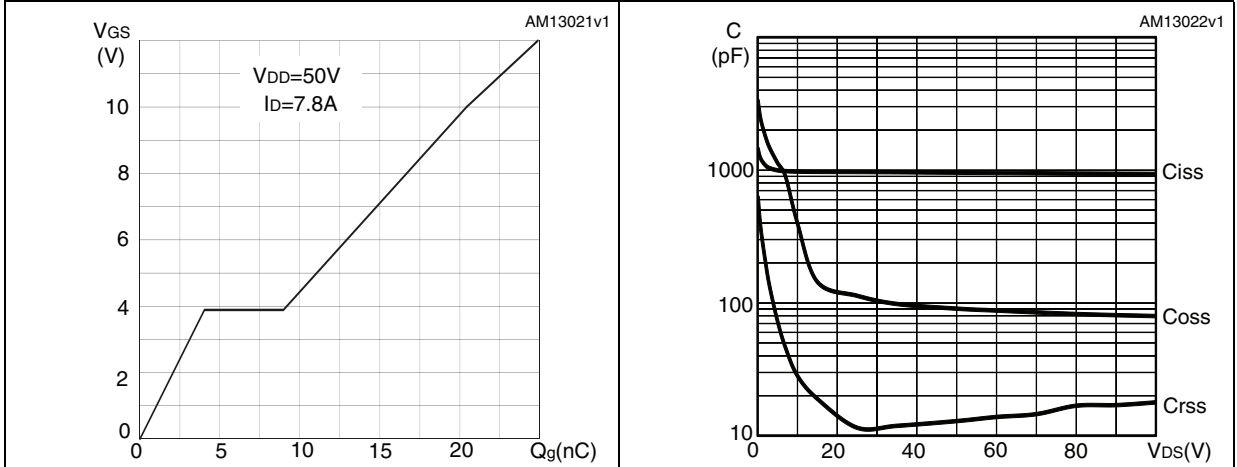
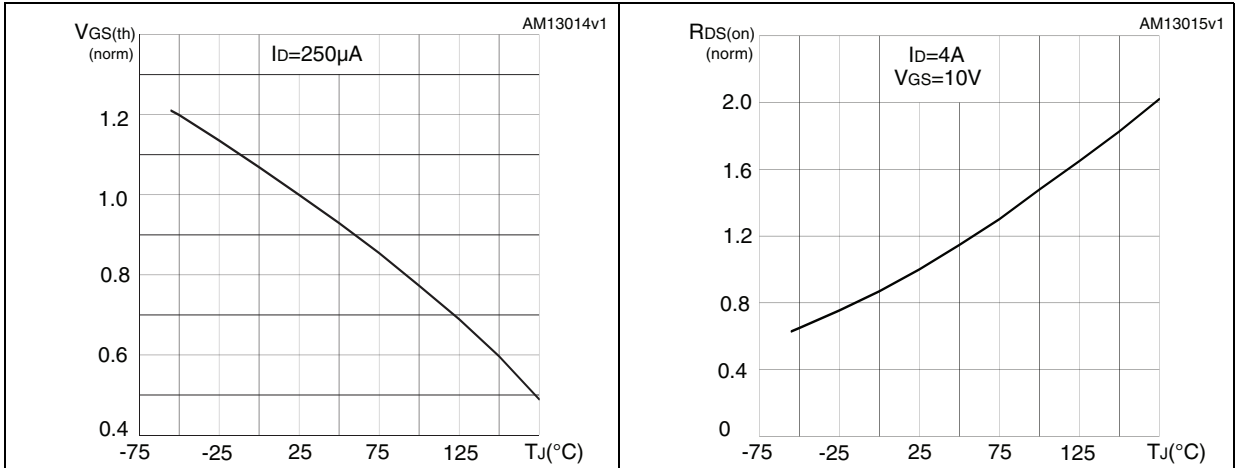


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature







## 4 Package mechanical data

**Table 8. PowerFLAT 5x6 type S-R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 18. PowerFLAT 5x6 type S-R drawing

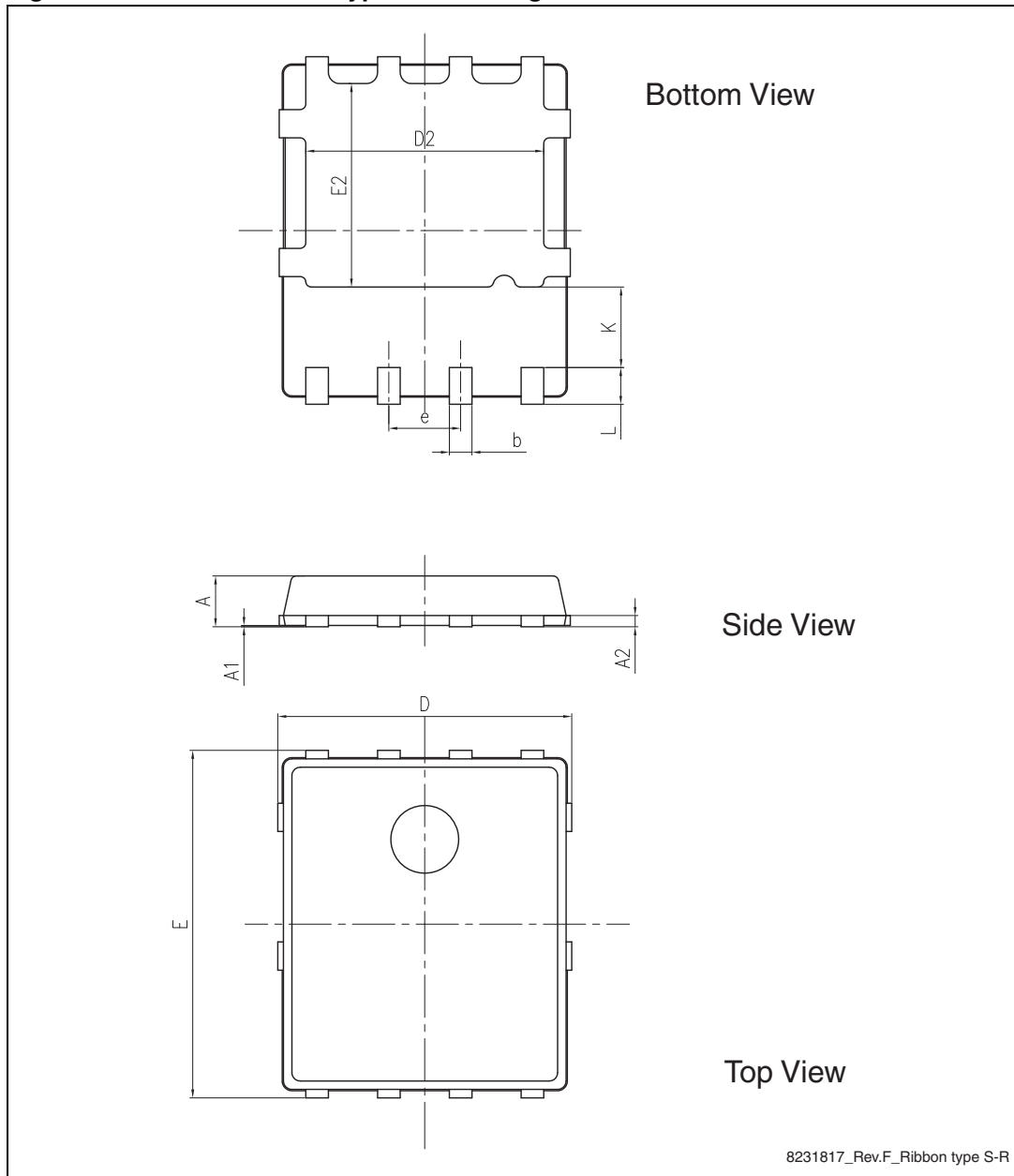
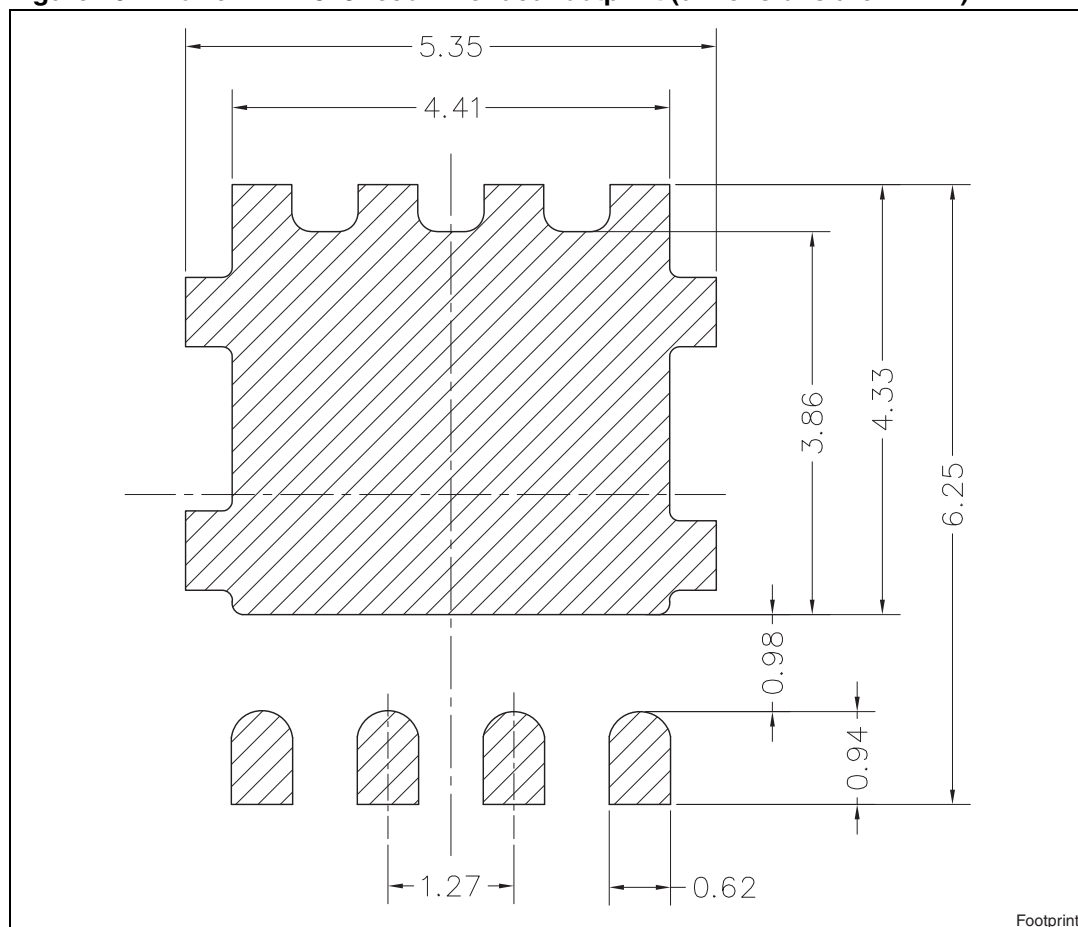


Figure 19. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
17-Jan-2013	1	First release.

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