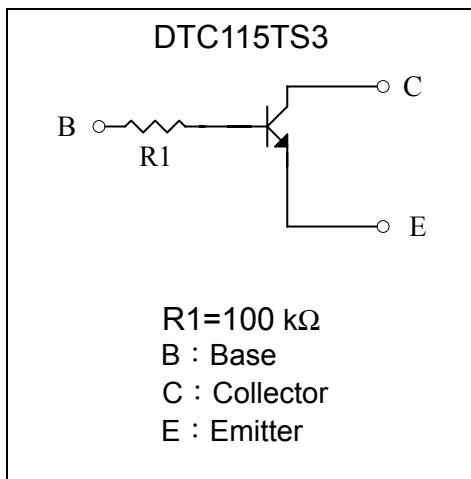
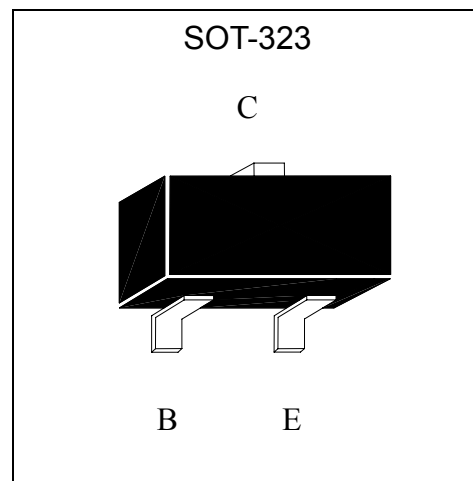


**NPN Digital Transistors (Built-in Resistors)**

# DTC115TS3

**Features**

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA115TS3.
- Pb-free & Halogen-free package.

**Equivalent Circuit**

**Outline**

**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	50	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C</sub>	100	mA
Power Dissipation	P <sub>d</sub>	200	mW
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C



**Electrical Characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Collector-Base Breakdown Voltage	V <sub>CB0</sub>	50	-	-	V	I <sub>C</sub> =50μA
Collector-Emitter Breakdown Voltage	V <sub>CEO</sub>	50	-	-	V	I <sub>C</sub> =1mA
Emitter-Base Breakdown Voltage	V <sub>EB0</sub>	5	-	-	V	I <sub>E</sub> =50μA
Collector-Base Cutoff Current	I <sub>CB0</sub>	-	-	0.5	μA	V <sub>CB</sub> =50V
Emitter-Base Cutoff Current	I <sub>EB0</sub>	-	-	0.5	μA	V <sub>EB</sub> =4V
Collector-Emitter Saturation Voltage	V <sub>CE(sat)</sub>	-	-	0.3	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0.1mA
DC Current Gain	h <sub>FE</sub>	100	-	600	-	V <sub>CE</sub> =5V, I <sub>C</sub> =1mA
Input Resistance	R	70	100	130	kΩ	-
Transition Frequency	f <sub>T</sub>	-	250	-	MHz	V <sub>CE</sub> =10V, I <sub>C</sub> =5mA, f=100MHz *

\* Transition frequency of the device

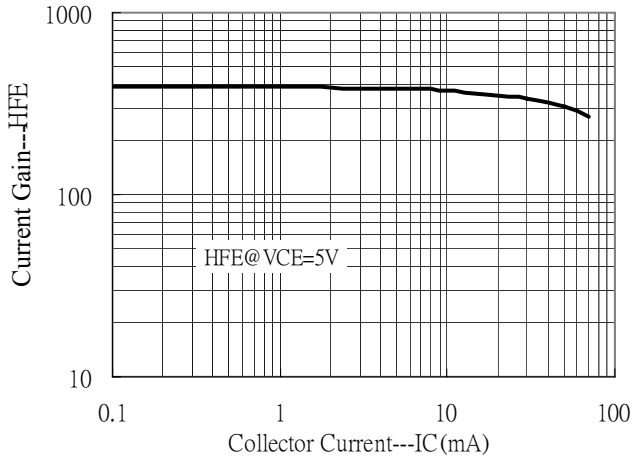
**Ordering Information**

Device	Package	Shipping	Marking
DTC115TS3	SOT-323 (Pb-free & Halogen-free package )	3000 pcs / Tape & Reel	8U

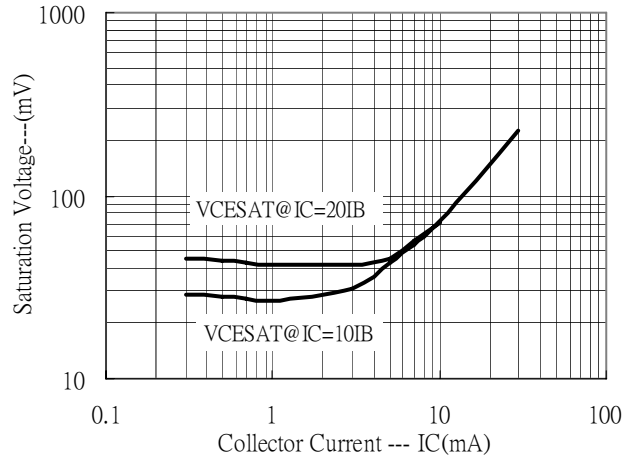


### Characteristic Curves

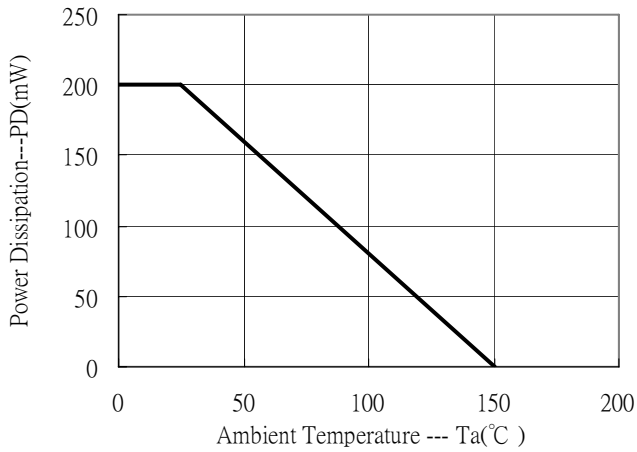
Current Gain vs Collector Current



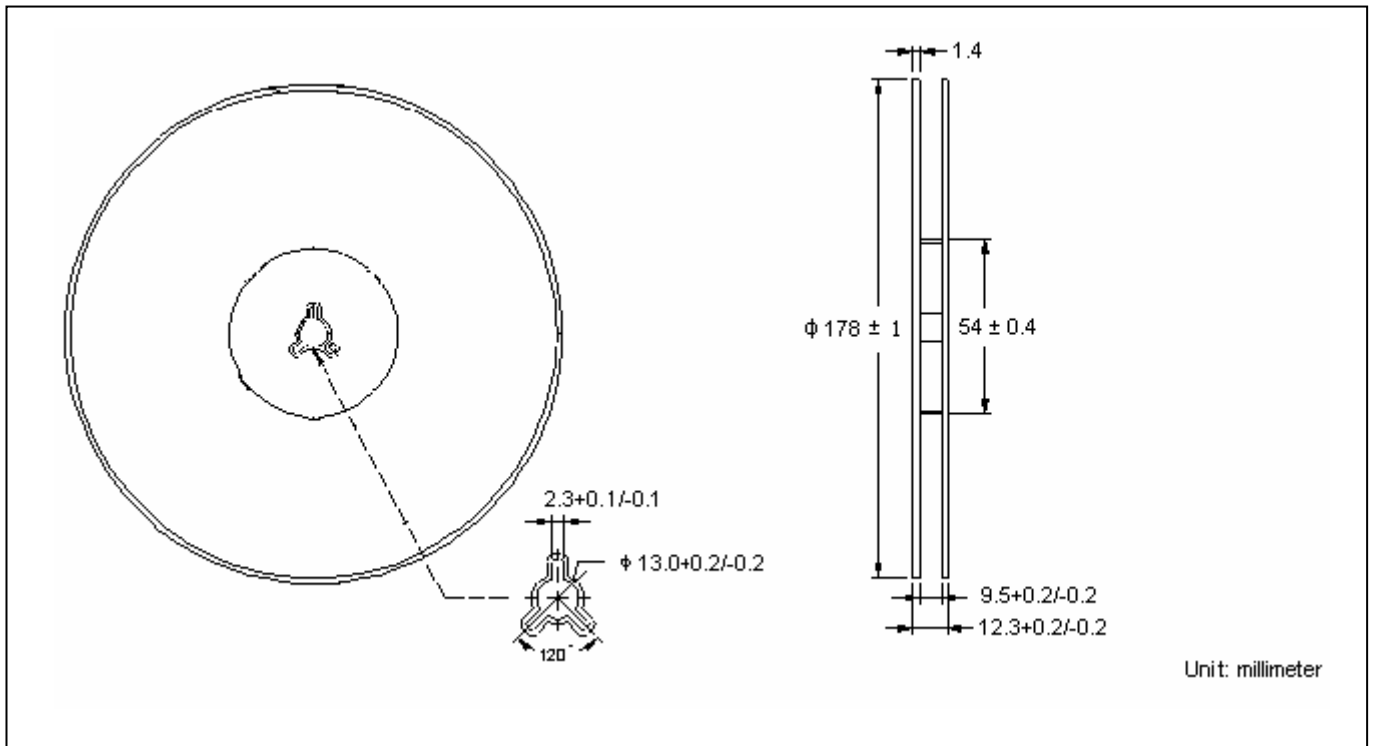
Saturation Voltage vs Collector Current



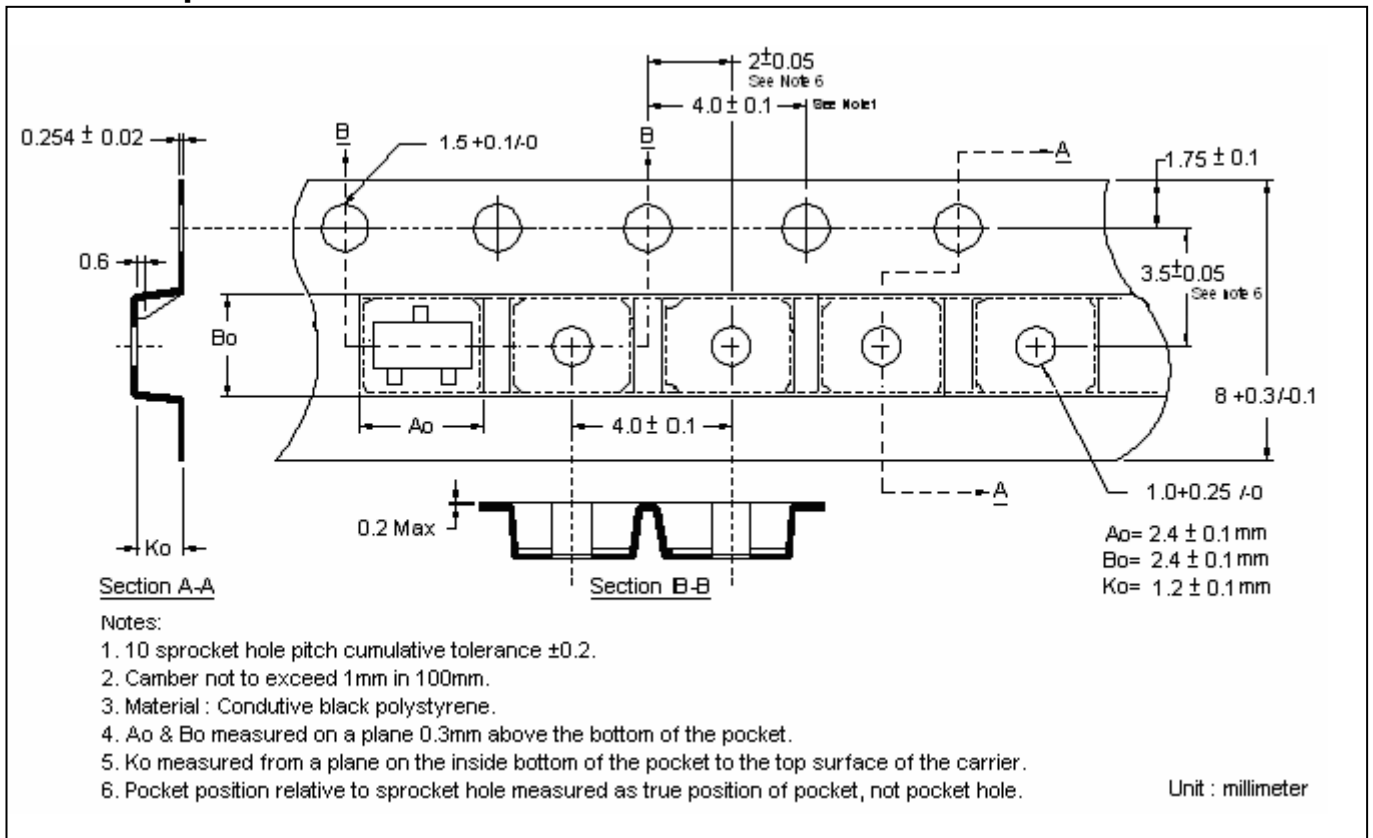
Power Derating Curve



### Reel Dimension



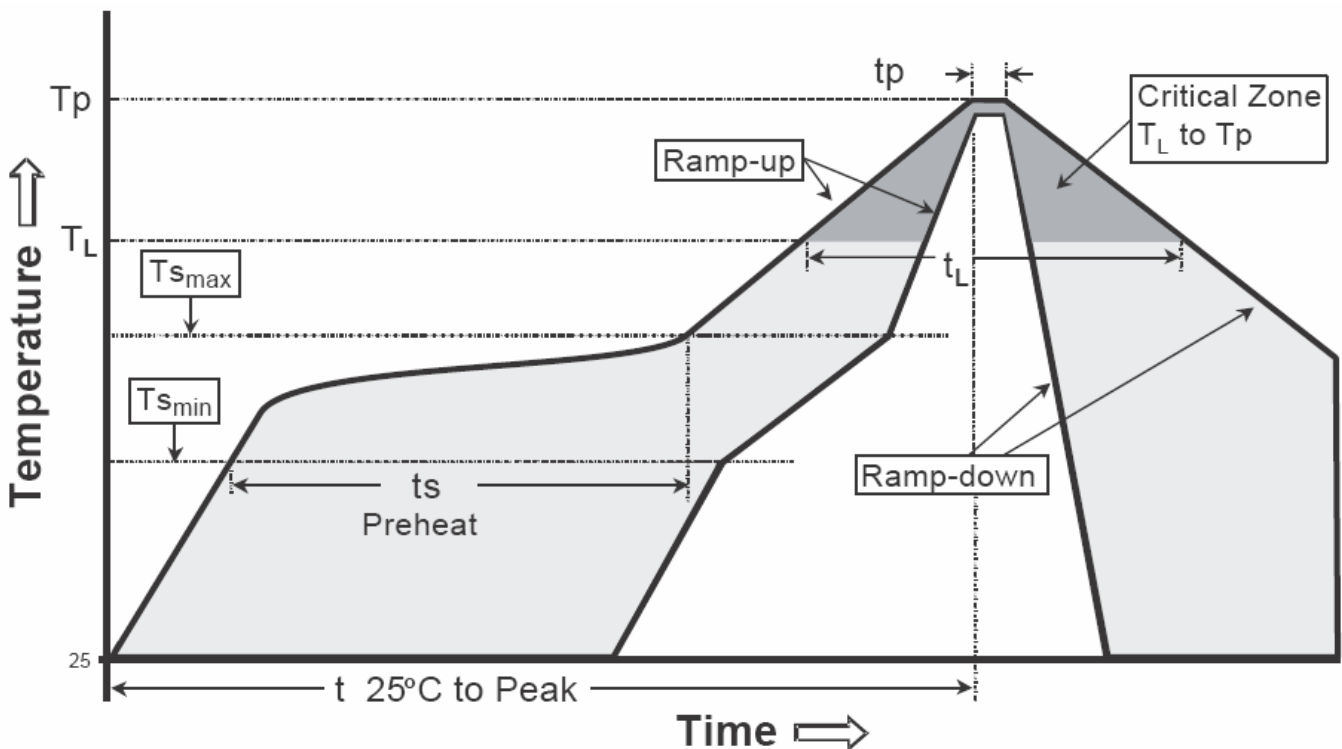
### Carrier Tape Dimension



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

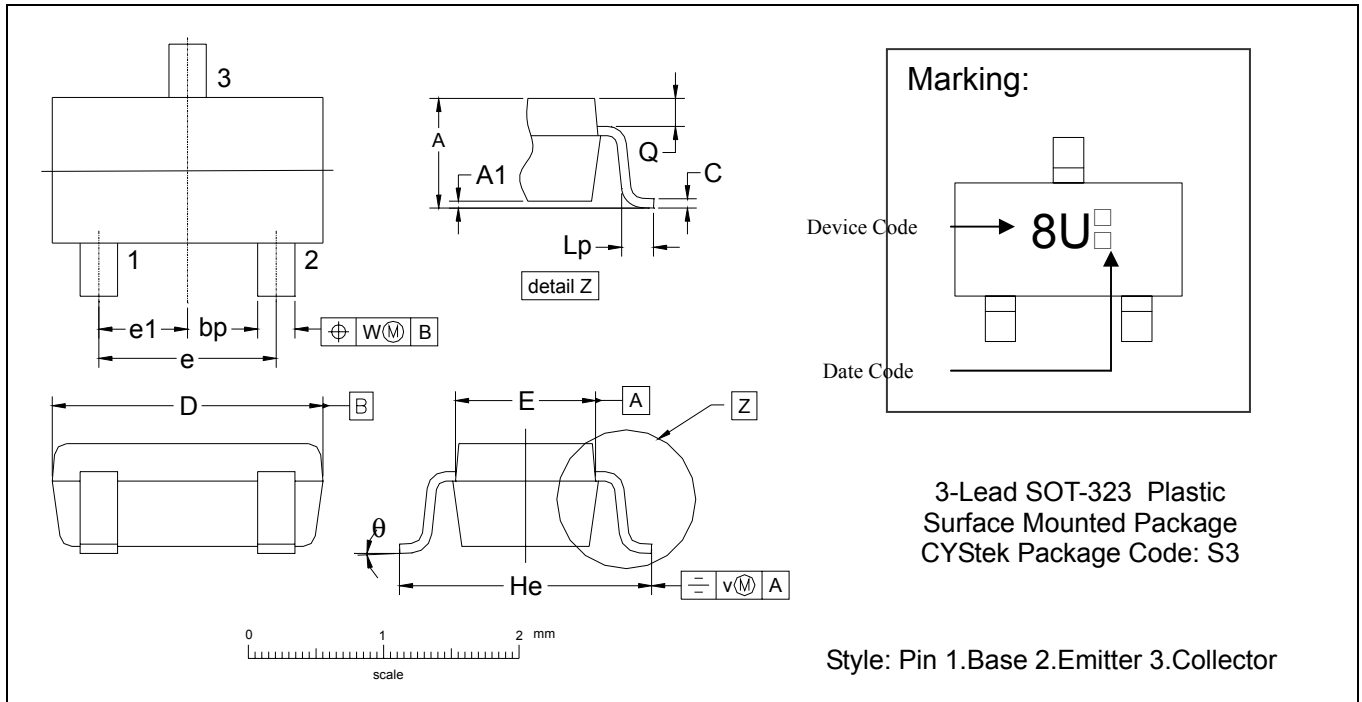
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Ts_max to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts_min)	100°C	150°C
-Temperature Max(Ts_max)	150°C	200°C
-Time(ts_min to ts_max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T_L)	183°C	217°C
- Time (t_L)	60-150 seconds	60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-323 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0315	0.0433	0.80	1.10	e1	0.0256*		0.65*	
A1	0.0000	0.0039	0.00	0.10	He	0.0787	0.0965	2.00	2.45
bp	0.0118	0.0157	0.30	0.40	Lp	0.0059	0.0181	0.15	0.46
C	0.0031	0.0098	0.08	0.25	Q	0.0051	0.0091	0.13	0.23
D	0.0709	0.0866	1.80	2.20	v	0.0079	-	0.2	-
E	0.0453	0.0531	1.15	1.35	w	0.0079	-	0.2	-
e	0.0472	0.0551	1.20	1.40	θ	0°	10°	0°	10°

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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