TW8833/TW8833S – TFT Display Controller

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Introduction

Applications

- In-car display controller
- Portable DVD and DVRs players
- Portable media player

Description

The TW8833 incorporates many of the features required to create multi-purpose in-car LCD display system in a single package. It integrates a high quality 2D comb NTSC/PAL/SECAM video decoder, triple high speed RGB ADCs, high quality scaler, triple DACs and images enhancement functions which include Black and White Stretch and etc. It also supports panoramic scaling for conversion to wide screen display. On the input side, it supports a rich combination of CVBS, S-video and analog component inputs. On the output side, it supports analog panel type with its built-in timing controller.

– Analog Video Decoder

– NTSC (M, 4.34) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection

– Three 10-bit ADCs and analog clamping circuit

– Fully programmable static gain or automatic gain control for the Y or CVBS channel

– Programmable white peak control for the Y or CVBS channel

– Software selectable analog inputs

– High quality adaptive 2D comb filter for both NTSC and PAL standards

– PAL delay line for color phase error correction

– Image enhancement with 2D dynamic peaking and CTI

– Digital sub-carrier PLL for accurate color decoding

– Digital horizontal PLL and Advanced synchronization processing for VCR playback and weak signal performance

– Programmable hue, brightness, saturation, contrast and sharpness

– High quality horizontal and vertical filtered down scaling with arbitrary scale down ratio

– Detection of level of copy protection according to Macrovision standard

TFT Panel Support

– Built-in programmable timing controller

– Supports 3, 4, 6 or 8 bits per pixel up to 16.8 million colors with built-in dithering engine

– Support analog panel up to WQVGA resolution

– Support Serial (8bit) RGB panel

On Screen Display

– Integrated 256 programmable font RAM and 384 display RAM

– Four windows font OSD with bordering / shadow

– Supports bit-mapped based OSD through SPI (TW8833S only)

Image Processing

– High quality scaler with both up/down and nonlinear scaling support

– Built-in 2D de-interlacing function

– Programmable hue, brightness, saturation, contrast and peaking

– Supports programmable cropping of input video and graphics

– Independent RGB gain and offset controls

– Panorama / Water-glass scaling

– Programmable 10-bit Gamma correction for each color

– Operated in Frame Sync mode

– Black/White Stretch

Clock Generation

– Spread spectrum clock

– Modulation frequency and spread width are selectable

Power Management

– Supports functional based independent power down control.

– 1.8 / 3.3 V operation

Miscellaneous

– Supports 2-wire serial bus interface

– Built-in single LED back light controller

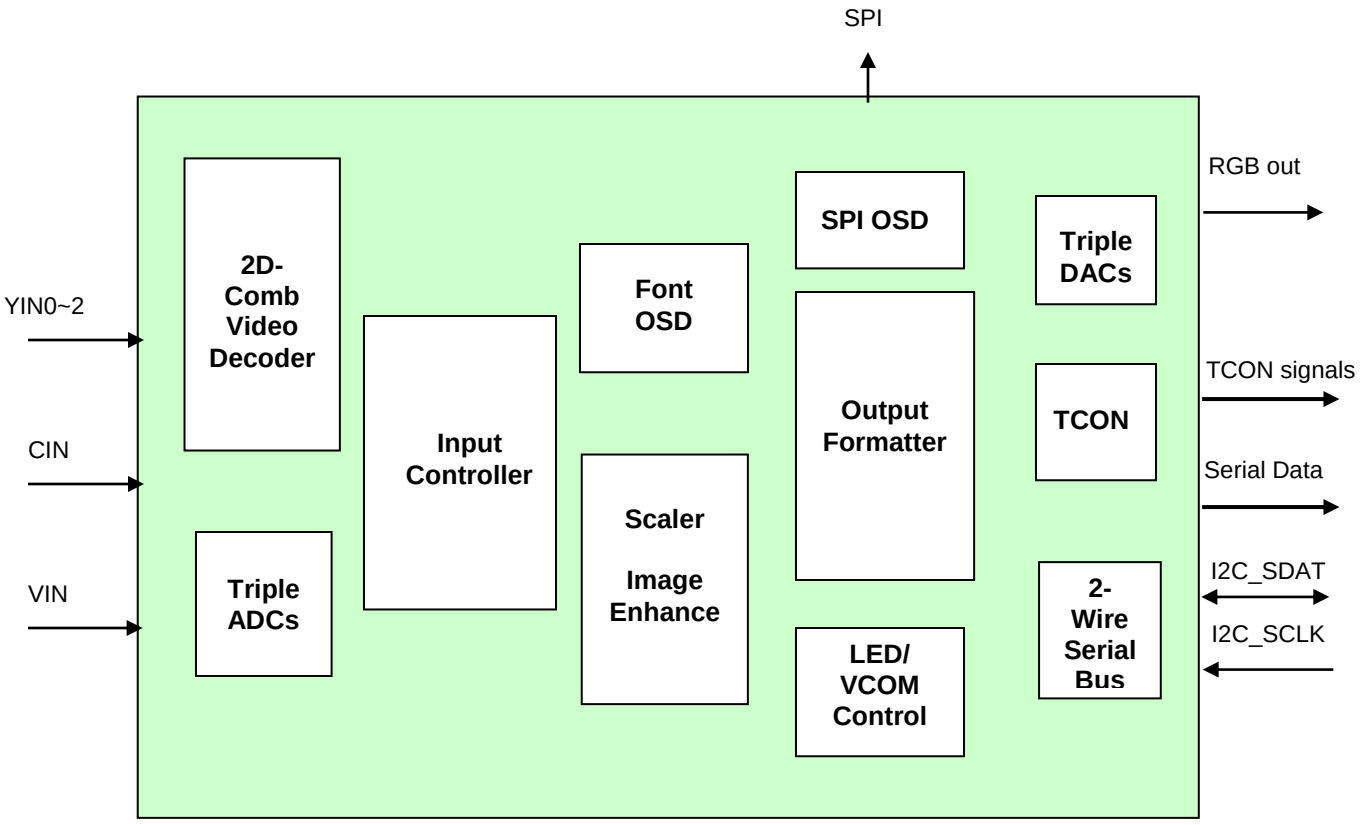
– Built-in VCOM DC voltage

– Built-in VCOM analog amplitude

– Built-in DC-DC convertor

– Single 27MHz crystal

– 48 pin QFN package



Functional block diagram

Order Information

Package Description

Part #	Name	Description	Pin Count	Body Size
TW8833-DENA1-GR	QFN	Quad Flat No-lead	48	7x7 mm^2
TW8833S-DENA1-GR	QFN	Quad Flat No-lead	48	7x7 mm^2

Functional Description

Overview

Intersil|Techwell's TW8833 Flat Panel TV/Monitor controller is a highly integrated TFT panel controller. It integrates a high quality 2D comb NTSC/PAL/SECAM video decoder, scalers, timing controller, triple DACs and flexible font based multi-window OSD engine. This unique level of mixed signal integration turns a TFT panel into a flexible display system. It incorporates easy-to-operate features in a single package for multi-purpose in-car LCD display, portable DVD and DVRs media players.

It contains all the logic required to convert analog or digital video signals in various formats to the signal formats that is necessary to drive various kind of TFT panel types. It supports different panel resolutions depending on the scaler and panel clock settings. It has built-in TCON for direct connecting with low cost TCON-less panel.

The integrated analog front-end contains ADCs with clamping circuits and Automatic Gain Control (AGC) circuit as well as anti-aliasing filter to minimize external component count. The built-in video decoder employs proprietary 2D Comb filter Y/C separation technologies to produce exceptionally high quality pictures.

The chip's internal logic synchronizes the panel frame rate to the incoming input frame rate. A high quality image-scaling engine is used to convert the different input resolution formats to the output panel resolution. An internal de-interlacing engine also allows interlaced video to be displayed.

On Screen Display is supported through on-chip multi-window OSD engine for maximum flexibility.

It also has built-in back light controller and panel bias voltage generator to further simplify the system design. The host control interface supports the standard 2-wire serial bus

Analog Front-end

The analog front-end converts analog video signals to the required digital format. Each channel contains automatic clamping circuit, AGC circuit, anti-aliasing filter and high performance ADCs to minimize the external component used. The clamping circuit restores the signal DC level so it can be properly digitized. The analog inputs source selections are software programmable. Different input source has different signal conditioning logics to properly convert the signal into correct format for further processing

Video Decoder

Sync processor

The decoder sync processor of video input detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-Video signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. It has wide lock-in range for tracking any non-standard video signal.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. A detection window controls the determination of sync. This provides more reliable synchronization. It

simulates the functionality of a PLL without the complexity of a PLL. The field status is determined at vertical synchronization time based on the vertical and horizontal sync relationship.

Color Decoding

Y/C separation

The color-decoding block contains the luma / chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma / chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter can be found in the filter curve section.

In the case of comb filter, the decoder separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary adaptive comb algorithm. It leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color demodulation

The color demodulation for NTSC and PAL standard is done by quadrature mixing the chroma signal to the base band and extracting the chroma components with low-pass filter. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM color demodulation process consists of bell filtering, FM demodulator and de-emphasis filtering. The chroma carrier frequency is identified in the process and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by transmission loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then compensated in amplitude accordingly. The range of ACC control is –6db to +24db.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

Automatic standard detection

The video decoder has its automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

The integrated video decoder supports all common video formats as shown in Table 1. It needs to be programmed appropriately for each of the composite video input formats.

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.58 MHz	Japan
PAL-B, G, N	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	3.58 MHz	Brazil
PAL-CN	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43 MHz	China
NTSC (4.43)	525	60	4.43 MHz	Transcoding

Table 1. Video Input Formats Supported

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The video decoder adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

It also provides a sharpness control function through a control register. The center frequency of the peaking filter is selectable. A coring function is provided along with the sharpness control to reduce enhancement to the noise.

The Hue and Saturation

When decoding NTSC signals, the decoder can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Input Image Control

The input cropping control provides a way for programming the active display window region for the selected input video or graphic. In the normal operation, the first active line starts with the VSYNC signal. This and vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in one pixel increments for single pixel input mode or two pixels increments for double pixels input mode. If data qualifier is used, then only qualified pixels will be counted in the window size.

Image Scaling

The internal high quality image-scaling engine can scale up or down the input image to fit the output panel resolution. It operates in the frame-sync mode such that both input and output frame rates are always the same. The vertical and horizontal scaling ratio can be adjusted independently in fine granularity. The panel clock frequency selection needs to be coordinated with the scaling ratio as well as input frequency to avoid internal buffer overrun. The scaler also acts as a de-interlacer to properly de-interlace the input video based on its field nature. The scaler can also be programmed to perform the panorama or water glass mode scaling for flexible display output. In addition, the image mirroring can be supported through scaler with register control.

Image Enhancement Processing

Black/White Stretch

This feature is to expand dynamic range of the input image, which creates more vivid image impression.

TFT Panel Support

It supports a variety of active matrix TFT panel types and resolutions.

Dithering

It has the dithering circuit to reduce the output dynamic range to fit the panel type. This allows LCD panels with 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel to can display up to 2.1 million colors. It employs both spatial and frame modulation dithering. When dithering with the least significant 4-bits of input data it uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, it uses either spatial modulation with 2x2 pixel blocks, or frame modulation.

Gamma Table

It has integrated gamma table for each color output and it is fully programmable through host bus.

TCON

The integrated Timing controller supports flexible column/row driver control signals to interface with TCON-less panel directly.

Font On Screen Display

The TW8833 supports built-in OSD controller with programmable RAM font. The OSD display is independent of the input active window setting or the scaling ratio.

The on-chip OSD controller is a character-based controller. The pre-defined character or graphic bit map is stored in the font RAM. It can store up to 256 fonts. Each character is 12 pixels wide by 18 pixels high. The characters can be displayed on the screen in four user defined window locations of any size from 1 to 384 characters. The spaces between characters are also programmable. There is a limit of 384 characters that may be displayed on screen at one time in all windows combined. The attributes of each window can also be set to give it a shadow effect or 3-D effect. In addition, the characters can be expanded by a factor of 2,3 or 4 in vertical or horizontal directions and have the blinking effect, italic effect, under line effect and border/shadow effect on a character by character basis.

On chip OSD functions

% Font SRAM : Max 256 User Programmable Single Color Font (6912x8 SRAM)

- % Character Register SRAM : 384 Location (8-bit Font Address + 12-bit Character Attribute, 384x20 SRAM)
- % Characters
  - Character Color : 16 colors
  - Character Background Color : 16 colors
  - Character Blinking : Enable/Disable, 1 Hz Blinking frequency
  - Character Italic Effect : Enable/Disable
  - Character Under Line Effect : Enable/Disable
  - Character Border/Shadow Effect : Enable/Disable
    (Multi OSD Window Display Case : Chip has a limitation)
  - Character Space : Both H and V programmable by number of pixels
  - Quick Character Change in Window : Programmable Start Address and Buffer Size
  - Programmable OSD Color Palette Support
  - Re-designed OSD Font Supporting Standard Alpha-Numerical Character Set

% Windows

- Number of Windows : 4 Independent Windows
- Window Color : 16 colors
- Window Zoom : 2, 3, 4 times zoom by dot number, H/V separate zooming control
- Window Position : Programmable
  H Direction : 1-pixel per step, V Direction : 1-Line per step
- Window Size : Both H and V programmable by number of characters
- Window Bordering/Shadowing Effect : 4 Independent Windows Enable/Disable Control
- Window Alpha Blending Control : 4 Independent Windows Control
  → 16 Different Color for Alpha Blending support(4-bit control)
- Window 3-D Effect : 4 Independent Windows Enable/Disable Control
- Window Border Color : 16 Colors
- Window Border Width : programmable

Basic register setting flow example for Built-in OSD controller

Step_1: OSD_WINDOW_CONFIGURATION setting for Window#1 (0x310~0x31F)

Note) Window#2 (0x320~0x32F), Window#3 (0x330~0x33F), Window#4 (0x340~0x34F)

1. OSD Window Disable	0x310, bit7
2. OSD Window Zoom multiplier	0x310, bit1-0: V, bit3-2:H
3. OSD Window Background B Color	0x31E, bit6-4
4. OSD Window Background G Color	0x31E, bit6-4
5. OSD Window Background R Color	0x31E, bit6-4
6. OSD Window Background Color Extension	0x31E, bit7
OSD Window 3-D Effect Top/Bottom Mode Select	0x31B, bit6
8. OSD Window 3-D Effect Level Select	0x31B, bit5
9. OSD Window 3-D Effect Enable/Disable	0x31B, bit7
10. OSD Window H-Start Location (see details in next page)	0x313, bit7-0 0x312, bit6-4
11. OSD Window V-Start Location (see details in next page)	0x314, bit7-0 0x312, bit1-0
12. OSD Window Width	0x316, bit5-0
13. OSD Window Height	0x315, bit5-0
14. OSD Window Border_Line Width	0x318, bit4-0
15. OSD Window Border_Line B color	0x317, bit2-0
16. OSD Window Border_Line G color	0x317, bit2-0
17. OSD Window Border_Line R color	0x317, bit2-0
18. OSD Window Border_Line Enable	0x318, bit7
19. OSD Window Border Color Extension	0x317, bit3
20. OSD Window Shadow Width	0x31C, bit4-0
21. OSD Window Shadow B color	0x31B, bit2-0
22. OSD Window Shadow G color	0x31B, bit2-0
23. OSD Window Shadow R color	0x31B, bit2-0
24. OSD Window Shadow Enable	0x31C, bit7
25. OSD Window Shadow Color Extension	0x31B, bit3
26. OSD Window H-Space Width (Between Border_line and Characters)	0x319, bit6-0
27. OSD Window V-Space Width (Between Border_line and Characters)	0x31A, bit6-0
28. Character H-Space Width (Between Character and Character)	0x31D, bit7-4 0x31C, bit6
29. Character V-Space Width (Between Character and Character)	0x31D, bit3-0 0x31C, bit5
30. OSD Window Alpha Blending Color Select	0x311, bit7-4
31. OSD Window Alpha Blending Value Control	0x311, bit3-0
32. Window content start address	0x305, bit0 0x306, bit7-0
33. Repeat 1 – 32	

Step_2: OSD_COLOR_ATTRIBUTE / FONT setting (OSD RAM)

1. Enable OSD RAM Access - 0x304 (bit0 = 0)
2. OSD RAM Address - 0x305 (bit0), 0x306 (bit7-0)
   - The first address is Step_1_32 Window content start address.
3. OSD RAM Data Port High (Font Address)
   - 0x307 Data is written to above address automatically.
   - 0x307=8'hfe : FONT_RAM h00 to hff (Max 256 characters)
4. OSD RAM Data Port Bit19(Border Effect), Bit18(Under Line Effect), Bit17(Italic Effect), Bit16 (Blinking Effect)
   - 0x304 Bit7, Bit6, Bit5, Bit4 Data is written to above address automatically.
5. OSD RAM Data Port Low (Color Attribute)
   - 0x308 Data is written to above address automatically.
6. Repeat 2), 3), 4), 5) .
   -The address should be increased by one each.

Step_3: COLOR LOOK-UP TABLE setting

1. Select Color Look-Up Table Write Address - 0x30C (bit[3:0])
   - BIT[3:0] : These 4 bits specify one of the 16 entries in the look-up table. Each entry is a 16-bit RGB color by its content.
   - There are 65536 colors available; but only sixteen of them are accessible by OSD controller at a given time.

BIT[3:0]	Default Value
0000	0000h
0001	0010h
0010	0400h
0011	0410h
0100	8000h
0101	8810h
0110	8400h
0111	8410h
1000	2104h
1001	0008h
1010	0200h
1011	0208h
1100	4000h
1101	4008h
1110	4200h
1111	FFFFh

2. Color Look-Up Table control bits setting - 0x30D (High Byte), 0x30E (Low Byte)
   - The data of the Look-Up Table is accessed through 0x30D and 0x30E.

3. Repeat 1), 2) to program each entry of the Look-Up Table.

Step_4: FONT_RAM_DATA setting (FONT RAM)

1. Enable FONT RAM Access - 0x304 (bit0 = 1)
2. FONT RAM Address Setting - 8 bits(h00 – hFF) - 0x309
   - h00~hFF : Single Font RAM(256 Programmable Characters)
3. FONT RAM Data Port
   - 0x30A Data is written to above address automatically.
4. Repeat (4) at 27 times for one FONT RAM Data
   - The internal address automatically increases by one each.
5. New FONT RAM Address Setting – 8 bits
6. Repeat 3),4),5)
   - The FONT RAM Address should be increased by one each.

Note) As for the FONT RAM configuration and font bit mapping, see the detailed description

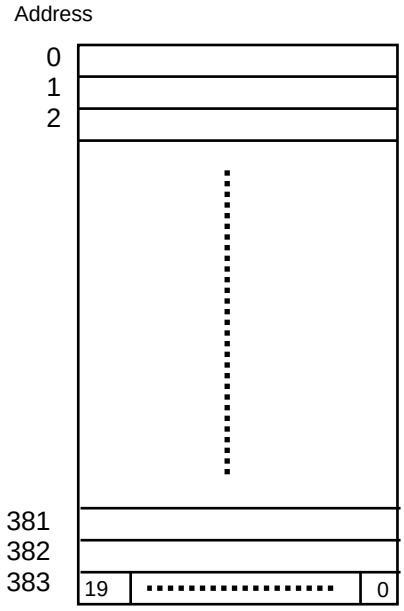
Step_5: End of OSD setting and Enable OSD

1. OSD On/Off Enable Control 0: ON, 1: OFF - 0x30C (bit4 = 0)
2. OSD Window Enable - 0x310 (bit7 = 1) Window1 Enable

OSD Window Start Location: Built-in OSD controller

- Internal generated OSD DE Position delayed from H-SYNC: 0x303[7:0].
- OSD window H_start location from start of internal OSD DE: 0x312[6:4], 0x313[7:0] increment by 1 pixel at a time.
- OSD window V_start location from start of VACT: 0x312[1:0], 0x314[7:0] increment by 1 line at a time.

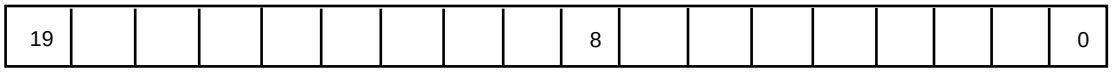
OSD_RAM Configuration



The characters can be displayed on the screen in four user defined window locations of any size from 1 to 384 characters. There is a limit of 384 characters that may be displayed on screen at one time in all windows combined.

Example

Window #1: Address 0 – 2 (3 characters)
Window #2: Address 3 – 100 (98 characters)
Window #3: Address 101– 254 (154 characters)
Window #4: Address 383 (1 character)



FONT_ADDRESS (12-bits)

Bit 19: Border/Shadow
Bit 18: Under Line Effect ON
Bit 17: Italic Effect ON
Bit 16: Blinking
Bit 15 - 8: FONT Address

FONT_ATTRIBUTE (8-bits)

Bit 7: Character's background color extension
Bit 6: Character's background R
Bit 5: Character's background G
Bit 4: Character's background B
Bit 3: Character's color extension
Bit 2: Character R
Bit 1: Character G
Bit 0: Character B

Alpha Blending for OSD Window

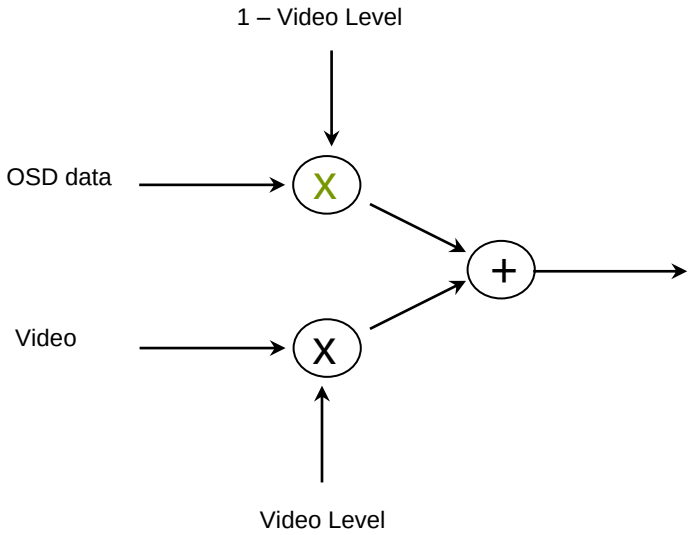
The TW8833 uses "Alpha Blending" in OSD 4 separation windows & 16 separation colors. Alpha blending mixes (adds) the video signal and OSD signal at the following specified levels. In other words, alpha blending determines the transparency of the OSD window each color to in relation to video signal. When alpha blending is disabled, the only OSD data is displayed in OSD window.

The alpha blending level selection are 4-bit assigned, it can support 8 different level controls.

The alpha blending level bits and alpha blending color selection bits are in register 0x311 for window#1, 0x321 for window#2, 0x331 for window#3, 0x341 for window#4.

alpha[3:0]	Video Level
0000	0.00 %
0001	12.5
0010	25.0
0011	37.5
0100	50.0
0101	62.5
0110	75.0
0111	87.5
1000	100

Alpha Blending Concept



SPI On Screen Display (for TW8833S only)

The integrated SPIOSD provides a flexible mapping between its display on the LCD and its bit mapped image stored in the SPI memory. In general a buffer in the SPI memory is specified for the image to be displayed. The buffer size is larger than the display size of the window. The bit mapped image stored is 8 bits per pixel. During display, the 8-bit pixel is fetched from the SPI memory and mapped to a 32-bit quantity by the window's LUT (Look Up Table). The 32-bit quantity consists of 24-bit RGB, 7-bit alpha blending attribute, and one bit blinking attribute. The pixel is then mixed with video before displaying on the LCD panel.

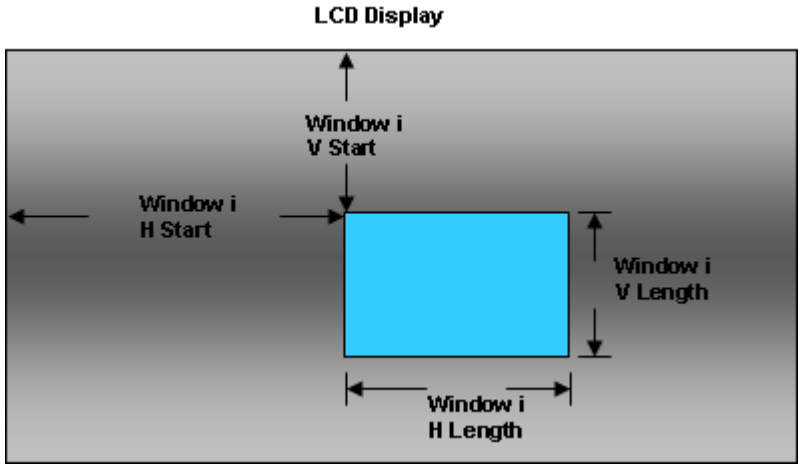
Two SPIOSD windows are provided. Each window has its own set of register but shares a LUT. Both windows can be active at the same time but cannot be overlapped and have a minimum horizontal spacing requirement.

Looping control for adjacent buffers is provided for each window. Animation can be achieved by properly allocating multiple buffers in the adjacent area and the looping control.

SPIOSD Window Display Starting Location and Sizes

There are four registers used to specify the staring location and size on the LCD:

- Window i Horizontal Start
- Window i Vertical Start
- Window i Horizontal Length
- Window i Vertical Length



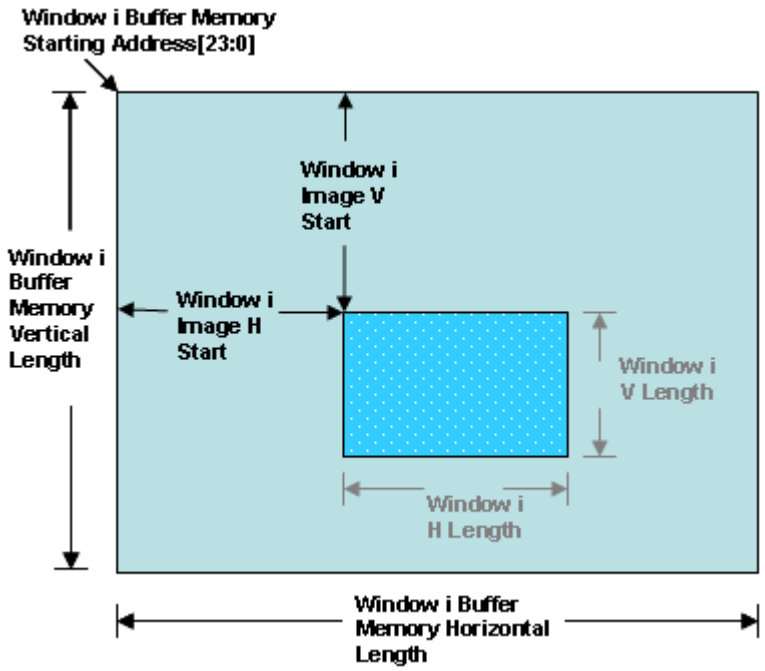
SPIOSD Window Buffer Memory

Three registers together define the buffer starting location and boundaries:

- Window i Buffer Memory Starting Address
- Window i Buffer Memory Horizontal Length
- Window i Buffer Memory Vertical Length

Two registers point to the starting location of the image stored:

- Window i Image Vertical Start
- Window i Image Horizontal Start

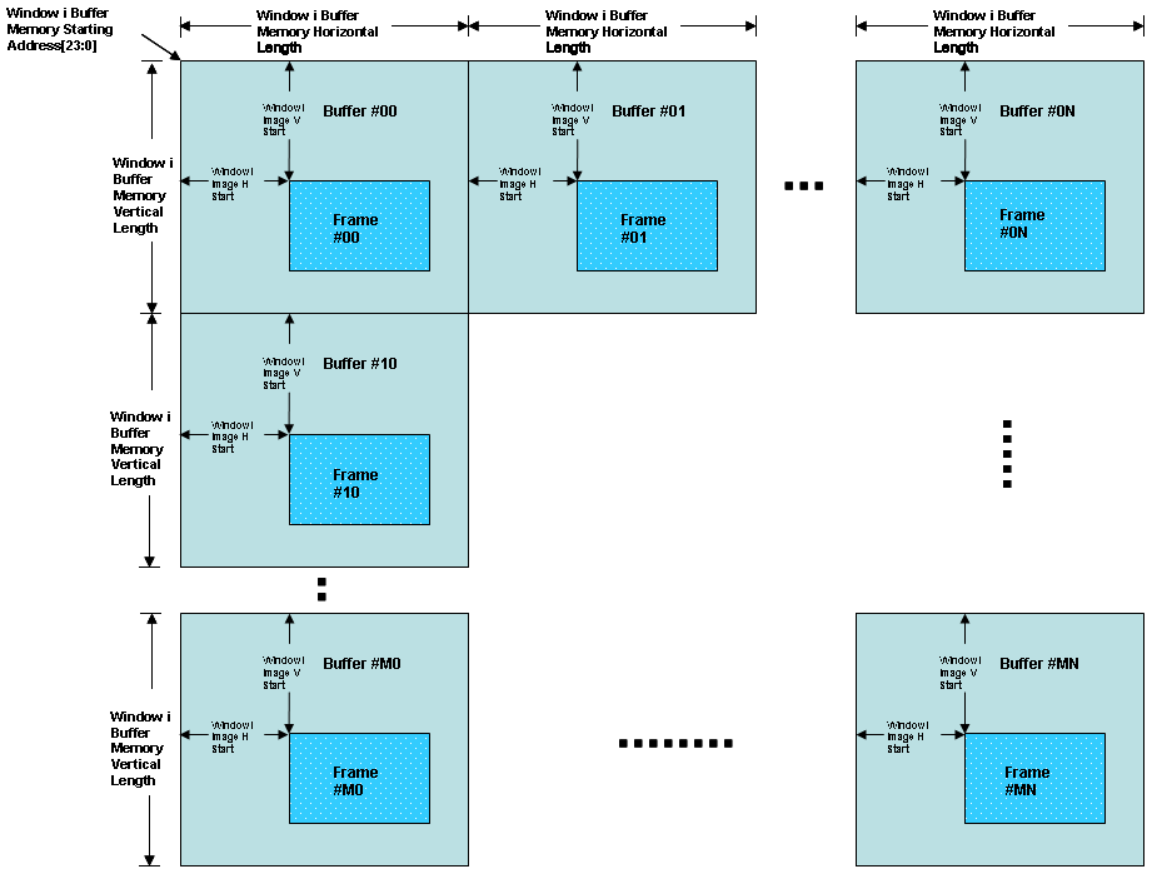


SPIOSD Window Loop Control

Three registers are used for loop control:

- Window i Looping Horizontal Frame Number
- Window i Looping Vertical Frame Number
- Window i Frame Duration

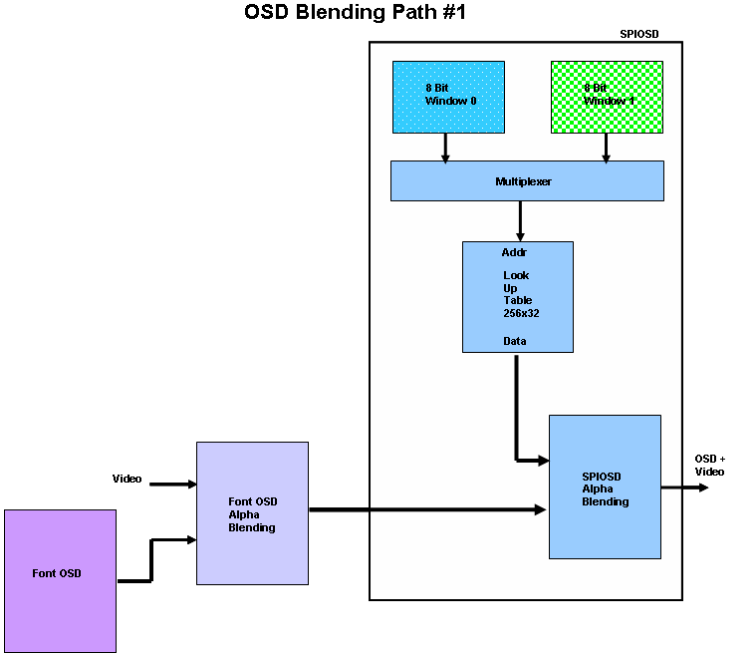
In the diagram below, the **Looping Horizontal Frame Number** register contains a value N, and the **Looping Vertical Frame Number** register contains a value M. The display starts from Frame #00 and then moves horizontally to the right and then vertically down. The display order is #00, #01, #02, … 0N, #10, #11, #12, … #1N, …. #M0, #M1, …#MN. Each frame stays on for the time specified by **Frame Duration** register.



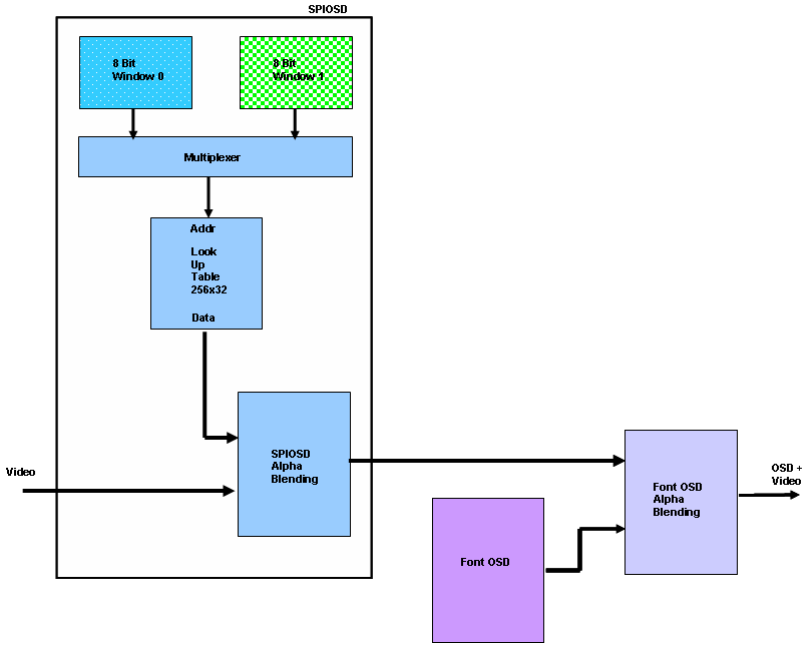
OSD Display Path

In normal mixing order, Video input is mixed with Font OSD first. The resultant output is then mixed with SPIOSD. Alternatively, Video input can be mixed with SPIOSD first and then Font OSD.

OSD Blending Path #1



OSD Blending Path #2



Microcontroller Interface

The host interface is accessed via 2-wire serial bus interface. It always operates as a slave device.

Two Wire Serial Bus Interface

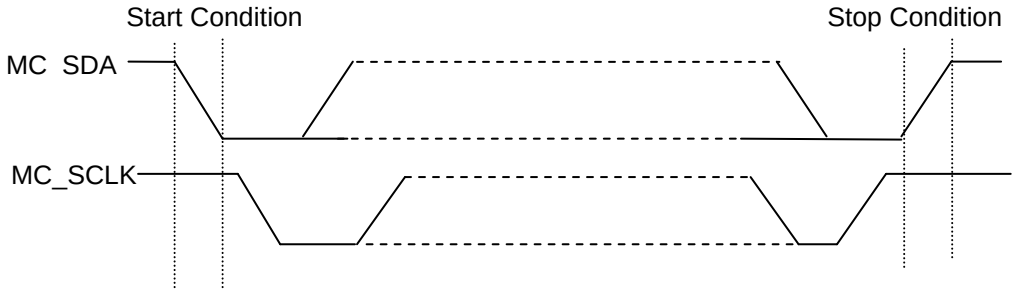


Figure 1. Definition of the serial bus interface bus start and stop

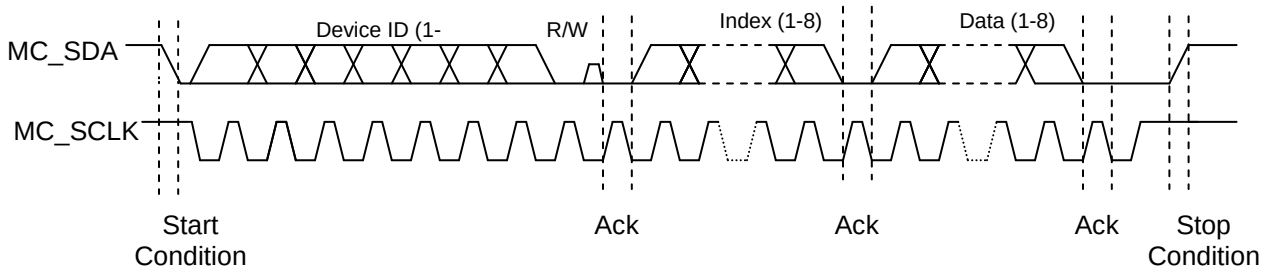


Figure 2. One complete register Write sequence via the serial bus interface

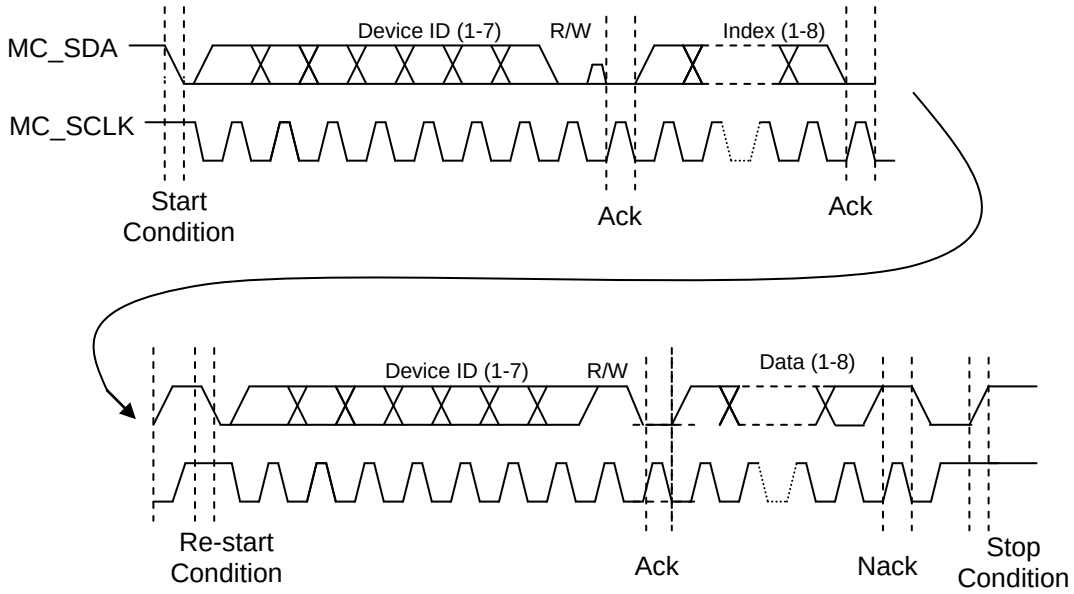


Figure 3. One complete register Read sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the internal registers. MC_SCLK is the serial clock and MC_SDA is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling MC_SCLK and MC_SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of the MC_SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever MC_SCLK is high.

The device is operated as a bus slave device. The 7-bit device address field is fixed and concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives MC_SDA from high to low, while MC_SCLK is high, this is defined to be a start condition (See Figure 1.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 2. (The next byte is normally the index to the internal registers and is a write to the device therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the MC_SDA line while holding MC_SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the MC_SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register, the master sends another 8-bit of data, it loads this to the register pointed by the internal index register. The device will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes if they are in ascending sequential order. After each 8-bit transfer the device will acknowledge the receipt of the 8-bits with an acknowledgement pulse. To end all transfers, the host has to issue a stop condition.

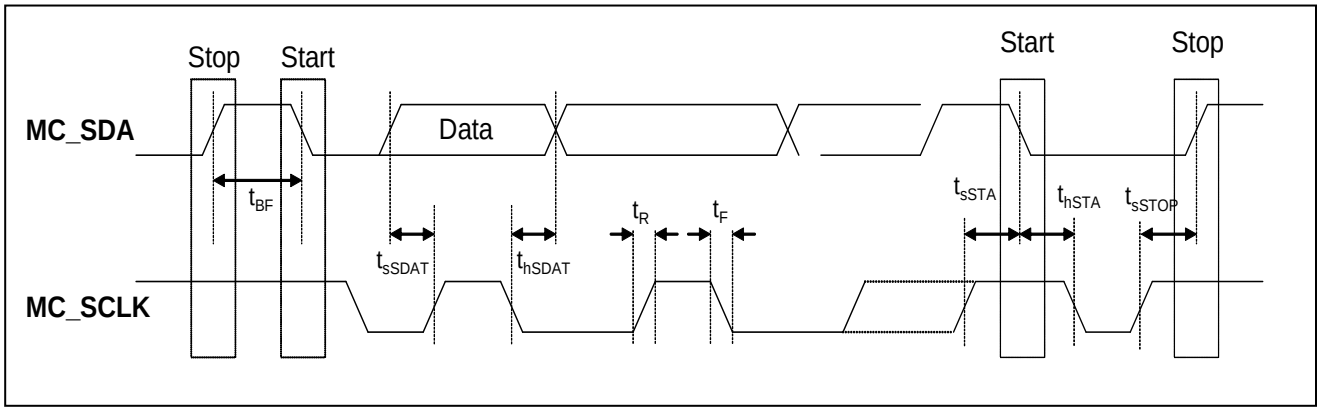
Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	1	0	1=Read 0=Write

Table 2. Serial bus interface 7-bit slave address and read write bit

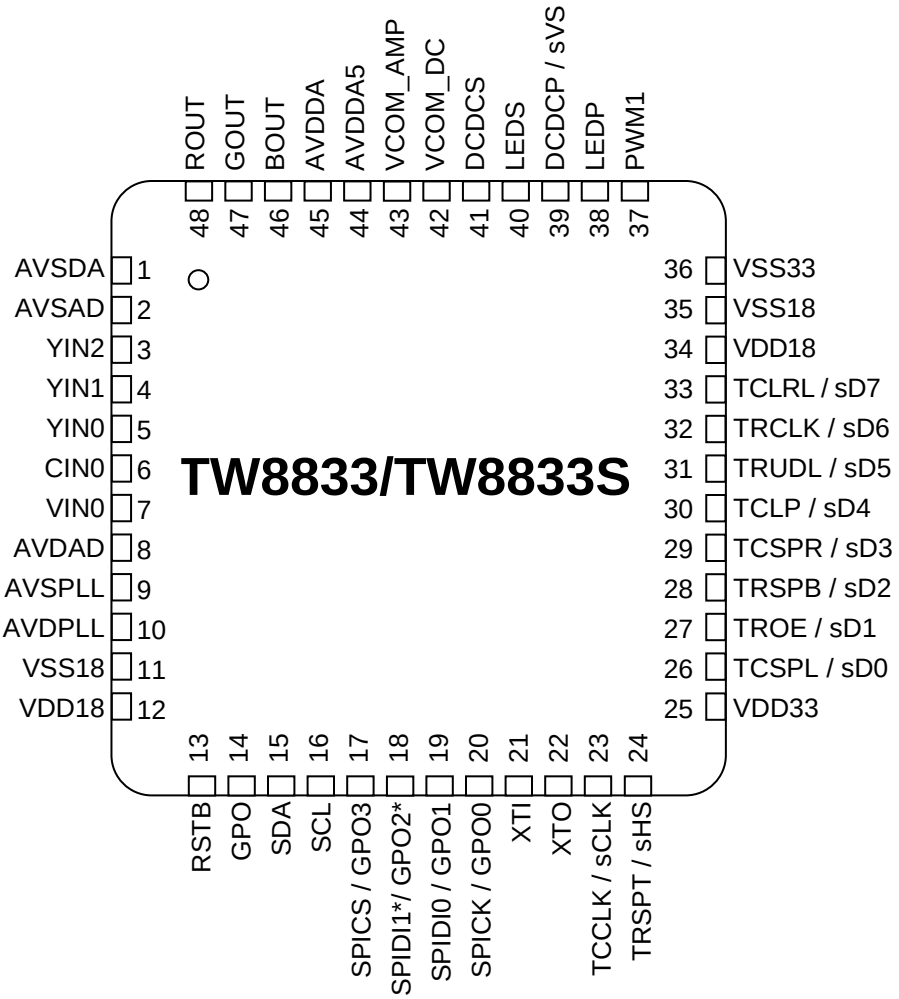
The device read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 3). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the MC_SDA line and acknowledge the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (MC_SDA is left high during a clock pulse) and issue a stop condition.

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	740	-	-	ns
MC_SDA setup time	t_{sSDAT}	74	-	-	ns
MC_SDA hold time	t_{hSDAT}	50	-	900	ns
Setup time for START condition	t_{sSTA}	370	-	-	ns
Setup time for STOP condition	t_{sSTOP}	370	-	-	ns
Hold time for START condition	t_{hSTA}	74	-	-	ns
Rise time for MC_SCLK and MC_SDA	t_R	-	-	300	ns

Table 3. Serial bus interface Timing



Pin Diagram



* for TW8833S only

Pin Description

This section provides a detailed description of each pin for the TW8833. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

The pin description also includes the buffer direction and type used for that pin.

PIN#	I/O	Pin Name	Description	Internal Connection	Recommended Connection of Unused Pin	Status at HW Reset
Analog I/F signals and Power						
2	P	AVSAD	Analog A/D Ground	-	-	Pwr
3	AI	YIN2	Analog composite or luma input 2		Connect to AVSAD	-
4	AI	YIN1	Analog composite or luma input 1			
5	AI	YIN0	Analog composite or luma input 0			
6	AI	CIN0	Analog component C input 0			
7	AI	VIN0	Analog component V input 0			
8	P	AVDAD	Analog A/D Power +1.8V		-	Pwr
9	P	AVSPLL	PLL (Internal Analog) Ground			Pwr
10	P	AVDPLL	PLL (Internal Analog) Power +1.8V			
40	AI	LEDS	LED Sense		Connect to AVSAD	Hi-Z
41	AI	DCDCS	DCDC Sense			
42	AO	VCOM_DC	VCOM out for DC		-	-
43	AO	VCOM_AMP	VCOM out for AMP TCON-Column Driver Inversion			
DAC I/F signals and Power						
44	P	AVDDA5	DAC Analog Power +5.0V	-	-	Pwr
45	P	AVDDA	DAC Analog Power +3.3V			
46	AO	BOUT	DAC Analog Blue data output		Open/Unconnected	-
47	AO	GOUT	DAC Analog Green data output			
48	AO	ROUT	DAC Analog Red data output			
1	P	AVSDA	DAC Analog Ground		-	Pwr
Digital I/F signals						
13	I	RSTB#	Reset Pin	Pull up	-	-
14	O	GPO	General Purpose Data Out	Pull up		
15	I/O	SDA	I2C Data	-	Open/Unconnected	-
16	I	SCL	I2C Clock			

17	O	SPICS	SPI Chip Select	-*	Open/Unconnected	-
	O	GPO5	GPO5			
18	I/O	SPIDI1	SPI Data 1 (for TW8833S only)			
	O	GPO2	GPO2 (for TW8833S only)			
19	I/O	SPIDI0	SPI Data 0			
	O	GPO1	GPO1			
20	O	SPICK	SPI clock			
	O	GPO0	GPO0			
21	I	XTI	Crystal terminal or oscillator input	-	-	-
22	O	XTO	Crystal terminal			
23	O	TCCLK	TCON-Column Driver clock	Pull down	Open/Unconnected	Hi-Z
	O	sCLK	Serial Clock			
24	O	TRSPT	TCON-Row Driver Starting Pulse(Top Start)			
	O	sHS	Serial HSYNC			
26	O	TCSPL	TCON-Column Driver Start Pulse (Left to right scan)			
	O	sD0	Serial Data Output bit (LSB)			
27	O	TROE	TCON-Row Driver Output Enable			
	O	sD1	Serial Data Output bit			
28	O	TRSPB	TCON-Row Driver Starting Pulse (Bottom Start)			
	O	sD2	Serial Data Output bit			
29	O	TCSPR	TCON-Column Driver Start Pulse (Right to left scan)			
	O	sD3	Serial Data Output bit			
30	O	TCLP	TCON-Column Driver Load Pulse			
	O	sD4	Serial Data Output bit			
31	O	TRUDL	TCON-Up Down selection			
	O	sD5	Serial Data Output bit			
32	O	TRCLK	TCON-Row Driver Shift Clock			
	O	sD6	Serial Data Output bit			
33	O	TCLRL	TCON-Left Right election			
	O	sD7	Serial Data Output bit (MSB)			
37	O	PWM1	PWM Control 1	-*	Open/Unconnected	-
38	O	LEDP	LED Control Pulse			
39	O	DCDCP	DCDC Pulse			
	O	sVS	Serial VSYNC			
Digital Power						
25	P	VDD33	Digital I/O Power +3.3V	-	-	Pwr
36	P	VSS33	Digital I/O Ground			

12,34	P	VDD18	Digital Core Power +1.8V			
11,35	P	VSS18	Digital Core Ground			

1: Pull-up Resistor 38K(min), 54K(typ), 83K(max)ohm

2: Pull-down Resistor 35K(min), 57K(typ), 107K(max)ohm

3: "-" means N/A

4: "_*" means register controllable after reset

Parametric Information

AC/DC Electrical Parameters

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
V_{DDA5} *(measured to V_{SSA} *) 5V	VDDA5M	-	-	5.25	V
V_{DDA33} *(measured to V_{SSA} *) 3.3V	VDDA33M	-	-	3.6	V
V_{DDA18}* (measured to V_{SSA18}*) 1.8V	VDDAM	-	-	1.92	V
V_{DD18}*(measured to V_{SS18}*) 1.8V	VDD18M	-	-	1.98	V
V_{DD33} (measured to V_{SS33}) 3.3V	VDD33M	-	-	3.6	V
Voltage on any digital signal pin (See the note below)	-	V_{SS33} – 0.5	-	5.5	V
Analog Input Voltage (supplied by 1.8V)	-	V_{SSA18} – 0.5	-	1.92	V
Analog Input Voltage (suppied by 3.3V)	-	V_{SSA} -0.5		3.6	V
Analog Input Voltage (suppied by 5V)	-	V_{SSA} -0.5		3.6	V
Storage Temperature	T S	–65	-	+150	°C
Junction Temperature	T J	-	-	+125	°C
Reflow Soldering	Tpeak	255 +5/-0 (10~30 seconds)			°C

Note * :
V_{DDA5} : AVDDA5
V_{DDA33} : AVDDA
V_{SSA} : AVSDA
V_{DDA18}: AVDAD, AVDPLL
V_{SSA18}: AVSAD, AVSPLL
V_{DD33}: VDD33
V_{SS33}VSS33
V_{DD18}: VDD18
V_{SS18}: VSS18

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 4 can induce destructive latch-up.

Table 5. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO 3.3V	V_{DD33}	3.15	3.3	3.6	V
Power Supply — Digital Core 1.8V	V_{DD18}	1.62	1.8	1.98	V
Power Supply — Analog 5V	V_{DDA5}	-	-	5.25	V
Power Supply — Analog 3.3V	V_{DDA33}	3.15	3.3	3.6	V
Power Supply — Analog 1.8V	V_{DDA18}	1.62	1.8	1.92	V
Ambient Operating Temperature	T_A	-40		+85	°C
Analog Supply current 5V	Iaa5	-	11.5	-	mA
Analog Supply current 3.3V	Iaa33	-	4.8	-	mA
Analog Supply current 1.8V (CVBS)	Iaa18	-	25.1	-	mA
Digital I/O Supply current 3.3V*	Idd33	-	8.9	-	mA
Digital Core Supply Current*	Idd18	-	41.3	-	mA
* Note : Digital I/O and core power supply current measurement is base on WQVGA output (10MHz clock rate) with SMPTE pattern.					

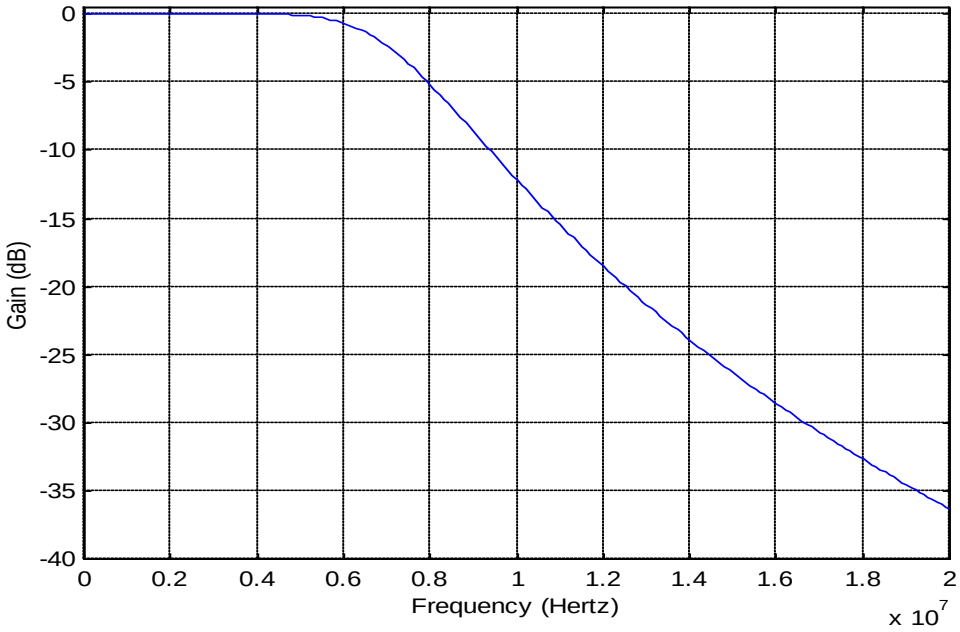
Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD33} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	μA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	μA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	V_{DD33}	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF

Parameter	Symbol	Min	Typ	Max	Units
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
YIN0, YIN1 and YIN2 Input Range (AC coupling required)		0.5	1.0	2.0	Vpp
CIN0 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
VIN0 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	9	-	Bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	27	60	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz

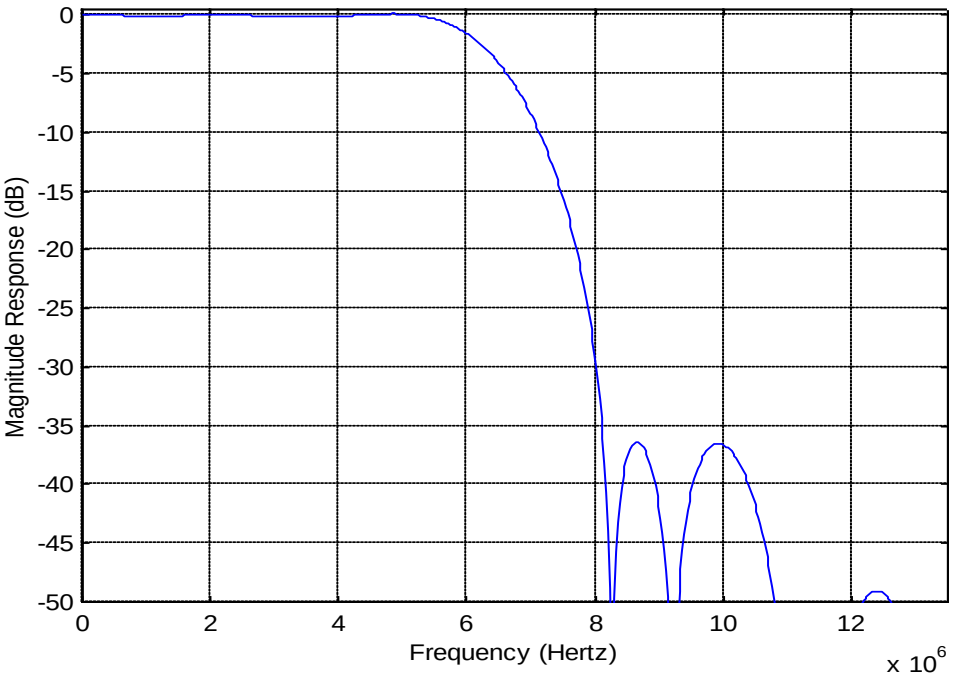
Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
Subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
Deviation		-	-	±50	ppm
Load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
*Note : Crystal Deviation crossover normal operation temperature range					

Filter Curves

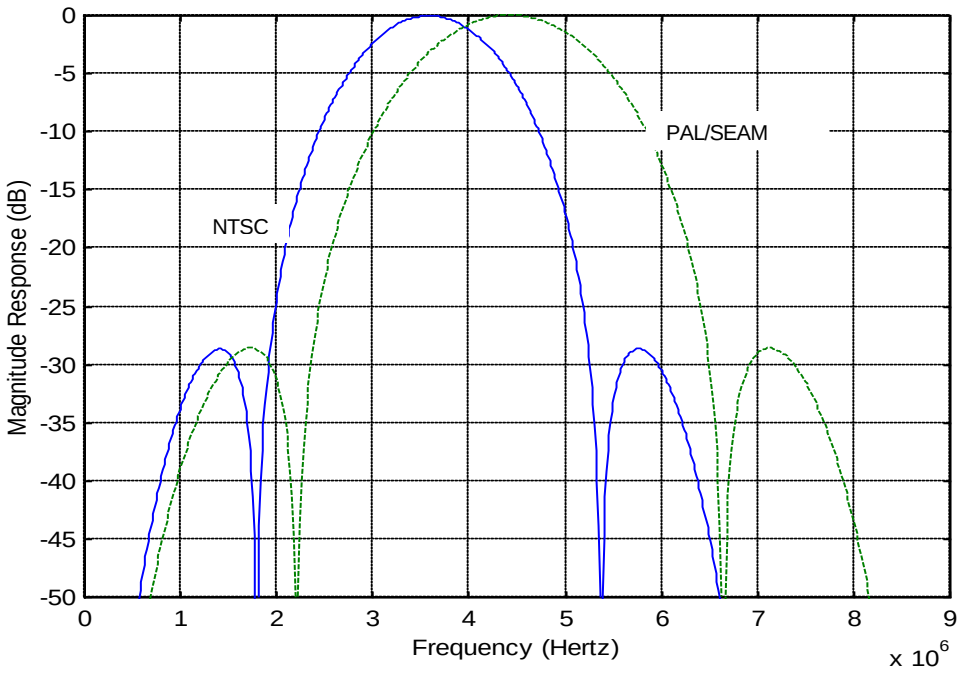
Anti-alias filter



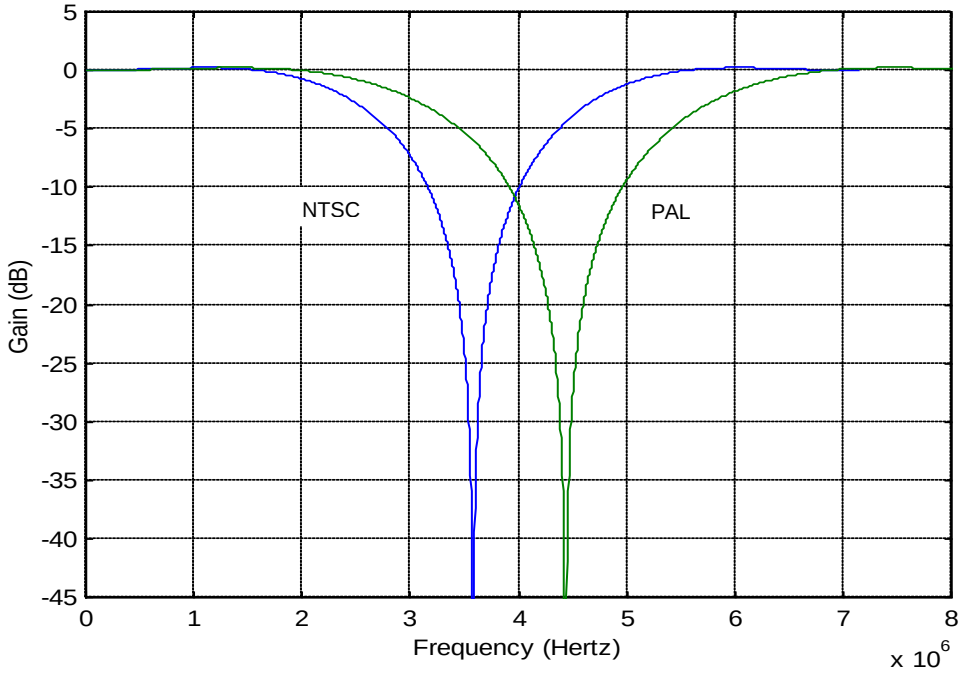
Decimation filter



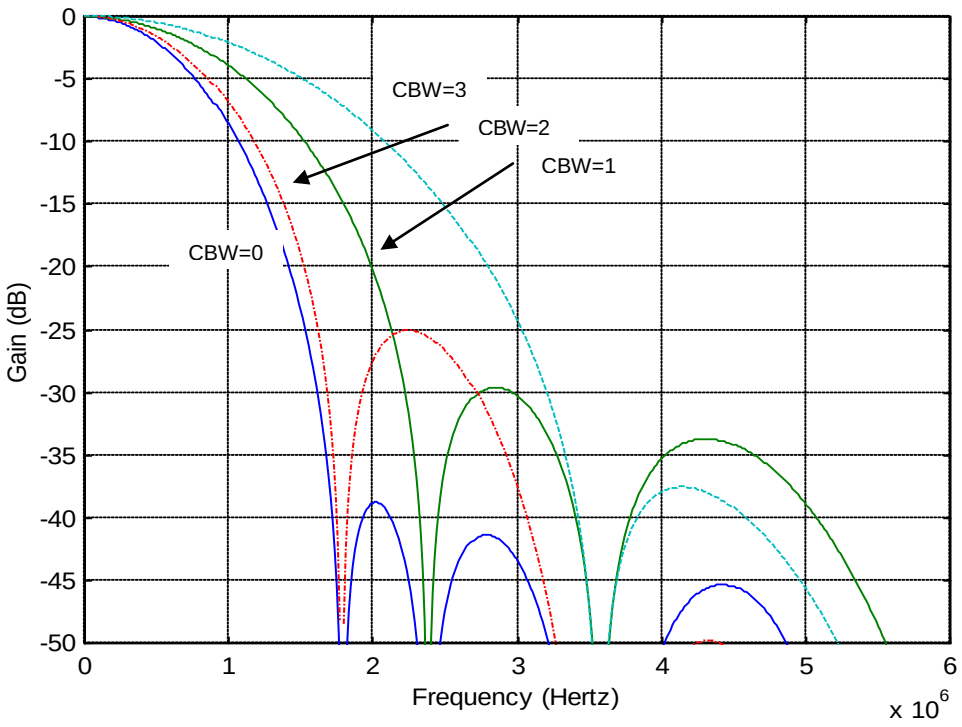
Chroma Band Pass Filter Curves



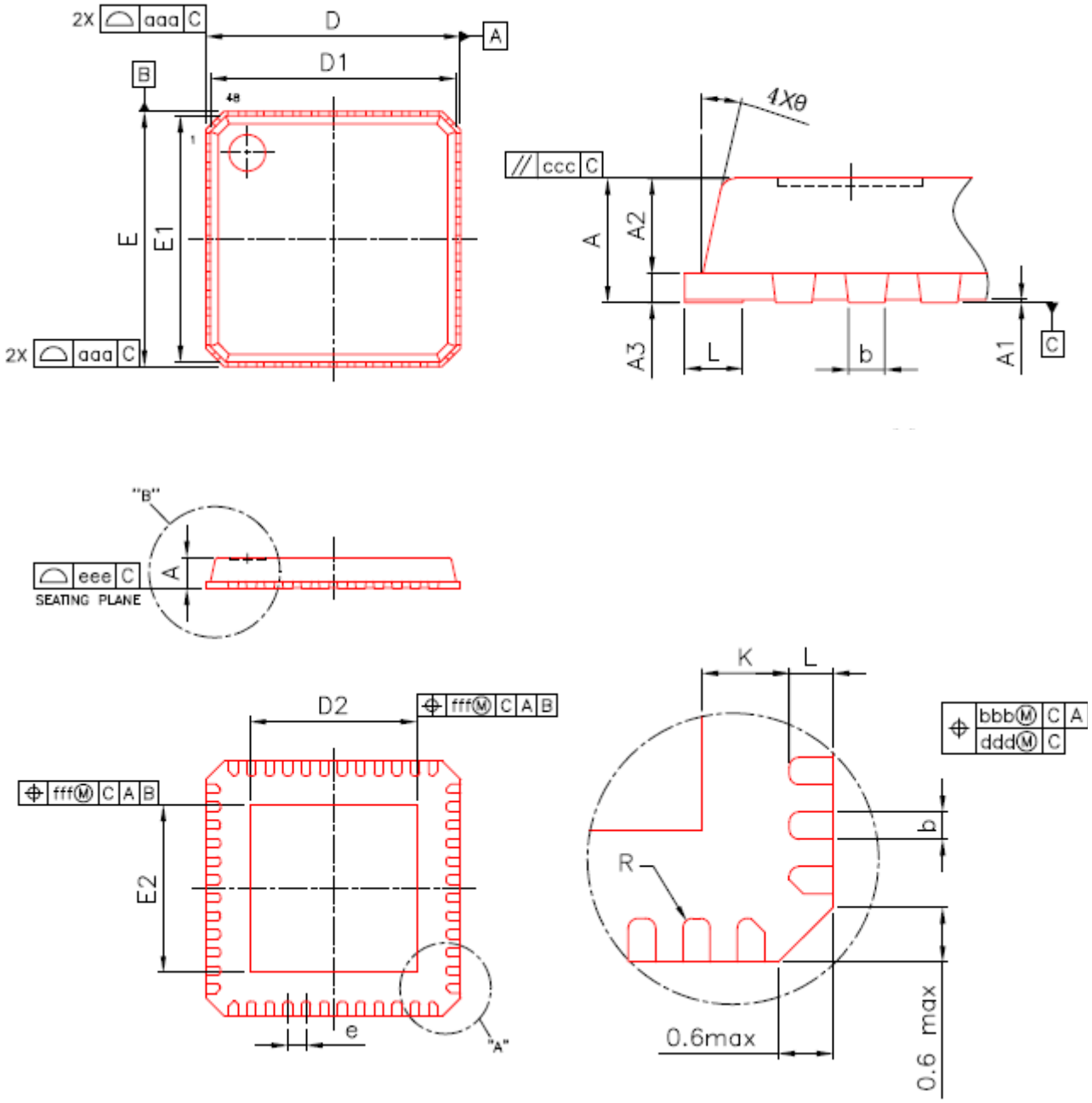
Luma Notch Filter Curve for NTSC and PAL



Chrominance Low-Pass Filter Curve



Mechanical Data 48 QFN



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.2 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	6.90	7.00	7.10	0.272	0.276	0.280
D1/E1	6.75 BSC.			0.266 BSC.		
D2/E2	4.45	4.60	4.75	0.175	0.181	0.187
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 BSC.			0.020 BSC.		
θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

* CONTROLLING DIMENSION : MM

NOTES:

1. All dimensions are in millimeters.

Register Summary

The registers are organized in functional groups in this Register Summary. A register containing different functional bits may appear more than once in different functional groups. If a particular bit of a register is not related to that functional group, it is printed in smaller font than those related. For example, bit 7 of index 006 is classified as "General" and is printed in normal size; the other bits in this register are printed in smaller size for their functionality is not classified as "General".

"-": for Register it means "Reserved", for Reset Value it means "unknown"

General

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
000	ID					REV			30h
XFF	-				PAGE				00h

General

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
002	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	21h
003	IMASK								FFh
006	SRST	-	AINC	TCKDIV	TRUDL	TCLRL	TRSP	TCSP	00h
007	-					TCONSEL			00h
008	TCKDRV		-	TRI_EN	GPO_SEL				30h
009	GPOEN2	-	GPO5	-		GPO2	GPO1	GPO0	00h
01F	TEST								00h

LEDC/DC-DC/VCOM Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DB	-	FPCLK_DELAY			FPWM2[9-8]		FPWM1[9-8]		05h
0DC	FPWM1[7-0]								00h
0DD	DPWM1								80h
0DE	FPWM2[7-0]								00h
0DF	DPWM2								80h
0E0	L_OVEN	L_OIEN	L_UIEN	L_FBEN	-		LEDA_PD	LEDC_EN	F2h
0E1	LEDA_FB				LEDA_VOP				77h
0E2	-		LEDC_ST		LEDC_LSTP				04h
0E3	LEDC_FPWM								40h
0E4	LEDC_FDIM								84h
0E5	DMODE	LEDC_DDIM							00h
0E6	LEDC_PWMTOP								20h
0E8	D_OVEN	D_OIEN	D_UIEN	D_FBEN	-		LEDA_PD	DC_EN	F2h
0E9	-				DC_FB		DC_VOP		0Ah
0EA	-		DC_ST		DC_LSTP				04h
0EB	DC_FPWM								40h
0EC	DC_PWMTOP								20h
0ED	VCOM_OFFSET								80h
0EE	-	IREF	VCOM_AMP						20h

DAC

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F0	DAC_PD	DAC_VCM			DACGAIN				C8h
0F1	-				DAC_CKINV	DAC_CKDLY	DACTOG	DACINV	02h

SSPLL

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F6	SPICLK_DIV				PCLK_DIV				00
0F7	-	EDGE_SEL_P	CP_X4_SSPLL_P		LP_X4_SSPLL_P		LP_X8_SSPLL_P		16h
0F8	-				FPLL[19:16]				01h
0F9	FPLL[15:8]								20h
0FA	FPLL[7:0]								00h
0FB	FSS[7:0]								40h
0FC	PD_SSPLL	SSD			SSG				30h
0FD	POST		VCO		-	IPMP			11h

Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
101	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	-
102	-	FC27	IFSEL		YSEL		CSEL0	VSEL	40h
103	-								-
104	-	CKHY		-					00h
105	-		SAVE	-	FBPY	FBPC	FBPV	DEC_SEL	00h
106	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	V_PDN	00h
107	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		12h
108	VDELAY_LO								12h
109	VACTIVE_LO								20h
10A	HDELAY_LO								0Ah
10B	HACTIVE_LO								D0h
10C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CCh
10D	-		WSSEN	CCODDLINE					00h
110	BRIGHTNESS								00h
111	CONTRAST								5Ch
112	SCURVE	VSF	CTI		SHARPNESS				11h
113	SAT_U								80h
114	SAT_V								80h
115	HUE								00h
117	SHCOR				-	VSHP			80h
118	CTCOR		CCOR		VCOR		CIF		44h
11A	-	EDS_EN	CC_EN	PARITY	FF_OVF	FF_EMP	CC_EDS	LO_HI	10h
11B	CC_DATA								-
11C	DTSTUS	STDNOW			ATREG	STANDARD			27h
11D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSCM	7Fh
11E	-	CVSTD			CVFMT				00h
11F	TEST								00h
120	CLPEND				CLPST				50h
121	NMGAIN				WPGAIN			AGCGAIN8	22h
122	AGCGAIN								F0h
123	PEAKWT								D8h
124	CLMPLD	CLMPL							BCh
125	SYNCTD	SYNCT							B8h
126	MISSCNT				HSWIN				44h
127	PCLAMP								38h
128	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00h
129	BSHT		VSHT						00h
12A	CKILLMAX		CKILLMIN						78h
12B	FCOMB	HTL			VTL1	VTL			44h
12C	CKLM	YDLY			HFLT				30h
12D	HPLC	EVCNT	PALC	SDET	TBC_EN	BYPASS	SYOUT	HADV	14h

12E	HPM		ACCT		SPM		CBW		**A5h**
12F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	**E0h**
130	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	**-**
131	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	**-**
132	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								**-**
133	FRM		YNR		CLMD		PSP		**05h**
134	INDEX		NSEN/SSEN/PSEN/WKTH						**1Ah**
135	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	**00h**
140	-		WSS0						**-**
141	CRCERR	WSSFLD	WSS1						**-**
142	WSS2								**-**

SCALER / TCON

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
201	MIRROR	PWEN	PXDBL	LNDBL	LNEXT	LNFIX	VALOCK	SMODE	00h
202	-		FOFFSET						20h
203	XSCALE[7-0]								00h
204	XSCALE[15-8]								20h
205	YSCALE[7-0]								00h
206	YSCALE[15:8]								20h
207	PXSCALE[11-4]								80h
208	PXINC[7-0]								10h
209	HDSCALE[7-0]								00h
20A	-	VANOM	CEVEN	HFT	HDSCALE[11-8]				01h
20B	HDELAY2								30h
20C	HACTIVE[7-0]								D0h
20D	HACTIVE2[9-8]		CKOSEL	CKP	VSP	HSP	CKDIV		80h
20E	-		LNTT[9-8]		HPADJ[11-8]				00h
20F	HPADJ[7-0]								00h
210	HAPOS								10h
211	HALEN[7-0]								00h
212	PXSCALE[3-0]				HALEN[11-8]				03h
213	HSPOS								10h
214	PXINC[11-8]				HSLEN				20h
215	VAPOS								20h
216	VALEN[7-0]								00h
217	PXINC[11-8]				VALEN{11-8]				03h
218	VSLEN		VSPOS						00h
219	LNTT[7-0]								00h
21A	DM_TOP								00h
21B	DM_BOT								00h
240	CSP_WID				CSP_POS				10h
241	CLP_POS								00h
242	CLP_WID								01h
243	-	RCK_POS[10-8]			-	RCK_WID[10-8]			00h
244	RCK_POS[7-0]								00h
245	RCK_WID[7-0]								01h
246	ROE_EXT		ROE_POS[10-8]		-	ROE_WID[10-8]			00h
247	ROE_POS[7-0]								00h
248	ROE_WID[7-0]								01h
249	-		RSP_WID			RSP_POS[10-8]			10h
24A	RSP_POS[7-0]								00h
24B	-	CPL_POS[10-8]			CLP_EXT				00h
24C	CPL_POS[7-0]								10h
24D	ROE_MOD		CPL_POL	RSP_POL	ROE_POL	RCK_POL	CLP_POL	CSP_POL	80h
24E	CPL_REF	CPL_SWP	CPL_TGM		ROE_DE	CLP_REF	CLP_DE	CSP_DE	00h

Image Adjustment

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
280	-		HUE						20h
281	CONTRAST_R								80h
282	CONTRAST_G								80h
283	CONTRAST_B								80h
284	CONTRAST_Y								80h
285	CONTRAST_Cb								80h
286	CONTRAST_Cr								80h
287	BRIGHTNESS_R								80h
288	BRIGHTNESS_G								80h
289	BRIGHTNESS_B								80h
28A	BRIGHTNESS_Y								80h
28B	H_SHARP_COR				H_SHARPNESS				30h
28C	SH_FREQ	-							00h
2B0	-		PEDLVL	WHTLVL	-			BW_EN	10h
2B1	BW_FMIN								40h
2B2	BW_FMAX								40h
2B6	BW_BLACK_TILT								67h
2B7	BW_WHITE_TILT								94h
2BF	TPG_EN	SWAP			PAT_SEL				00h

Gamma & Dither

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
2E0	GAMAE_R	GAMAE_G	GAMAE_B	-	AUTO_INC		GAMMA_RGB_INDX		00h
2E1	GAMMA_RAM_STARTING_ADDR								00h
2E2	-						GAMMA_RAM_DATA[9:8]		00h
2E3	GAMMA_RAM_DATA[7:0]								00h
2E4	-	DITHER_OPTION			-	DITHER_FORMAT			00h
2F0	RDPOS_X[7:0]								00h
2F1	RDPOS_Y[7:0]								00h
2F2	-	RDPOS_Y[10:8]			RDPOS_X[11:8]				00h
2F3	RDVALUE_R								-
2F4	RDVALUE_G								-
2F5	RDVALUE_B								-
2F8	DELTA_EN	RGB_ORDR	AVRG_EN	AVRG_POL	COL_ODD		COL_EVEN		00h
2F9	DELTA_TYPE	-					DMMY_EN	DMMY_POS	80h

FOSD

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
300	-					MIREN	FONT_SWITCH	OSD_SWITCH	00h
301	-							STATUS	-
302	-		DBGWIN		DBG				06h
303	OSD DE Delay								06h
304	BLINK	ITALIC	ULINE	BSEN	AUTO		CLEAR	FR_RAC_SEL	00h
305	-		FBITEXT	RD_SEL	-			I2COSDRAD	00h
306	I2COSDRAD								00h
307	FDATA								00h
308	FATTRIBUTE								00h
309	I2CFONTRAD								00h
30A	I2CFONTDAT								00h
30B	MADD								31h
30C	-			OSDON	TABLE_WSEL				00h
30D	TABLE_CON_H								00h
30E	TABLE_CON_L								00h
310	WIN1EN	WIN1MCOLOR	WIN1CVEXT	-	XWIN1ZOOM		YWIN1ZOOM		00h
311	WIN1ASEL				WIN1ALPHA				00h
312	-	WIN1HSTR			-		WIN1VSTR		00h
313	WIN1HSTR								00h
314	WIN1VSTR								00h
315	-		WIN1HEIGHT						00h
316	-		WIN1WIDTH						00h
317	-			WIN1REGSTA	WIN1BC				00h
318	WIN1BCEN	-		WIN1BCWID					00h
319	-	WIN1HBWID							00h
31A	-	WIN1VBWID							00h
31B	WIN1BEN	WIN1TEN	WIN1EFF	WIN1BSEL	WIN1SC				00h
31C	WIN1SCEN	WIN1CHSPC	WIN1CVSPC	WIN1SCWID					00h
31D	WIN1CHSPC				WIN1CVSPC				00h
31E	WIN1BGC				WIN1BSC				00h
31F	WIN1REGSTA								00h
320	WIN2EN	WIN2MCOLOR	WIN2CVEXT		XWIN2ZOOM		YWIN2ZOOM		00h
321	WIN2ASEL				WIN2ALPHA				00h
322	-	WIN2HSTR			-		WIN2VSTR		00h
323	WIN2HSTR								00h
324	WIN2VSTR								00h

325	-			WIN2HEIGHT			**00h**
326	-			WIN2WIDTH			**00h**
327	-			WIN2REGSTA	WIN2BC		**00h**
328	WIN2BCEN	-		WIN2BCWID			**00h**
329	-	WIN2HBWID					**00h**
32A	-	WIN2VBWID					**00h**
32B	WIN2BEN	WIN2TEN	WIN2EFF	WIN2BSEL	WIN2SC		**00h**
32C	WIN2SCEN	WIN2CHSPC	WIN2CVSPC	WIN2SCWID			**00h**
32D	WIN2CHSPC			WIN2CVSPC			**00h**
32E	WIN2BGC			WIN2BSC			**00h**
32F	WIN2REGSTA						**00h**
330	WIN3EN	WIN3MCOLOR	WIN3CVEXT	-	XWIN3ZOOM	YWIN3ZOOM	**00h**
331	WIN3ASEL			WIN3ALPHA			**00h**
332	-	WIN3HSTR		-	WIN3VSTR		**00h**
333	WIN3HSTR						**00h**
334	WIN3VSTR						**00h**
335	-			WIN3HEIGHT			**00h**
336	-			WIN3WIDTH			**00h**
337	-			WIN3REGSTA	WIN3BC		**00h**
338	WIN3BCEN	-		WIN3BCWID			**00h**
339	-	WIN3HBWID					**00h**
33A	-	WIN3VBWID					**00h**
33B	WIN3BEN	WIN3TEN	WIN3EFF	WIN3BSEL	WIN3SC		**00h**
33C	WIN3SCEN	WIN3CHSPC	WIN3CVSPC	WIN3SCWID			**00h**
33D	WIN3CHSPC			WIN3CVSPC			**00h**
33E	WIN3BGC			WIN3BSC			**00h**
33F	WIN3REGSTA						**00h**
340	WIN4EN	WIN4MCOLOR	WIN4CVEXT	-	XWIN4ZOOM	YWIN4ZOOM	**00h**
341	WIN4ASEL			WIN4ALPHA			**00h**
342	-	WIN4HSTR		-	WIN4VSTR		**00h**
343	WIN4HSTR						**00h**
344	WIN4VSTR						**00h**
345	-			WIN4HEIGHT			**00h**
346	-			WIN4WIDTH			**00h**
347	-			WIN4REGSTA	WIN4BC		**00h**
348	WIN4BCEN	-		WIN4BCWID			**00h**
349	-	WIN4HBWID					**00h**
34A	-	WIN4VBWID					**00h**

34B	WIN4BEN	WIN4TEN	WIN4EFF	WIN4BSEL	WIN4SC	**00h**
34C	WIN4SCEN	WIN4CHSPC	WIN4CVSPC	WIN4SCWID		**00h**
34D	WIN4CHSPC			WIN4CVSPC		**00h**
34E	WIN4BGC			WIN4BSC		**00h**
34F	WIN4REGSTA					**00h**

SPI OSD (for TW8833S only)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
400	BLTSEL		-				MIXODR	OSDRST	**00h**
40F	TIMADJ								**45h**
410	LUTWE	LUTINC_SEL		-			LUT_BYT		**00h**
411	LUTADDR								**00h**
412	LUTDATA								**00h**
420	WIN0LPE		WIN0_PERPIX	WIN0_ALPHA_ENA	-			WIN0_ENA	**00h**
421	-					WIN0_HS_HB			**00h**
422	WIN0_HS_LB								**00h**
423	-					WIN0_VS_HB			**00h**
424	WIN0_VS_LB								**00h**
425	-				WIN0_HL_HB				**00h**
426	WIN0_HL_LB								**00h**
427	-				WIN0_VL_HB				**00h**
428	WIN0_VL_LB								**00h**
429	BFM0_AST_HB								**00h**
42A	BFM0_AST_MB								**00h**
42B	BFM0_AST_LB								**00h**
42C	-				BFM0_HL_HB				**00h**
42D	BFM0_HL_LB								**00h**
42E	-				BFM0_VL_HB				**00h**
42F	BFM0_VL_LB								**00h**
430	-					WFM0_HS_HB			**00h**
431	WFM0_HS_LB								**00h**
432	-					WFM0_VS_HB			**00h**
433	WFM0_VS_LB								**00h**
434	-	WIN0_ALPHA							**00h**
435	WIN0_LPHNUM								**00h**
436	WIN0_LPVNUM								**00h**
437	WIN0_FD								**00h**
440	WIN1LPE		WIN1_PERPIX	WIN1_ALPHA_ENA	-			WIN1_ENA	**00h**
441	-					WIN1_HS_HB			**00h**
442	WIN1_HS_LB								**00h**
443	-					WIN1_VS_HB			**00h**
444	WIN1_VS_LB								**00h**

445	-	WIN1_HL_HB	**00h**
446	WIN1_HL_LB		**00h**
447	-	WIN1_VL_HB	**00h**
448	WIN1_VL_LB		**00h**
449	BFM1_AST_HB		**00h**
44A	BFM1_AST_MB		**00h**
44B	BFM1_AST_LB		**00h**
44C	-	BFM1_HL_HB	**00h**
44D	BFM1_HL_LB		**00h**
44E	-	BFM1_VL_HB	**00h**
44F	BFM1_VL_LB		**00h**
450	-	WFM1_HS_HB	**00h**
451	WFM1_HS_LB		**00h**
452	-	WFM1_VS_HB	**00h**
453	WFM1_VS_LB		**00h**
454	-	WIN1_ALPHA	**00h**
455	WIN1_LPHNUM		**00h**
456	WIN1_LPVNUM		**00h**
457	WIN1_FD		**00h**

SPI Interface

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
480	-	HOST SPI_MODE			-	OSD SPI_MODE			00h
481	-		EDGE_SEL	CYCLE_EN	-			DMA_NONV	00h
483	DMA_SEL		DMA_REG_MODE		WR_CNT_NUM				40h
484	-					BUSY_CHECK	WR_MODE	DMA_STR	00h
485	DMA_WAIT				SPI_WAIT				80h
486	DMA_REG_PAGE								04h
487	INDEX								90h
488	DMA_LENGTH[15:8]								00h
489	DMA_LENGTH[7:0]								00h
48A	WR_REG1_RG								00h
48B	WR_REG2_RG								00h
48C	WR_REG3_RG								00h
48D	WR_REG4_RG								00h
48E	WR_REG5_RG								00h
490	BUF1								00h
491	BUF2								00h
492	BUF3								00h
493	BUF4								00h
494	BUF5								00h
495	BUF6								00h
496	BUF7								00h
497	BUF8								00h
498	STATUS_CMD_RG								05h
499	-				BUSY_POL	BUSY_BIT			08h
49A	DMA_LENGTH[23:16]								00h

Register Description

0x000 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	TW8833 Product ID code	06
2-0	Revision	R	Revision number	0

0x002 – IRQ

Bit	Function	R/W	Description	Reset
7	INT7	R/W	Reserved	-
6	INT6	R/W	Reserved	-
5	INT5	R/W	Vertical display end interrupt.	1
4	INT4	R/W	SPI-DMA completion interrupt. Reset when written.	0
3	INT3	R/W	End of Font OSD display interrupt. Reset when written	0
2	INT2	R/W	End of SPI-DMA window interrupt	0
1	INT1	R/W	Video detection interrupt. The detection corresponds to the Input selection.	0
0	INT0	R/W	Video loss interrupt. The source selection corresponds to the IPSEL register.	1

0x003 – IMASK

Bit	Function	R/W	Description	Reset
7-0	IMASK	R/W	Interrupt mask for IRQ status register. An “1” for any bit masks the interrupt for that specific bit.	FF

0x006 – SRST

Bit	Function	R/W	Description	Reset
7	SRST	W	Chip soft reset by writing “1” to this bit. No register will be affected by this action. It is a self-resetting bit.	0
6	Reserved	R/W	Reserved	-
5	AINC	R/W	2-wire host interface auto index increment control 1 = disable 0 = enable	0
4	TCKDIV	R/W	TCCLK divider control 1 = ½ 0 = 1	0
3	TRUDL	R/W	TRUDL pin control. . 1 = high 0 = low	0
2	TCLRL	R/W	TCLRL pin control. 1 = high 0 = low	0
1	TRSP	R/W	TRSP output direction. 1 = TRSPT 0 = TRSPB	0
0	TCSP	R/W	TCSP output direction. 1 = TCSPL 0 = TCSPR	0

0x007 – OUTPUT CTRL I

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	TCONSEL	R/W	TCON pin output mode control 0 = TCON 1 = Serial RGB 2 = N/A 3 = Y-ADC data 4 = C-ADC data 5 = V-ADC data 6 = test 7 = N/A	0

0x008 – OUTPUT CTRL II

Bit	Function	R/W	Description	Reset
7-6	TCKDRV	R/W	TCCLK drive strength 0 = disable 1 = 4mA 2 =8mA 3 = 12mA	0
5	Reserved	R/W	Reserved	-
4	TRI_EN	R/W	1 = Tristate all output pins	1
3-0	GPOSEL	R/W	GPO pin output control 0 = Negtive IRQ controlled by IRQ and IMASK registers 1 = Positive IRQ controlled by IRQ and IMASK registers 2 = decoder vdloss 3 = N/A 4 = N/A 5 = vact2 6 = tcpolp 7 = field 8 = decoder field rate (hz50) 9 = sDE (serial RGB DE) A = pwm2 output B = 0 C = 1, it needs to set 0x0302[5-4] = 0 and 0x302[3-0] = F. D,E,F = N/A	0

0x009 – GPO Control

Bit	Function	R/W	Description	Reset
7	GPOEN2	R/W	SPICS, SPI-D1, SPI-D0, SPICLK output control 1 = Enable GPO function 0 = Normal SPI function	0
6	Reserved	R/W	Reserved	-
5	GPO5	R/W	GPO5 (SPICS) output control when enabled	0
4-3	Reserved	R/W	Reserved	-
2	GPO2	R/W	GPO2 (SPI-D1) output control when enabled	0
1	GPO1	R/W	GPO1 (SPI-D0) output control when enabled	0
0	GPO0	R/W	GPO0 (SPICLK) output control when enabled	0

0x01F – TEST

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	4 = dtest1 6 = dactest1 7 = dactest2 9 = cctest B = clamp test	00

0x0DB – FPWM_HI

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	FPCLK_DELAY	R/W	Clock delay selection of FPCLK 000 = Normal Clock Path Select 001 = 1 ns delay Clock Path Select 010 = 2 ns delay Clock Path Select 011 = 3 ns delay Clock Path Select 100 = Normal Clock Path Select with polarity inversion 101 = 1 ns delay Clock Path Select with polarity inversion 110 = 2 ns delay Clock Path Select with polarity inversion 111 = 3 ns delay Clock Path Select with polarity inversion	0
3-2	FPWM2[9-8]	R/W	PWM2 frequency control MSB. A 10-bit register.	1
1-0	FPWM1[9-8]	R/W	PWM1 frequency control MSB. A 10-bit register.	1

0x0DC – FPWM1_LO

Bit	Function	R/W	Description	Reset
7-0	FPWM1[7-0]	R/W	PWM1 frequency control LSB. A 10-bit register. Freq = 27MHz / 256 / FPWM1	80

0x0DD – DPWM1

Bit	Function	R/W	Description	Reset
7-0	DPWM1	R/W	PWM1 Duty cycle control. Duty = (DPWM1 / 256) %	0

0x0DE – FPWM2_LO

Bit	Function	R/W	Description	Reset
7-0	FPWM2[7-0]	R/W	PWM2 frequency control LSB. A 10-bit register. Freq = 27MHz / 256 / FPWM2	80

0x0DF – DPWM2

Bit	Function	R/W	Description	Reset
7-0	DPWM2	R/W	PWM2 Duty cycle control. Duty = (DPWM2 / 256) %	80

0x0E0 – LEDC Control I

Bit	Function	R/W	Description	Reset
7	LED_OVEN	R/W	Over voltage feedback control 0 = disable 1 = enable	1
6	LED_OIEN	R/W	Over current feedback control 0 = disable 1 = enable	1
5	LED_UIEN	R/W	Protection control 0 = disable 1 = enable	1
4	LED_FBEN	R/W	LEDC feedback loop control 0 = open loop 1 = close loop	1
3-2	Reserved	R/W	Reserved	-
1	LEDA_PD	R/W	LEDC Analog block power down. 0 = Analog block power up. 1 = Analog block power down.	1
0	LEDC_EN	R/W	LEDC digital block enable control 0 = LEDC digital block disable. 1 = LEDC digital block enable.	0

0x0E1 – LEDC Sense Control

Bit	Function	R/W	Description	Reset
7-4	VFB	R/W	Lamp voltage threshold from 0.25V to 2.05V in 0.12V per step. 00 = 0.25V … FF = 2.05V	0
3-0	VOP	R/W	Over voltage threshold control. Factory use only.	A

0x0E2 – LEDC Control II

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	LEDC_ST	R	LEDC status	-
3-0	LSTP	R/W	LEDC feedback gain control with “1h” being the smallest gain.	4

0x0E3 – LEDC PWM

Bit	Function	R/W	Description	Reset
7-0	LEDC_FPWM	R/W	LEDC PWM control frequency FPWM[6:0] : LED PWM (13.5MHz / Fpwm)	40

0x0E4 – LEDC Dim Frequency

Bit	Function	R/W	Description	Reset
7-0	LEDC_FDIM	R/W	LEDC dimming frequency control. 13.18KHz / Fdim	84

0x0E5 – LEDC Dim Control

Bit	Function	R/W	Description	Reset
7	DMODE	R/W	0 = LEDC digital output disable 1 = LEDC digital output enable	0
6-0	LEDC_DDIM	R/W	LED dimming control 0 = Full brightness 7F = Lowest brightness	00

0x0E6 – LEDC PWMTOP

Bit	Function	R/W	Description	Reset
7-0	PWMTOP	R/W	Factory use only	20

0x0E8 – DCDC Control I

Bit	Function	R/W	Description	Reset
7	DC_OVEN	R/W	Over voltage feedback control 0 = disable 1 = enable	1
6	DC_OIEN	R/W	Over current feedback control 0 = disable 1 = enable	1
5	DC_UIEN	R/W	Under current feedback control 0 = disable 1 = enable	1
4	DC_FBEN	R/W	LED feedback loop control 0 = open loop 1 = close loop	1
3-2	Reserved	R/W	Reserved	0
1	DCA_PD	R/W	DC sense block power down. 0 = Sense block power up. 1 = Sense block power down.	1
0	DC_EN	R/W	DC digital block enable control 0 = DC converter digital block disable. 1 = DC converter digital block enable.	0

0x0E9 – DCDC Sense Control

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-2	DC_FB	R/W	FB sense threshold control 0 =1.48V 1 = 1.38V 2 = 1.28V 3= 1.18V	2
1-0	VOP	R/W	Reserved	2

0x0EA – DCDC Control II

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	DC_ST	R	DCDC status	-
3-0	DC_LSTP	R/W	DCDC feedback gain control with “1h” being the smallest gain.	4

0x0EB – DCDC PWM

Bit	Function	R/W	Description	Reset
7-0	DC_FPWM	R/W	DCDC PWM control frequency FPWM[7:0] : LED PWM (13.5MHz / Fpwm)	40

0x0EC – DCDC PWMTOP

Bit	Function	R/W	Description	Reset
7-0	DC_PWMTOP	R/W	Factory use only	20

0x0ED – VCOM-DC OFFSET Control

Bit	Function	R/W	Description	Reset
7-0	VC-OFFSET	R/W	VCOM DC output offset control from 0.67V to 2.64V	80

0x0EE – VCOM-AC AMP Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	VCOM_IREF	R/W	VCOM IREF control. Factory use only.	1
5-0	VCOM_AMP	R/W	VCOM-AC amplitude control from 0 to 3.3V	00

0x0F0 – DAC I

Bit	Function	R/W	Description	Reset
7	DAC_PD	R/W	1 = DAC power down	1
6-4	DAC_VCM	R/W	Output common mode selection	4
3-0	DAC_GAIN	R/W	DAC Channel Gain	8

0x0F1 – DAC II

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3	DAC_CKINV	R/W	DAC clock polarity control	0
2	DAC_CKDLY	R/W	DAC clock delay control	0
1	DACTOG	R/W	DAC output toggle control. 1 = toggling 0 = no toggling	1
0	DACINV	R/W	DAC output inversion 1 = inversion 0 = normal	0

0x0F6 – CLOCK_DIV

Bit	Function	R/W	Description	Reset
7-4	SPICLK_DIV	R/W	These bits control the SPI clock divider as follow. 0 = 1 1 = ½ 2 = 1/3 3 = 1/4	0
3-0	PCLK_DIV	R/W	These bits control the pclk divider as follow 0 = 1 1 = ½ 2 = 1/3 3 = ¼ 4 = 1/8	0

0x0F7 – SSPLL

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	EDGE_SEL_P	R/W	Edge selection for SSPLL. Factory use only	0
5-4	SSPLL_CP_X 4	R/W	SSPLL_X4 CP selection. Factory use only. 1uA / 5uA / 10uA / 15uA	1
3-2	SSPLL_LP_X4	R/W	SSPLL_X4 LP selection among 80K to 20K. Factory use only.	1
1-0	SSPLL_LP_X8	R/W	SSPLL_X8 LP selection among 18K to 0.8K. Factory use only.	2

0x0F8 – SSPLL Control Registers

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	FPLL[19-16]	R/W	Part of a 20-bit register that control the PLL center frequency as below. PLL Oscillation frequency = 108MHz * FPLL / 2 ^ 17 / 2^ POST	1

0x0F9 – SSPLL Frequency Control Registers

Bit	Function	R/W	Description	Reset
7-0	FPLL[15-8]	R/W	Part of a 20-bit register that control the PLL center frequency as below. PLL Oscillation frequency = 108MHz * FPLL / 2 ^ 17 / 2^ POST	20

0x0FA – SSPLL Frequency Control Registers

Bit	Function	R/W	Description	Reset
7-0	FPLL[7-0]	R/W	Part of a 20-bit register that control the PLL center frequency as below. PLL Oscillation frequency = 108MHz * FPLL / 2 ^ 17 / 2^ POST	00

0x0FB – SSPLL Modulation Frequency Control Registers

Bit	Function	R/W	Description	Reset
7-0	FSS[7-0]	R/W	Spread spectrum modulation frequency = 27MHz * FSS / 2^16	40

0x0FC – SSPLL

Bit	Function	R/W	Description	Reset
7	PD_SSPLL	R/W	PD_SSPLL, PLL power down control 1 = Power Down	0
6-4	SSD	R/W	Spread spectrum gain divider. See SSG description.	3
3-0	SSG	R/W	Spread Spectrum gain control. The frequency deviation is controller by a center spreading sawtooth waveform. The controlling frequency is determined by FSS and its associated equation. The percentage of peak-to-peak spread or deviation of the center frequency is determined by the following equation. DEVpp = SSG * 2^8 / (FPLL * 2^SSD) * 100 %	0

0x0FD – SSPLL Analog Control Registers

Bit	Function	R/W	Description	Reset
7-6	POST	R/W	POST, PLL post divider 0 = 1 1 = 1/2 2 = 1/4 3 = 1/8 Set PLL post divider larger than 1 is recommended	0
5-4	VCO	R/W	VCO Range control. 0 = 13.5 ~ 27MHz 2 = 54 ~ 108MHz 1 = 27 ~ 54 MHz 3 = 108 ~ 216MHz	1
3	Reserved	R/W	Reserved	-
2-0	IPMP	R/W	Charge pump currents (uA) 0 = 1.5 1 = 2.5 2 = 5 3 = 10 4 = 20 5 = 40 6 = 80 7 = 160	1

0x0FE – FPGA Debug

Bit	Function	R/W	Description	Reset
7-0	SHUE	R/W	FPGA debug use only FPGA DAC output selection	00

Decoder

0x101 – Chip Status Register (CSTATUS)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	-
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	-
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	-
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	-
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	-
2	Reserved	R	Reserved	-
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	-
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	-

0x102 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	0 = Composite video decoding 1 = S-video decoding 2 = Component video decoding (Interlace input) 3 = Component video decoding (Progressive input)	0
3-2	YSEL	R/W	These two bits control the input video selection. It selects the composite video source or Luma source. 0 = YIN0 1 = YIN1 2 = YIN2 3 = N/A	0
1	CSEL	R/W	This bit select the C channel input 0 = CVIN0 1 = N/A	0
0	VSEL	R/W	This bit select the V channel input 0 = VIN0 1 = N/A	0

0x103 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x104 – HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-5	CKHY	R/W	Color killer time constant 0 = Fastest 3 = Slowest	0
4-0	Reserved	R/W	Reserved	-

0x105 – Anti-aliasing

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	SAVE	R/W	0 = Normal ADC current. 1 = Enable ADC current saving mode.	0
4	Reserved	R/W	Reserved	-
3	FBPY	R/W	0 = Disable 1 = Enable Y channel anti-aliasing filter (decoder mode)	0
2	FBPC	R/W	0 = Disable 1 = Enable C channel anti-aliasing filter (decoder mode)	0
1	FBPV	R/W	0 = Disable 1 = Enable V channel anti-aliasing filter (decoder mode)	0
0	DEC_SEL	R/W	AFE control selection 0 = Disable 1 = Decoder input mode	0

0x106 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	A 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = 27 MHz clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	0
0	V_PDN	R/W	0 = V channel ADC in normal operation. 1 = V channel ADC in power down mode.	0

0x107 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	Bit[9:8] of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	Bit[9:8] of the 10-bit VACTIVE register. Refer to description on Reg0x09 for its shadow register.	1
3-2	HDELAY_HI	R/W	Bit[9:8] of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	Bit[9:8] of the 10-bit HACTIVE register.	2

0x108 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	Bit[7:0] of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0x109 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	Bit[7:0] of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0x10A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	Bit[7:0] of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

0x10B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	Bit[7:0] of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0x10C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	Combined with VTL[3], there are four different chroma bandwidth can be selected. 1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Color killer sensitivity 1 = Low 0 = High	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC/PAL 0 = Notch filter	1
2	HCOMP	R/W	1 = Operation mode 1. (recommended) 0 = Operation mode 0.	1
1	YCOMB	R/W	This bit controls the comb operation when there is no color burst. 1 = No comb 0 = Comb.	0
0	PDLY	R/W	PAL delay line 1 = Disable 0 = Enable	0

0x10D – CC/WSS Control

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	WSSEN	R/W	0 = Disable WSS decoding 1 = Enable	0
4-0	CCODDLINE	R/W	These bits control the Closed Caption decoding line number in case of odd field	00

0x110 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0x111 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CONTRAST	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 100 (64h) yields a gain of 100%. The gain ranges from 0 to 255%	5C

0x112 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	Color transient improvement level control. There are 4 enhancement levels with 0 being the lowest and 3 being the highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image and '15' being the strongest.	1

0x113 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x114 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x115 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue. It is in 2's complement form with 0 being the center value. Positive value results in red hue and negative value gives green hue.	00

0x116 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x117 – Vertical Peaking Control I

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8
3	Reserved	R/W	Reserved	-
2-0	VSHP	R/W	Vertical peaking gain control	0

0x118 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring function for the CTI. It has internal step size of 2.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of the vertical peaking logic. It has an internal step size of 2.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5 dB 2 = 3 dB 3 = 6 dB	0

0x119 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x11A – CC/EDS Status Register (CC_STATUS)

Bit	Function	R/W	Description	Reset
7	CCVLDEN	R/W	Reserved	-
6	EDS_EN	R/W	0 = EDS data is not transferred to the CC_DATA FIFO. 1 = EDS data is transferred to the CC_DATA FIFO.	0
5	CC_EN	R/W	0 = CC data is not transferred to the CC_DATA FIFO. 1 = CC data is transferred to the CC_DATA FIFO.	0
4	PARITY	R	0 = Data in CC_DATA has no error. 1 = Data in CC_DATA has odd parity error.	-
3	FF_OVF	R	0 = An overflow has not occurred. 1 = An overflow has occurred in the CC_DATA FIFO.	-
2	FF_EMP	R	0 = CC_DATA FIFO is empty. 1 = CC_DATA FIFO has data available.	-
1	CC_EDS	R	0 = Closed caption data is in CC_DATA register. 1 = Extended data service data is in CC_DATA register.	-
0	LO_HI	R	0 = Low byte of the 16-bit word is in the CC_DATA register. 1 = High byte of the 16-bit word is in the CC_DATA register.	-

0x11B – CC/EDS Data Register (CC_DATA)

Bit	Function	R/W	Description	Reset
7-0	CC_DATA	R	These bits store the incoming closed caption or even field closed caption data.	-

0x11C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	-
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = N/A	-
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STANDARD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x11D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x11E – Component Video Format (CVFMT)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	CVSTD	R	Component video input format detection. 0 = 480i 1 = 576i 2 = 480p 3 = 576p others = NA	-
3-0	CVFMT	R/W	Component video format selection. 0 = 480i 1 = 576i 2 = 480p 3 = 576p 8 = Auto others = N/A	0

0x11F – Test

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x120 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x121 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x122 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x123 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	D8

0x124– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0x125– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0x126 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits set the size for the horizontal sync detection window.	4

0x127 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	38

0x128 – Vertical Control I

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = Fastest 3 = Slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = Fastest 3 = Slowest.	0
3	VMODE	R/W	Vertical detection window. 0 = Vertical count down mode 1 = Search mode	0
2	DETV	R/W	0 = Normal Vsync logic 1 = recommended for special application only	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 0 = Short 1 = Normal	0

0x129 – Vertical Control II

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control.	0
4-0	VSHT	R/W	Vsync output delay control in the increment of half line length	00

0x12A – Color Killer Level Control

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

0x12B – Comb Filter Control

Bit	Function	R/W	Description	Reset
7	FCOMB	R/W	1 = Non-adaptive comb 0 = Adaptive comb.	0
6-4	HTL	R/W	Adaptive Comb filter control (factory use only).	4
3	VTL1	R/W	Comb filter bandwidth control	0
2-0	VTL	R/W	Adaptive Comb filter threshold control (factory use only)	4

0x12C – Luma Delay and HFilter Control

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by SCURVE bit.	0

0x12D – Miscellaneous Control Register I (MISC1)

Bit	Function	R/W	Description	Reset
7	HPLC	R/W	Reserved	0
6	EVCNT	R/W	0 = Normal operation 1 = Even field counter in special mode	0
5	PALC	R/W	Reserved	0
4	SDET	R/W	ID detection sensitivity. "1" is recommended.	1
3	TBC_EN	R/W	0 = TBC off 1 = Internal TBC enabled. (test purpose only)	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	0 = Hsync is always generated 1 = Hsync is disabled when video loss is detected	0
0	HADV	R/W	Reserved	0

0x12E – Miscellaneous Control Register II (MISC2)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 0 = Slow 1 = Medium 2 = Auto 3 = Fast	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = Slow 2 = Medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. 0 = Low 1 = Medium 2 = High 3 = NA	1

0x12F – Miscellaneous Control III (MISC3)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disable	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disable	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disable	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disable	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disable	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color 0 = Black	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disable	0

0x130 – Macrovision Detection

Bit	Function	R/W	Description	Reset
7	SID_FAIL	R	1 = SECAM ID detection failed	-
6	PID_FAIL	R	1 = PAL ID detection failed	-
5	FSC_FAIL	R	1 = Fsc frequency detection failed	-
4	SLOCK_FAIL	R	1 = Sub-carrier lock detection failed	-
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	-
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	-
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	-
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	-

0x131 – Chip STATUS II (CSTATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator	-
6	WKAIR	R	Weak signal indicator 2	-
5	WKAIR1	R	Weak signal indicator1	-
4	VSTD	R	Standard line per field indicator	-
3	NINTL	R	Non-interlaced signal indicator	-
2	WSSDET	R	1 = WSS data detected 0 = Not detected.	-
1	EDSDET	R	1 = EDS data detected 0 = Not detected.	-
0	CCDET	R	1 = CC data detected 0 = Not detected.	-

0x132 – H Monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF, etc.	R	Horizontal line frequency indicator HREF[9:2] / GVAL[8:1] / PHERRDO / CGAINO / BAMPO / MINAVG / SYTHRD / SYAMP	-

0x133 – CLAMP MODE(CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode. 0,1 = Auto mode 2 = 60 Hz 3 = 50 Hz	0
5-4	YNR	R/W	Y HF Noise Reduction. 0 = None 1 = Smallest 2 = Small 3 = Medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = NA	1
1-0	PSP	R/W	Slice level. 0 = Low 1 = Medium 2 = High 3 = NA	1

0x134 – ID Detection Control (NSEN/SSEN/PSEN/WKTH)

Bit	Function	R/W	Description	Reset
7-6	INDEX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A/ 20 / 1C / 2A

0x135 – Clamp Control (CLCNTL)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debug use.	0
6	YCLEN	R/W	0 = Enable Y channel clamp 1 = Disable	0
5	CCLEN	R/W	0 = Enable C channel clamp 1 = Disable	0
4	VCLEN	R/W	0 = Enable V channel clamp 1 = Disable	0
3	GTEST	R/W	0 = Normal operation 1 = Test	0
2	VLPF	R/W	Sync filter bandwidth control	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x140 – WSS0

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WSS0	R	These are the sliced WSS data bit 19 to 14	-

0x141 – WSS1

Bit	Function	R/W	Description	Reset
7	CRCERR	R	This is the CRC error indicator for 525-line WSS 0 = No CRC error 1 = CRC error	-
6	WSSFLD	R	These bit indicates the detected WSS field information 0 = Odd 1 = Even	-
5-0	WSS1	R	These bits represent the sliced WSS data bit 13 to 8.	-

0x142 – WSS2

Bit	Function	R/W	Description	Reset
7-0	WSS2	R	These bits represent the sliced WSS bit 7 to 0.	-

SCALER

0x201 – General Scaler Control

Bit	Function	R/W	Description	Reset
7	MIRROR	R/W	1 = Enable horizontal mirror output 0 = Normal output	0
6	PWEN	R/W	1 = Enable Panoramic / water glass display 0 = Normal display	0
5	PXDBL	R/W	1 = Enable pixel doubling function. 0 = Disabled	0
4	LNDBL	R/W	1 = Enable line doubling function 0 = Disabled	0
3	LNEXT	R/W	Reserved for factory use.	0
2	LNFIX	R/W	1 = Fix the scaler output line number defined by register LNTT. 0 = Output line number determined by scaling factor.	0
1	VALOCK	R/W	1 = Output active start position tracks the input active position 0 = Output active start position defined by VA_POS register.	0
0	SMODE	R/W	Scaler mode selection 1 = Scaling from the start of the field / frame 0 = Scaling from the start of the input active	0

0x202– Scaling Offset Control

Bit	Function	R/W	Description	Reset
7-6	RDLY	R/W	Scaling buffer read out delay in lines	0
5-0	FOFFSET	R/W	Scaling initial offset control	20

0x203– XSCALE_LO

Bit	Function	R/W	Description	Reset
7-0	XSCALE_LO	R/W	Up scaling ratio control in X-direction. A 16-bit register. The scaling ratio is defined as 2000h / XSCALE.	00

0x204– XSCALE_HI

Bit	Function	R/W	Description	Reset
7-0	XSCALE_HI	R/W	Up scaling ratio control in X-direction. A 16-bit register. The scaling ratio is defined as 2000h / XSCALE	20

0x205– YSCALE_LO

Bit	Function	R/W	Description	Reset
7-0	YSCALE_LO	R/W	Up / down scaling ratio control in Y-direction. A 16-bit register. The scaling ratio is defined as 2000h / YSCALE.	00

0x206– YSCALE_HI

Bit	Function	R/W	Description	Reset
7-0	YSCALE_HI	R/W	Up / down scaling ratio control in Y-direction. A 16-bit register. The scaling ratio is defined as 2000h / YSCALE	20

0x207– PXSCALE

Bit	Function	R/W	Description	Reset
7-0	PXSCALE	R/W	Initial Scaling value for the Panoramic / water glass display in increment of 4. MSB 8-bit of a 12-bit register.	80

0x208– PXINC

Bit	Function	R/W	Description	Reset
7-0	PXINC[7-0]	R/W	Increment step value for the Panoramic / water glass display. The step is in 2's complement format for both positive and negative increment.	10

0x209– HDSCALE_LO

Bit	Function	R/W	Description	Reset
7-0	HDSCALE_LO	R/W	Down scaling control in X-direction. A 12-bit register. The down scaling ratio is defined as 100h / HDSCALE	00

0x20A– HDSCALE_HI

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	VANOM	R/W	VA control. Factory use only.	0
5	CEVEN	R/W	Reserved	0
4	HFT	R/W	Down scaler filter control. 1 = On 0 = Off	0
3-0	HDSCALE_HI	R/W	Down scaling control in X-direction. A 12-bit register. The down scaling ratio is defined as 100h / HDSCALE	1

0x20B– HDELAY2

Bit	Function	R/W	Description	Reset
7-0	HDELAY2	R/W	Scaler buffer data output delay in number of pixels in relation to the H sync.	30

0x20C– HACTIVE2_LO

Bit	Function	R/W	Description	Reset
7-0	HACTIVE2	R/W	Scaler data output length in number of pixels. A 10-bit register.	D0

0x20D– HACTIVE2_HI

Bit	Function	R/W	Description	Reset
7-6	HACTIVE2_HI	R/W	Scaler data output length in number of pixels. A 10-bit register	2
5	CKOSEL	R/W	Pixel clock output selection. 0 = divided clock specified by CKDIV 1 = un-divided clock	0
4	CKP	R/W	Pixel clock polarity control. 0 = Active High 1= Active Low	0
3	VSP	R/W	FPVS output polarity control. 0 = Active High 1= Active Low	0
2	HSP	R/W	FPHS output polarity control. 0 = Active High 1= Active Low	0
1-0	CKDIV	R/W	Pixel clock output frequency division control. 0 = 1 1 = ½ 2 = 1/3 3 = ¼	0

0x20E– HPADJ_HI

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	LNTT_HI	R/W	It controls the scaler total output lines when LNFIX=1. It is used in special case. A 10-bit register.	0
3-0	HPADJ_HI	R/W	Blanking H period adjustment. A 12-bit 2's complement register.	0

0x20F– HPADJ_LO

Bit	Function	R/W	Description	Reset
7-0	HPADJ_LO	R/W	Blanking H period adjustment. A 12-bit 2's complement register	00

0x210– HA_POS

Bit	Function	R/W	Description	Reset
7-0	HA_POS	R/W	Output DE position control relative to the internal reference in number of output clock	10

0x211– HA_LEN_LO

Bit	Function	R/W	Description	Reset
7-0	HALEN_LO	R/W	Output DE length control in number of the output clocks. A 12-bit register	00

0x212– HA_LEN_HI

Bit	Function	R/W	Description	Reset
7-4	PXSCALE	R/W	Initial X scaling factor. LSB 4-bit of a 12-bit register.	0
3-0	HALEN_HI	R/W	Output DE length control in number of the output clocks. A 12-bit register	3

0x213– HS_POS

Bit	Function	R/W	Description	Reset
7-0	HS_POS	R/W	Output H sync position relative to internal reference in number of output clocks.	10

0x214– HS_LEN

Bit	Function	R/W	Description	Reset
7-4	PXINC[11-8]	R/W	MSB 4-bit of a 12-bit register that defines the scaling increment for both panorama and waterglass display. It works with PXSCALE.	2
3-0	HS_LEN	R/W	Output H sync length in number of output clocks.	0

0x215– VA_POS

Bit	Function	R/W	Description	Reset
7-0	VA_POS	R/W	Output DE position control relative to the internal reference in number of output lines	20

0x216– VA_LEN_LO

Bit	Function	R/W	Description	Reset
7-0	HALEN_LO	R/W	Output DE control in number of the output lines. A 12-bit register	00

0x217– VA_LEN_HI

Bit	Function	R/W	Description	Reset
7-4	PXINC_HI	R/W	Output DE control in number of the output lines. A 12-bit register	0
3-0	HALEN_HI	R/W	Output DE control in number of the output lines. A 12-bit register	3

0x218– VS_LEN_POS

Bit	Function	R/W	Description	Reset
7-6	VS_LEN	R/W	Output V sync length in number of output lines.	0
5-0	VS_POS	R/W	Output V sync position relative to internal reference in number of output lines.	00

0x219– LNTT_LO

Bit	Function	R/W	Description	Reset
7-0	LNTT_LO	R/W	It controls the scaler total output lines when LNFIX=1. It is used in special case. A 10-bit register.	00

0x21A– DM_TOP

Bit	Function	R/W	Description	Reset
7-0	DM_TOP	R/W	These bits control the number of data masked lines (black lines) from the top of DE	00

0x21B– DM_BOT

Bit	Function	R/W	Description	Reset
7-0	DM_BOT	R/W	These bits control the number of data masked lines from the end of DE.	00

TCON

0x240– CSP Control

Bit	Function	R/W	Description	Reset
7-4	CSPWID	R/W	Column Start pulse width control in number of output clocks.	1
3-0	CSPPOS	R/W	Column start pulse position control relative to the leading edge of the DE	0

0x241– CLP Position

Bit	Function	R/W	Description	Reset
7-0	CLPPOS	R/W	Column latch pulse position control relative to either the trailing edge of DE of the start of line reference depending on CLPREF	0

0x242– CLP Width

Bit	Function	R/W	Description	Reset
7-0	CLPWID	R/W	Column latch pulse width control in number of output clocks.	01

0x243– RCK Control HI

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	RCKPOS_HI	R/W	RCK position control relative to the leading edge of DE in number of output clocks. A 11-bit register.	0
3	Reserved	R/W	Reserved	-
2-0	RCKWID_HI	R/W	RCK width control in number of output clocks. A 11-bit register.	0

0x244– RCK Position LO

Bit	Function	R/W	Description	Reset
7-0	RCKPOS_LO	R/W	RCK position control relative to the leading edge of DE in number of output clocks. A 11-bit register.	00

0x245– RCK Width LO

Bit	Function	R/W	Description	Reset
7-0	RCKWID_LO	R/W	RCK width control in number of output clocks. A 11-bit register.	01

0x246– ROE Control HI

Bit	Function	R/W	Description	Reset
7-6	ROE_EXT	R/W	Row driver enable pulse extension control.	0
5-4	ROEPOS_HI	R/W	ROE position control relative to the leading edge of DE in number of output clocks. A 10-bit register.	0
3	Reserved	R/W	Reserved	-
2-0	ROEWID_HI	R/W	ROE width control in number of output clocks. A 11-bit register.	0

0x247– ROE Position LO

Bit	Function	R/W	Description	Reset
7-0	ROEPOS_LO	R/W	ROE position control relative to the leading edge of DE in number of output clocks. A 10-bit register.	00

0x248– ROE Width LO

Bit	Function	R/W	Description	Reset
7-0	ROEWID_LO	R/W	ROE width control in number of output clocks. A 11-bit register.	01

0x249– RSP Control

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	RSPWID	R/W	Row Start pulse width control in number of output lines.	1
3	Reserved	R/W	Reserved	-
2-0	RSPPOS_HI	R/W	Row start pulse position control relative to the first output DE line. An 11-bit register in 2’s complement form.	0

0x24A– RSP position control

Bit	Function	R/W	Description	Reset
7-0	RSP_POS_LO	R/W	Row start pulse position control relative to the first output DE line. An 11-bit register in 2’s complement format.	00

0x24B– CPL position Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	CPLPOS_HI	R/W	Polarity pulse change position relative to the reference controlled by CPLREF in number of output clocks. This is a 11-bit register.	0
3-0	CPLEXT	R/W	Polarity pulse extension in number of lines. This is effective in polarity toggle mode 2 only.	0

0x24C– CPL position control LO

Bit	Function	R/W	Description	Reset
7-0	CPLPOS_LO	R/W	Polarity pulse change position relative to the reference controlled by CPLREF in number of output clocks. This is a 11-bit register.	10

0x24D– TCON Control I

Bit	Function	R/W	Description	Reset
7-6	ROEMOD	R/W	ROE output mode control. 0 = always low 1 = always high 2 = toggle 3 = N/A	2
5	CPLPOL	R/W	Polarity pulse polarity control. 0 = Active Low 1= Active High	0
4	RSPPOL	R/W	Row start pulse polarity control. 0 = Active High 1= Active Low	0
3	ROEPOL	R/W	Row output enable pulse polarity control. 0 = Active High 1 = Active Low	0
2	RCKPOL	R/W	Rck output plarity control. 0 = Active High 1 = Active Low	0
1	CLPPOL	R/W	Column driver latch pulse polarity control. 0 = Active High 1 = Active Low	0
0	CSPPOL	R/W	Column driver start pulse polarity control. 0 = Active High 1 = Active Low	0

0x24E– TCON Control II

Bit	Function	R/W	Description	Reset
7	CPLREF	R/W	Polarity pulse change reference point control. It is to be used with CPLPOS register. 0 = reference to internal line sync 1 = reference to trailing edge of DE	0
6	CPLSWP	R/W	Positive and negative polarity pulse swap. 0 = no swap	0
5-4	CPLTGM	R/W	Polarity pulses toggle mode control. 0 = frame inversion 1 = no frame inversion 2 = frame inversion in blanking period only	0
3	ROEDE	R/W	Row driver output enable control 0 = output in active line 1 = output in every line	0
2	CLPREF	R/W	Column driver latch pulse position reference control. 0 = leading edge of DE 1 = trailing edge of DE	0
1	CLPDE	R/W	Column driver latch pulse control. 0 = only output in active line 1 = output in every line	0
0	CSPDE	R/W	Column driver start pulse control. 0 = only output in active line 1 = output in every line.	0

0x280 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	HUE	R/W	Hue Adjustment. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (with 20h)	20

0x281 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_R	R/W	Red Contrast Adjustment 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x282 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_G	R/W	Green Contrast Adjustment 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x283 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_B	R/W	Blue Contrast Adjustment 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x284 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Y	R/W	Y Contrast Adjustment 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x285 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cb	R/W	Cb Contrast Adjustment 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x286 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_ Cr	R/W	Cr Contrast Adjustment 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x287 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS _R	R/W	Red Brightness Adjustment 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x288 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS _G	R/W	Green Brightness Adjustment 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x289 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS _B	R/W	Blue Brightness Adjustment 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x28A – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS _Y	R/W	Y Brightness Adjustment 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x28B – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	H_SHARP_ COR	R/W	Coring function for sharpness control	3
3-0	H_SHARPNE SS	R/W	Sharpness Adjustment	0

0x28C – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	H_SHARP_ FREQ	R/W	Sharpness frequency select 0 = Low freq 1 = High freq	0
6-0	Reserved	R/W	Reserved	-

0x2B0 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	PEDLVL	R/W	Black level selection. 0 = 0 1 = 16d	0
4	WHTLVL	R/W	White level selection. 0 = 235d 1 = 255d	1
3-1	Reserved	R/W	Reserved	-
0	BW_EN	R/W	0 = BW stretch disable 1 = BW stretch enable	0

0x2B1 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_BSLOPE	R/W	Black side slope. 00 = x1 40 = x2 80 = x3 C0h = x4 Should not be larger than D0h	40

0x2B2 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_WSLOPE	R/W	White side slope. 00 = x1 40 = x2 80 = x3 C0h = x4 Should not be larger than D0h	40

0x2B6 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_BLACK_T ILT	R/W	Tilt point for black stretch	67

0x2B7 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_WHITE_T ILT	R/W	Tilt point for white stretch	94

0x2BF – Test Pattern Generator Register

Bit	Function	R/W	Description	Reset
7	TPG_EN	R/W	1 = Internal Test Pattern Generator Enabled 0 = Scaler output (Default)	0
6-4	SWAP	R/W	RGB/YcbCr byte swap for color change	0
3-0	PAT_SEL	R/W	Pattern selection. 0: Hue map 1: Hue map (fine) 2: Gray horizontal 17 steps 3: Gray vertical 17 steps 4: Gray H/V 17x17 steps 5: White rectangle 6: Vertical 1-dot stripe 7: Horizontal 1-dot stripe 8: Black/White checker board 9: RGB checker board A: Gray horizontal 17 steps + horizontal black stripes B: Mitsubishi WQVGA test pattern C: Flat 100% blue D: Ramp E, F: Flat 50% gray	0

0x2E0 – Gamma Control Register

Bit	Function	R/W	Description	Reset
7	GAMAE_R	R/W	Enable Red gamma correction.	0
6	GAMAE_G	R/W	Enable Green gamma correction.	0
5	GAMAE_B	R/W	Enable Blue gamma correction.	0
4	Reserved	R/W	Reserved	-
3-2	AUTO_INC	R/W	Enable Gamma table address auto increment for reading/writing Gamma data port. 0 = Disable 1 = Read Only 2 = Write Only 3 = Read/Write	0
1-0	GAMMA_RGB_INDX	R/W	Gamma tables access selection: Index address 0x2E1 to 0x2E2 are used for gamma table accesses. There are 3 sets of gamma table, one table for one color, sharing the same address port and data port. These 2 bits identifies which table is accessed. 0 = RGB Gamma table 1 = Red Gamma table 2 = Green Gamma table 3 = Blue Gamma table	0

0x2E1 – Gamma Table Address Port Register

Bit	Function	R/W	Description	Reset
7-0	GAMMA_RAM-STARTING_ADDR	R/W	Gamma table address port.	00

0x2E2 – Gamma Table Data Port Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W	Reserved	-
1-0	GAMMA_RAM_DATA[9:8]	R/W	Gamma table data port (upper bits)	0

0x2E3 – Gamma Table Data Port Register

Bit	Function	R/W	Description	Reset
7-0	GAMMA_RAM_DATA[7:0]	R/W	Gamma table data port (lower bits)	0

0x2E4 – Dither Option Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	DITHER_OPTION	R/W	Dither Option Code "010" is recommended for 6:6:6 output	0
3	Reserved	R/W	Reserved	-
2-0	DITHER_FORMAT	R/W	Dither Output Format Selection "001" is recommended for 6:6:6 output	0

Dither Output Selection and Calculations

Dither Output Format Selection	Flat Panel RGB Bit Format Output	Dither Option Code	Input LSBs Used in Dither Calculation	Dither Method
000	8:8:8	**000**	n/a	none
001	6:6:6	**001**	(3) (3) (3)	2x2
		010	(3,2) (3,2)(3,2)	2x2
		011	(3,2,1) (3,2,1)(3,2,1)	2x2
		100	(3,2,1,0) (3,2,1,0)(3,2,1,0)	4x4
010	5:6:5	**001**	(4) (3) (4)	2x2
		010	(4,3) (3,2) (4,3)	2x2
		011	(4,3,2) (3,2) (4,3,2)	2x2
		100	(4,3,2,1) (3,2,1) (4,3,2,1)	4x4
011	5:5:5	**001**	(4) (4) (4)	2x2
		010	(4,3) (4,3) (4,3)	2x2
		011	(4,3,2) (4,3,2) (4,3,2)	2x2
		100	(4,3,2,1) (4,3,2,1) (4,3,2,1)	4x4
100	4:4:4	**001**	(5) (5) (5)	2x2
		010	(5,4) (5,4) (5,4)	2x2
		011	(5,4,3) (5,4,3) (5,4,3)	2x2
		100	(5,4,3,2) (5,4,3,2) (5,4,3,2)	4x4
101	3:3:3	**001**	(6) (6) (6)	2x2
		010	(6,5) (6,5) (6,5)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (6,5,4,3)	4x4
110	3:3:2	**001**	(6) (6) (7)	2x2
		010	(6,5) (6,5) (7,6)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (7,6,5,4)	4x4

0x2F0 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RDKEYPOS_X	R/W	Color level readout position X [7:0] (LSB)	00

0x2F1 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RDKEYPOS_Y	R/W	Color level readout position Y [7:0] (LSB)	00

0x2F2 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	RDKEYPOS_Y[10:8]	R/W	Color level readout position Y [10:8] (MSB)	0
3-0	RDKEYPOS_X[11:8]	R/W	Color level readout position X [11:8] (MSB)	0

0x2F3 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RED_LVL	R	Red level	-

0x2F4 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	GRN_LVL	R	Green level	-

0x2F5 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	BLU_LVL	R	Blue level	-

0x2F8 – 8-bit Panel Interface Register

Bit	Function	R/W	Description	Reset
7	DELTA_EN	R/W	Reserved	-
6	RGB_ORDR	R/W	0 = R->G->B order 1 = R->B->G order	0
5	AVRG_EN	R/W	1 = Averaging on every other line enable 0 = No Averaging	0
4	AVRG_POL	R/W	1 = Averaging on even line 0 = Averaging on odd line	0
3-2	COL_ODD	R/W	Start color for odd line 0 = R 1 = B 2 = G 3 = N/A	0
1-0	COL_EVEN	R/W	Start color for even line 0 = R 1 = B 2 = G 3 = N/A	0

0x2F9 – 8-bit Panel Interface Register

Bit	Function	R/W	Description	Reset
7	DELTA_TYPE	R/W	Type selection of 8-bit interface for averaging 1 = Serial RGB 0 = Delta RGB	1
6-2	Reserved	R/W	Reserved	-
1	DMMY_EN	R/W	Serial RGB mode 1 = S-RGB with Dummy 0 = S-RGB without Dummy	0
0	DMMY_POS	R/W	Serial RGB Dummy byte position 1 = Dummy comes first 0 = Dummy comes last	0

0x300 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2	MIREN	R/W	1 = Enable FONT Mirror	0
1	FONT_SWITC	R/W	1 = Bypass FONT RAM FIFO	0
0	OSD_SWITCH	R/W	1 = Bypass OSD RAM FIFO	0

0x301 – Test Register

Bit	Function	R/W	Description	Reset
7-1	Reserved	R/W	Reserved	-
0	STATUS	R	OSD Window Active Status	-

0x302 – Test Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	DBGWIN	R/W	OSD Debug Window Selection	0
3-0	DBG	R/W	OSD Debug Signal Selection	6

0x303 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-0	OSD DE Delay	R/W	OSD DE Delay from H-SYNC	06

0x304 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7	BLINK	R/W	1 = Character Blinking effect enable	0
6	ITALIC	R/W	1 = Character Italic effect enable.	0
5	ULINE	R/W	1 = Character Underline effect enable.	0
4	BSEN	R/W	1 = Character Bordering/Shadowing effect enable.	0
3-2	AUTO	R/W	OSD RAM Auto Increase of Write Address Mode Selection. 0 = Normal mode 1 = Font Data or Attribute Address auto mode 3 = Font Data auto mode(Previous Attribute data automatic write)	0
1	CLEAR	R/W	OSD RAM Auto Clear Mode	0
0	FR_RAC_SEL	R/W	Font/OSD RAM Serial Bus Access 0 = OSD RAM 1 = Font RAM access	0

0x305 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	FBITEXT	R/W	1 = Enable character horizontal extension.	0
4	RD_SEL	R/W	Register 0x307, 308 Read mode selection. 0 = Normal display 1 = QVGA display	0
3-1	Reserved	R/W	Reserved	-
0	I2COSDRAD	R/W	OSD RAM Address High 1-bit (total 9 bits).	0

0x306 – OSD RAM Address Register

Bit	Function	R/W	Description	Reset
7-0	I2COSDRAD	R/W	OSD RAM Address Low 8-bit (word address for single byte access).	00

0x307 – OSD RAM Data Port Hi Register

Bit	Function	R/W	Description	Reset
7-0	FDATA	R/W	OSD RAM Data Port Hi (Font Data).	00

0x308 – OSD RAM Data Port Lo Register

Bit	Function	R/W	Description	Reset
7-0	FATTRIBUTE	R/W	OSD RAM Data Port Lo (Font Attribute).	00

0x309 – Font RAM Address Register

Bit	Function	R/W	Description	Reset
7-0	I2CFONTRAD	R/W	Serial Bus Font RAM Address.	00

0x30A – Font RAM Data Port

Bit	Function	R/W	Description	Reset
7-0	I2CFONTDAT	R/W	Serial Bus Font RAM Data Port.	00

0x30B – Multi-Color Font Start Position Register

Bit	Function	R/W	Description	Reset
7-0	MADD	R/W	Programmable SRAM address start position for Multi-Color fonts.	31

0x30C – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4	OSDON	R/W	OSD ON/OFF Control 0 = OSD ON 1 = OSD OFF	0
3-0	TABLE_WSEL	R/W	Character color look up table write address select.	0

0x30D – Character Color Look-up table data port High Byte Register

Bit	Function	R/W	Description	Reset
7-0	TABLE_CON_H	R/W	Character color look up table data port high byte.	00

0x30E – Character Color Look-up table data port Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	TABLE_CON_L	R/W	Character color look up table data port low byte.	00

0x310 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1EN	R/W	OSD Window #n Enable	0
6	WIN1MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN1CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved	-

3-2	XWIN1ZOOM	R/W	OSD Window #n Horizontal Zoom.
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

1-0	YWIN1ZOOM	R/W	OSD Window #n Vertical Zoom.
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

0x311 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN1ASEL	R/W	Window alpha blending color selection.	0
3-0	WIN1ALPHA	R/W	OSD Window #n alpha blending amount.	0

0x312 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	WIN1HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved	-
1-0	WIN1VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

0x313 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN1HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

0x314 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN1VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

0x315 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN1HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

0x316 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN1WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

0x317 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4	WIN1REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9 bits) of OSD Window #n.	0
3-0	WIN1BC	R/W	OSD Window #n Border Color control.	0

0x318 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved	-
4-0	WIN1BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

0x319 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN1HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

0x31A – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN1VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

0x31B – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN1TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN1EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN1BSEL	R/W	Character Border/Shadow selection. 1 = Shadow 0 = Border	0
3-0	WIN1SC	R/W	OSD Window #n shadow color control.	0

0x31C – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN1CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN1CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN1SCWID	R/W	OSD Window #n shadow width.	0

0x31D – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN1CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN1CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

0x31E – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN1BGC	R/W	OSD Window #n Background Color control	0
3-0	WIN1BSC	R/W	OSD Window #n character border/shadow color Control	0

0x31F – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN1REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

0x320 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2EN	R/W	OSD Window #n Enable	0
6	WIN2MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN2CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved	-

3-2	XWIN2ZOOM	R/W	OSD Window #n Horizontal Zoom
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

1-0	YWIN2ZOOM	R/W	OSD Window #n Vertical Zoom
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

0x321 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN2ASEL	R/W	Window alpha blending color selection.	0
3-0	WIN2ALPHA	R/W	OSD Window #n alpha blending amount.	0

0x322 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	WIN2HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved	-
1-0	WIN2VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

0x323 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN2HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

0x324 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN2VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

0x325 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN2HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

0x326 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN2WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

0x327 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4	WIN2REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9 bits) of OSD Window #n.	0
3-0	WIN2BC	R/W	OSD Window #n Border Color control.	0

0x328 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved	-
4-0	WIN2BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

0x329 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN2HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

0x32A – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN2VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

0x32B – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN2TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN2EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN2BSEL	R/W	Character Border/Shadow selection. 1 = Shadow 0 = Border	0
3-0	WIN2SC	R/W	OSD Window #n shadow color control.	0

0x32C – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN2CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN2CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN2SCWID	R/W	OSD Window #n shadow width.	00

0x32D – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN2CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN2CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

0x32E – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN2BGC	R/W	OSD Window #n Background Color control	0
3-0	WIN2BSC	R/W	OSD Window #n character border/shadow color Control	0

0x32F – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN2REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

0x330 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3EN	R/W	OSD Window #n Enable	0
6	WIN3MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN3CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved.	-

3-2	XWIN3ZOOM	R/W	OSD Window #n Horizontal Zoom
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

1-0	YWIN3ZOOM	R/W	OSD Window #n Vertical Zoom
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

0x331 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN3ASEL	R/W	Window alpha blending color selection.	0
3-0	WIN3ALPHA	R/W	OSD Window #n alpha blending amount.	0

0x332 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	WIN3HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved	-
1-0	WIN3VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

0x333 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN3HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

0x334 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN3VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

0x335 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN3HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

0x336 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN3WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

0x337 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4	WIN3REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9 bits) of OSD Window #n.	0
3-0	WIN3BC	R/W	OSD Window #n Border Color control.	0

0x338 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved	-
4-0	WIN3BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	0

0x339 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN3HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

0x33A – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN3VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

0x33B – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN3TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN3EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN3BSEL	R/W	Character Border/Shadow selection. 1 = Shadow 0 = Border	0
3-0	WIN3SC	R/W	OSD Window #n shadow color control.	0

0x33C – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN3CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN3CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN3SCWID	R/W	OSD Window #n shadow width.	0

0x33D – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN3CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN3CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

0x33E – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN3BGC	R/W	OSD Window #n Background Color control	0
3-0	WIN3BSC	R/W	OSD Window #n character border/shadow color Control	0

0x33F – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN3REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

0x340 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4EN	R/W	OSD Window #n Enable	0
6	WIN4MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN4CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved	-

3-2	XWIN4ZOOM	R/W	OSD Window #n Horizontal Zoom.
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

1-0	YWIN4ZOOM	R/W	OSD Window #n Vertical Zoom.
			0 = no zoom 1 = x2 3 = x3 4 = x4
				0

0x341 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN4ASEL	R/W	Window alpha blending color selection.	0
3-0	WIN4ALPHA	R/W	OSD Window #n alpha blending amount.	0

0x342 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	WIN4HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved	-
1-0	WIN4VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

0x343 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN4HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

0x344 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN4VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

0x345 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN4HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

0x346 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	WIN4WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

0x347 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4	WIN4REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9 bits) of OSD Window #n.	0
3-0	WIN4BC	R/W	OSD Window #n Border Color control.	0

0x348 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved	-
4-0	WIN4BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

0x349 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN4HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

0x34A – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN4VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

0x34B – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN4TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN4EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN4BSEL	R/W	Character Border/Shadow selection. 1 = Shadow 0 = Border	0
3-0	WIN4SC	R/W	OSD Window #n shadow color control.	0

0x34C – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN4CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN4CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN4SCWID	R/W	OSD Window #n shadow width.	0

0x34D – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN4CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN4CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

0x34E – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN4BGC	R/W	OSD Window #n Background Color control	0
3-0	WIN4BSC	R/W	OSD Window #n character border/shadow color Control	0

0x34F – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN4REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	0

SPI OSD 0x400~ 0x457 (for TW8833S only)

0x400 – OSD Control Register

Bit	Function	R/W	Description	Reset
7-6	BLTSEL	R/W	Blink timer interval selection 0 = 33 frames 1 = 16 frames 2 = 8 frames 3 = 4 frames	0
5-2	Reserved	R/W	Reserved.	-
1	MIXODR	R/W	OSD and video mixing order 0 = video & SPIOSD first, then mixed with Font OSD 1 = video & Font OSD first, then mixed with SPIOSD	0
0	OSDSRST	R/W	Soft reset for SPIOSD section	0

0x40F – SPIOSD Timing Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	TIMADJ	R/W	Adjust SPIOSD data read timing	45

0x410 – 8-Bit SPIOSD Look Up Table Access Control Register

Bit	Function	R/W	Description	Reset
7	LUTWE	R/W	This bit enable look up table write access for MCU or DMA 1 = Enable Look up table write access	0
6-5	LUTINC_SEL	R/W	LUT pointer increment selection: 0 = No increment 1 = Byte pointer increments by 1 after each LUT data port write ; when it reaches “11”, the byte pointer wraps around and the address pointer increments by 1 2 = Address pointer increments by 1 after each LUT data port write; when it reaches “FF”, the address pointer wraps around and the byte pointer increments by 1 Note: For DMA write access, there are only two valid selection, “01” or “10”.	0
4-2	Reserved	R/W	Reserved	-
1-0	LUTBYT	R/W	Byte pointer for the LUT access. Read reflects the current byte pointer value. If DMA is used to read from SPI Flash and write to LUT, the initial byte pointer is specified by 0x486[1:0] (with 0x410[6:5] =10), or 0x487[1:0] (with 0x 410[6:5] =01).	0

0x411 – 8 Bit SPIOSD Look Up Table Address [7:0] Register

Bit	Function	R/W	Description	Reset
7-0	LUTADDR	R/W	Address pointer to one of the 256 entries of the LUT. Read reflects the current address pointer value. If DMA is used to read from SPI Flash and write to LUT, the initial address is specified by 0x487[7:0] (with 0x410[6:5]=10), or 0x486[1:0]#0x487[7:2] (with 0x 410[6:5]=01).	00

0x412 – 8 Bit SPIOSD Look Up Table Data Port [7:0] Register

Bit	Function	R/W	Description	Reset
7-0	LUTDATA	R/W	Write data to the look up table pointed by the Address and Byte pointers Read returns the data pointed by the Address and Byte pointers. Two reads are required to get the correct data. Read does not advance either the Address pointer or Byte pointer. This register is not used for DMA write LUT.	00

0x420 – SPIOSD Window 0 Enable Register

Bit	Function	R/W	Description	Reset
7-6	WIN0LPE	R/W	Enable Window 0 loop back 0 = No looping; displays one time of the loop and then disappears 1 = No looping; displays one time of the loop and then stays at the last frame 2,3 = Enable looping	0
5	WIN0_PERPIX	R/W	OSD window 0 alpha blending selection 0 = Global window 0 alpha 1 = Per pixel alpha	0
4	WIN0_ALPHA_ENA	R/W	OSD window 0 alpha blending enable	0
3-1	Reserved	R/W	Reserved	-
0	WIN0_ENA	R/W	OSD window 0 = Enable	0

0x421 ~ 0x422 – SPIOSD Window 0 Horizontal Start [10:0] Registers

0x421 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WIN0_HS_HB	R/W	OSD window 0 horizontal start (offset from the LCD display first left pixel) High byte	0

0x422 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_HS_LB	R/W	OSD window 0 horizontal start (offset from the LCD display first left pixel) Low byte	00

0x423~0x424 – SPIOSD Window 0 Vertical Start [10:0] Registers

0x423 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WIN0_VS_HB	R/W	OSD window 0 Vertical start (offset from the LCD display top first line) High byte	0

0x424 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_VS_LB	R/W	OSD window 0 Vertical start (offset from the LCD display top first line) Low byte	00

0x425~0x0426 – SPIOSD Window 0 Horizontal Length [11:0] Registers

0x0425 – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	WIN0_HL_HB	R/W	OSD window 0 horizontal Length High byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x426 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_HL_LB	R/W	OSD window 0 horizontal Length Low byte (one pixel per increment, minimum is 1, maximum is 2048)	00

0x427~0x0428 – SPIOSD Window 0 Vertical Length [11:0] Registers

0x427 – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	WIN0_VL_HB	R/W	OSD window 0 vertical Length High byte (one line per increment, minimum is 1, maximum is 2048)	0

0x428 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_VL_LB	R/W	OSD window 0 vertical Length Low byte (one line per increment, minimum is 1, maximum is 2048)	00

0x429 – 0x42B SPIOSD Window 0 Buffer Memory Starting Address [23:0] Register

0x429 – High Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM0_AST_HB	R/W	Starting address of the Buffer Memory area allocated for OSD window 0; one byte per increment	00

0x42A – Mid byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM0_AST_MB	R/W	Starting address of the Buffer Memory area allocated for OSD window 0	00

0x42B – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM0_AST_LB	R/W	Starting address of the Buffer Memory area allocated for OSD window 0	00

0x42C~0x42D – SPIOSD Window 0 Buffer Horizontal Length [11:0] Registers

0x42C – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	BFM0_HL_HB	R/W	Define the Window 0 buffer horizontal length per frame, one pixel per increment; max length 2048 pixels. There can be more than one frame horizontally, but the total pixel horizontally is capped at 4095.	0

0x42D – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM0_HL_LB	R/W	(See description above)	00

0x42E~0x42F – SPIOSD Window 0 Buffer Vertical Length [11:0] Registers

0x42E – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved.	-
3-0	BFM0_VL_HB	R/W	Define the Window 0 buffer vertical length per frame, one line per increment; max length 2048 lines)	0

0x42F – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM0_VL_LB	R/W	(See description above)	00

0x430~0x431 – SPIOSD Window 0 Image Horizontal Start [10:0] Registers

0x430 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WFM0_HS_HB	R/W	Define the horizontal offset of the OSD Window 0 image from the buffer starting location; one pixel per increment	0

0x431 – Low byte Register

Bit	Function	R/W	Description	Reset
7-0	WFM0_HS_LB	R/W	(See description above)	00

0x432~0x434 — SPIOSD Window 0 Image Vertical Start [10:0] Registers

0x432 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WFM0_VS_HB	R/W	Define the vertical offset of the OSD Window 0 image from the buffer starting location; one line per increment	0

0x433 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WFM0_VS_LB	R/W	(See description above)	00

0x434 – SPIOSD Window 0 Global Alpha Value [6:0] Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN0_ALPHA	R/W	OSD window 0 global alpha blending value Min: 0x00 Max OSD window 0 shown after blending Max: 0x7F No OSD window 0 shown after blending	00

0x435~0x437 – SPIOSD Window 0 Loop Control Registers

0x435 – Looping Horizontal Frame Number Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_LPHNUM	R/W	Number of OSD frames horizontally in memory for the window 0 loop display The display starts from number 0. Upon reaching the number specified by this register, it returns to number 0. 0 = One frame 1 = Two frames FF = 256 frames	00

0x436 – Looping Vertical Frame Number Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_LPVNUM	R/W	Number of OSD frames vertically in memory for the window 0 loop display The display starts from number 0. Upon finishing the last horizontal frame, the number increments by 1. 0 = One frame 1 = Two frames FF = 256 frames	00

0x437 – Frame Duration Register

Bit	Function	R/W	Description	Reset
7-0	WIN0_FD	R/W	Duration time of each frame (in unit of Vsync) 0 = Infinite 1 = One Vsync period FF = 255 Vsync periods	00

0x440 – SPIOSD Window 1 Enable Register

Bit	Function	R/W	Description	Reset
7-6	WIN1LPE	R/W	Enable Window 1 loop back 0 = No looping; displays one time of the loop and then disappears 1 = No looping; displays one time of the loop and then stays at the last frame 2,3 = Enable looping	0
5	WIN1_PERPIX	R/W	OSD window 1 alpha blending selection 0 = Global window 1 alpha 1 = Per pixel alpha	0
4	WIN1_ALPHA_ENA	R/W	OSD window 1 alpha blending enable	0
3-1	Reserved	R/W	Reserved	-
0	WIN1_ENA	R/W	OSD window 1 (8 bit) enable; priority is lower than OSD window 0	0

0x441~ 0x442 – SPIOSD Window 1 Horizontal Start [10:0] Registers

0x441 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WIN1_HS_HB	R/W	OSD window 1 horizontal start (offset from the LCD display first left pixel) High byte	0

0x442 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_HS_LB	R/W	OSD window 1 horizontal start (offset from the LCD display first left pixel) Low byte	00

0x443~0x444 – SPIOSD Window 1 Vertical Start [10:0] Registers

0x443 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WIN1_VS_HB	R/W	OSD window 1 Vertical start (offset from the LCD display top first line) High byte	0

0x444 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_VS_LB	R/W	OSD window 1 Vertical start (offset from the LCD display top first line) Low byte	00

0x445~0x446 – SPIOSD Window 1 Horizontal Length [11:0] Registers

0x445 – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	WIN1_HL_HB	R/W	OSD window 1 horizontal Length High byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x446 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_HL_LB	R/W	OSD window 1 horizontal Length Low byte (one pixel per increment, minimum is 1, maximum is 2048)	00

0x447~0x448 – SPIOSD Window 1 Vertical Length [11:0] Registers

0x447 – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	WIN1_VL_HB	R/W	OSD window 1 vertical Length High byte (one line per increment, minimum is 1, maximum is 2048)	0

0x448 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_VL_LB	R/W	OSD window 1 vertical Length Low byte (one line per increment, minimum is 1, maximum is 2048)	00

0x449~0x044B – SPIOSD Window 1 Buffer Memory Starting Address [23:0] Registers

0x0449 – High Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM1_AST_HB	R/W	Starting address of the Buffer Memory area allocated for OSD window 1; one byte per increment	00

0x44A – Mid Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM1_AST_MB	R/W	Starting address of the Buffer Memory area allocated for OSD window 1	00

0x44B – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM1_AST_LB	R/W	Starting address of the Buffer Memory area allocated for OSD window 1	00

0x44C~0x044D – SPIOSD Window 1 Buffer Horizontal Length [11:0] Registers

0x44C – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	BFM1_HL_HB	R/W	Define the Window 1 buffer horizontal length per frame, one pixel per increment; max length 2048 pixels. There can be more than one frame horizontally, but the total pixel horizontally is capped at 4095.	0

0x44D – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM1_HL_LB	R/W	(See description above)	00

0x44E~0x44F – SPIOSD Window 1 Buffer Vertical Length [11:0] Registers

0x44E – High Byte Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	BFM1_HL_HB	R/W	Define the Window 1 buffer vertical length per frame, one line per increment; max length 2048 lines)	0

0x44F – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	BFM1_HL_LB	R/W	(See description above)	00

0x450~0x51F – SPIOSD Window 1 Image Horizontal Start [10:0] Registers

0x450 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved.	-
2-0	WFM1_HS_HB	R/W	Define the horizontal offset of the OSD Window 1 image from the buffer starting location in each frame; one pixel per increment	0

0x451 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WFM1_HS_LB	R/W	(See description above)	00

0x452~0x453 – SPIOSD Window 1 Image Vertical Start [10:0] Registers

0x452 – High Byte Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	WFM1_VS_HB	R/W	Define the vertical offset of the OSD Window 1 image from the buffer starting location in each frame; one line per increment	0

0x453 – Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	WFM1_VS_LB	R/W	(See description above)	00

0x454 – SPIOSD Window 1 Global Alpha Value [6:0] Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-0	WIN1_ALPHA	R/W	OSD window 1 global alpha blending value Min: 0x00 Max OSD window 1 shown after blending Max: 0x7F No OSD window 1 shown after blending	00

0x455~0x457 – SPIOSD Window 1 Loop Control Registers

0x455 – Looping Horizontal Frame Number Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_LPHNUM	R/W	Number of OSD frames horizontally in buffer memory for the window 1 loop display The display starts from number 0. Upon reaching the number specified by this register, it returns to number 0. 0 = One frame 1 = Two frames FF = 256 frames	00

0x456 – Looping Vertical Frame Number Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_LPVNUM	R/W	Number of OSD frames vertically in buffer memory for the window 1 loop display The display starts from number 0. Upon finishing the last horizontal frame, the number increments by 1. 0 = One frame 1 = Two frames FF = 256 frames	00

0x457 – Frame Duration Register

Bit	Function	R/W	Description	Reset
7-0	WIN1_FD	R/W	Duration time of each frame (in unit of Vsync 0 = Infinite 1 = One Vsync period FF = 255 Vsync periods	00

SPI Interface

0x480 – SPI Flash Mode Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	HOST SPI_MODE	R/W	SPI Flash Read Mode 0 = slow 1 = fast 2 = dual 3 = quad 4 = dual-io 5 = quad-io 6 = double edge quad 7,8 = N/A	0
3	Reserved	R/W	Reserved	-
2-0	OSD SPI_MODE	R/W	SPI Flash Read Mode 0 = slow 1 = fast 2 = dual 3 = quad 4 = dual-io 5 = quad-io 6 = double edge quad 7,8 = N/A	0

0x481 – SPI Flash Mode Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	EDGE_SEL	R/W	0 = Negative edge 1 = Positive edge	0
4	CYCLE_EN	R/W	Enable one cycle delay mode	0
3-1	Reserved	R/W	Reserved	-
0	DMA_NONV	R/W	Start mode 0 = Immediately 1 = At vertical blank	0

0x483 – DMA Control Register

Bit	Function	R/W	Description	Reset
7-6	DMA_SEL	R/W	Read/Write destination 0 = Font RAM data 1 = Chip Register 2 = SPIOSD LUT 3 = N/A	1
5-4	DMA_REG_MODE	R/W	Read/Write access mode 0 = Increase 1 = Decrease 2 = Fix 3 = N/A	0
3-0	WR_CNT_NUM	R/W	Command write byte count	0

0x484 – Flash Busy Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2	BUSY_CHECK	R/W	Busy check 0 = No busy check 1 = Busy check after command. Wait until busy is cleared	0
1	WR_MODE	R/W	SPI DMA/CMD Mode 0 = Read, 1 = Write	0
0	DMA_STR	R/W	Start command execution. Self cleared. Write '1' = Start Write '0' = Stop Read '1' = Busy Read '0' = Ready	0

0x485 – Wait Control Register

Bit	Function	R/W	Description	Reset
7-4	DMA_WAIT	R/W	DMA read wait cycle	8
3-0	SPI_WAIT	R/W	SPI read/write wait cycle	0

0x486 – DMA Page Register

Bit	Function	R/W	Description	Reset
7-0	DMA_REG_PAGE	R/W	Buffer index page or memory start address high byte	04

0x487 – DMA Index Register

Bit	Function	R/W	Description	Reset
7-0	INDEX	R/W	Buffer index or memory start address low byte	90

0x488 – DMA Length Mid Byte Register

Bit	Function	R/W	Description	Reset
7-0	DMA_LENGTH	R/W	Read/Write data count mid byte after command	00

0x489 – DMA Length Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	DMA_LENGTH	R/W	Read/Write data count low byte after command	00

0x48A – DMA Command Buffer Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG1_RG	R/W	Command buffer 1	00

0x48B – DMA Command Buffer2 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG2_RG	R/W	Command buffer 2	00

0x48C – DMA Command Buffer3 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG3_RG	R/W	Command buffer 3	00

0x48D – DMA Command Buffer4 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG4_RG	R/W	Command buffer 4	00

0x48E – DMA Command Buffer5 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG5_RG	R/W	Command buffer 5	00

0x490 – DMA Read/Write Buffer1 Register

Bit	Function	R/W	Description	Reset
7-0	BUF1	R/W	Default Read/write buffer 1	00

0x491 – DMA Read/Write Buffer2 Register

Bit	Function	R/W	Description	Reset
7-0	BUF2	R/W	Default Read/write buffer 2	00

0x492 – DMA Read/Write Buffer3 Register

Bit	Function	R/W	Description	Reset
7-0	BUF3	R/W	Default Read/write buffer 3	00

0x493 – DMA Read/Write Buffer4 Register

Bit	Function	R/W	Description	Reset
7-0	BUF4	R/W	Default Read/write buffer 4	00

0x494 – DMA Read/Write Buffer5 Register

Bit	Function	R/W	Description	Reset
7-0	BUF5	R/W	Default Read/write buffer 5	00

0x495 – DMA Read/Write Buffer6 Register

Bit	Function	R/W	Description	Reset
7-0	BUF6	R/W	Default Read/write buffer 6	00

0x496 – DMA Read/Write Buffer7 Register

Bit	Function	R/W	Description	Reset
7-0	BUF7	R/W	Default Read/write buffer 7	00

0x497 – DMA Read/Write Buffer8 Register

Bit	Function	R/W	Description	Reset
7-0	BUF8	R/W	Default Read/write buffer 8	00

0x498 – SPI Flash Status Command Register

Bit	Function	R/W	Description	Reset
7-0	STATUS_CMD_RG	R/W	Status command	05

0x499 – SPI Flash Busy Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3	BUSY_POL	R/W	Busy polarity 0 = Low 1 = High	1
2-0	BUSY_BIT	R/W	Busy bit in status command	0

0x49A – DMA Length High Byte Register

Bit	Function	R/W	Description	Reset
7-0	DMA_LENGTH	R/W	Read/Write data count high byte after command	00

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Revision History

Date	Revision Note
3/18/2010	Initial Draft
6/01/2010	-Correct I2C address -Correct Pin#38 Description -Add Power consumption information -Updated register 0x008[7:6][3:0], 0x2E4, 0x006[3:0], 0x20D[4:2], 0x2E0[1:0],0x24D[5:0], 0x0E8[4], 0x0DB[6:4]
10/25/2010	-Add Font OSD function description -Change company logo