QPRO XQ4000XL Series QML High-Reliability FPGAs

DS029 (v1.3) June 25, 2000 **Product Specification**

2

XQ4000X Series Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing)
- Ceramic and plastic packages
- Also available under the following standard microcircuit drawings (SMD)
  - XQ4013XL 5962-98513
  - XQ4036XL 5962-98510
  - XQ4062XL 5962-98511
  - XQ4085XL 5962-99575
- For more information contact the Defense Supply Center Columbus (DSCC) **http://www.dscc.dla.mis/v/va/smd/smdsrch.html**
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - SelectRAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System performance beyond 50 MHz
- Flexible array architecture
- Low power segmented routing architecture
- Systems-oriented features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per XQ4000XL output
- Configured by loading binary file
  - Unlimited reprogrammability
- Readback capability
  - Program verification
  - Internal node observability
- Development system runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest capacity—over 180,000 usable gates
- Additional routing over XQ4000E
  - Almost twice the routing capacity for high-density designs
- Buffered Interconnect for maximum speed
- New latch capability in configurable logic blocks
- Improved VersaRing™ I/O interconnect for better Fixed pinout flexibility
  - Virtually unlimited number of clock signals
- Optional multiplexer or 2-input function generator on device outputs
- 5V tolerant I/Os
- 0.35 μm SRAM process

Introduction

The QPRO™ XQ4000XL Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated soft-ware to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000XL Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing, and the latest Xilinx databook for package pinouts other than the CB228 (included in this data sheet). (Pinouts for XQ4000XL device are identical to XC4000XL.)

Table 1: **XQ4000XL Series High Reliability Field Progammable Gate Arrays**

Device	Logic Cells	Max Logic Gates (No RAM)(1)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)(1)	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XQ4013XL	2432	13,000	18,432	10,000-30,000	24x24	576	1,536	192	PG223, CB228, PQ240, BG256
XQ4036XL	3078	36,000	41,472	22,000-65,000	36x36	1,296	3,168	288	PG411, CB228, HQ240, BG352
XQ4062XL	5472	62,000	73,728	40,000-130,000	48x48	2,304	5,376	384	PG475, CB228, HQ240, BG432
XQ4085XL	7448	85,000	100,352	55,000-180,000	56x56	3,136	7,168	448	PG475, CB228, HQ240, BG432

Notes:
1. Maximum values of typical gate range includes 20% to 30% of CLBs used as RAM.

XQ4000XL Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or devicefamilies. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

2

All specifications subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family AC supplements available on the Xilinx web site at:

http://www.xilinx.com/partinfo/databook.htm.

Absolute Maximum Ratings(1)

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(2)		–0.5 to 5.5	V
V_{TS}	Voltage applied to High-Z output(2)		–0.5 to 5.5	V
V_{CCt}	Longest supply voltage rise time from 1V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic package	+150	°C
		Plastic package	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to V_{CC} + 2.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions(1)

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic	3.0	3.6	V
	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic	3.0	3.6	V
V_{IH}	High-level input voltage(2)		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of V_{CC}.

XQ4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage at I_{OH} = –4 mA, V_{CC} min (LVTTL)		2.4	-	V
	High-level output voltage at I_{OH} = –500 µA, (LVCMOS)		90% V_{CC}	-	V
V_{OL}	Low-level output voltage at I_{OL} = 12 mA, V_{CC} min (LVTTL)(1)		-	0.4	V
	Low-level output voltage at I_{OL} = 1500 µA, (LVCMOS)		-	10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	V
I_{CCO}	Quiescent FPGA supply current(2)		-	5	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	-	10	pF
		PGA packages	-	16	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.6V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low		0.3	2.0	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA.
2. With no output current loads, no active input or Longline pull-up resistors, all I/O pins in a High-Z state and floating.

Power-On Power Supply Requirements

Xilinx FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time. The slowest ramp-up time is 50 ms. Current capacity is not specified for a ramp-up time faster than 2 ms. The current capacity varies linealy with ramp-up time, *e.g.*, an XQ4036XL with a ramp-up time of 25 ms would require a capacity predicted by the point on the straight line drawn from 1A at 120 µs to 500 mA at 50 ms at the 25 ms time mark. This point is approximately 750 mA .

Product	Description	Ramp-up Time	
		Fast (120 µs)	**Slow (50 ms)**
XQ4013 - 36XL	Minimum required current supply	1A	500 mA
XC4062XL	Minimum required current supply	2A	500 mA
XC4085XL(1)	Minimum required current supply	2A(1)	500 mA

Notes:
1. The XC4085XL fast ramp-up time is 5 ms.
2. Devices are guaranteed to initialize properly with the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
3. This specification applies to Commercial and Industrial grade products only.
4. Ramp-up Time is measured from $0V_{DC}$ to $3.6V_{DC}$. Peak current required lasts less than 3 ms, and occurs near the internal power on reset threshold voltage. After initialization and before configuration, I_{CC} max is less than 10 mA.

XQ4000XL AC Switching Characteristic

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

Global Buffer Switching Characteristics

Symbol	Description	Device	All	-3	-1	Units
			Min	Max	Max	
T_{GLS}	Delay from pad through Global Low Skew buffer, to any clock K	XQ4013XL	0.6	3.6	-	ns
		XQ4036XL	1.1	4.8	-	ns
		XQ4062XL	1.4	6.3	-	ns
		XQ4085XL	1.6	-	5.7	ns

Global Early BUFGEs 1, 2, 5, and 6 to IOB Clock Characteristics

Symbol	Description	Device	All	-3	-1	Units
			Min	Max	Max	
T_{GE}	Delay from pad through Global Early buffer, to any IOB clock. Values are for BUFGEs 1, 2, 5 and 6.	XQ4013XL	0.4	2.4	-	ns
		XQ4036XL	0.3	3.1	-	ns
		XQ4062XL	0.3	4.9	-	ns
		XQ4085XL	0.4	-	4.7	ns

Global Early BUFGEs 3, 4, 7, and 8 to IOB Clock Characteristics

Symbol	Description	Device	All	-3	-1	Units
			Min	Max	Max	
T_{GE}	Delay from pad through Global Early buffer, to any IOB clock. Values are for BUFGEs 3, 4, 7 and 8.	XQ4013XL	0.7	2.4	-	ns
		XQ4036XL	0.9	4.7	-	ns
		XQ4062XL	1.2	5.9	-	ns
		XQ4085XL	1.3	-	5.5	ns

XQ4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and expressed in nanoseconds unless otherwise noted.

CLB Switching Characteristics

Symbol	Description	-3		-1		Units
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.6	-	1.3	ns
T_{IHO}	F/G inputs via H' to X/Y outputs	-	2.7	-	2.2	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	2.9	-	2.2	ns
T_{HH0O}	C inputs via SR/H0 via H to X/Y outputs	-	2.5	-	2.0	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	2.4	-	1.9	ns
T_{HH2O}	C inputs via D_{IN}/H2 via H to X/Y outputs	-	2.5	-	2.0	ns
T_{CBYP}	C inputs via EC, D_{IN}/H2 to YQ, XQ output (bypass)	-	1.5	-	1.1	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.7	-	2.0	ns
T_{ASCY}	Add/subtract input (F3) to C_{OUT}	-	3.3	-	2.5	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	2.0	-	1.5	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.8	-	2.4	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.26	-	0.20	ns
T_{NET}	Carry net delay, C_{OUT} to C_{IN}	-	0.32	-	0.25	ns
Sequential Delays						
T_{CKO}	Clock K to flip-flop outputs Q	-	2.1	-	1.6	ns
T_{CKLO}	Clock K to latch outputs Q	-	2.1	-	1.6	ns
Setup Time Before Clock K						
T_{ICK}	F/G inputs	1.1	-	0.9	-	ns
T_{IHCK}	F/G inputs via H	2.2	-	1.7	-	ns
T_{HH0CK}	C inputs via H0 through H	2.0	-	1.6	-	ns
T_{HH1CK}	C inputs via H1 through H	1.9	-	1.4	-	ns
T_{HH2CK}	C inputs via H2 through H	2.0	-	1.6	-	ns
T_{DICK}	C inputs via D_{IN}	0.9	-	0.7	-	ns
T_{ECCK}	C inputs via EC	1.0	-	0.8	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	0.6	-	0.5	-	ns
T_{CCK}	C_{IN} input via F/G	2.3	-	1.9	-	ns
T_{CHCK}	C_{IN} input via F/G and H	3.4	-	2.7	-	ns

CLB Switching Characteristics *(Continued)*

Symbol	Description	-3		-1		Units
		Min	Max	Min	Max	
Hold Time After Clock K						
T_{CKI}	F/G inputs	0	-	0	-	ns
T_{CKIH}	F/G inputs via H	0	-	0	-	ns
T_{CKHH0}	C inputs via SR/H0 through H	0	-	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	0	-	ns
T_{CKHH2}	C inputs via D_{IN}/H2 through H	0	-	0	-	ns
T_{CKDI}	C inputs via D_{IN}/H2	0	-	0	-	ns
T_{CKEC}	C inputs via EC	0	-	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	0	-	ns
Clock						
T_{CH}	Clock High time	3.0	-	2.5	-	ns
T_{CL}	Clock Low time	3.0	-	2.5	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	3.0	-	2.5	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.7	-	2.8	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	-	19.8	-	15.0	ns
T_{MRQ}	Delay from GSR input to any Q	See page 95 for T_{RRI} values per device.				
F_{TOG}	Toggle frequency (MHz) (for export control)	-	166	-	200	MHz

2

XQ4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and are expressed in nanoseconds unless otherwise noted.

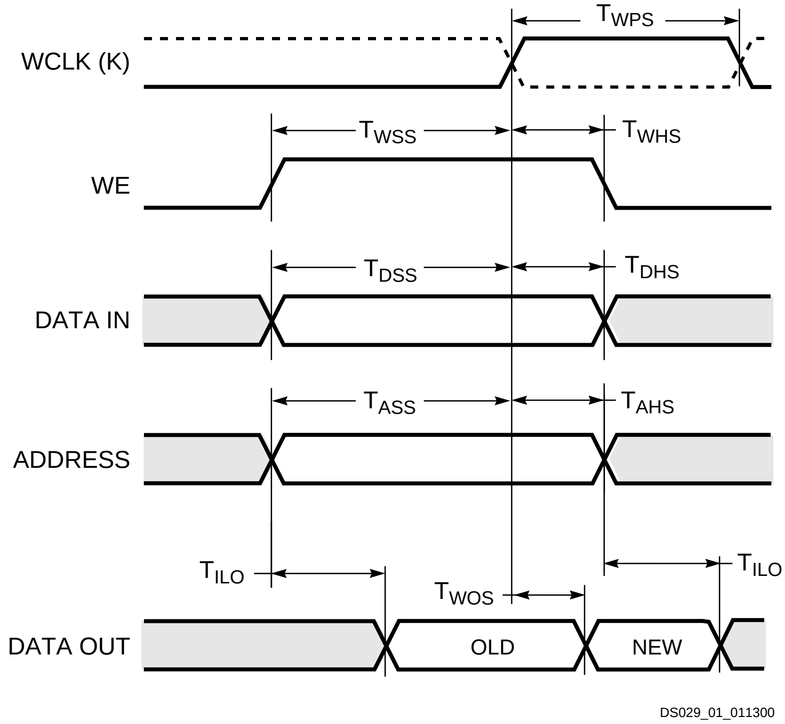
Single-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Single Port RAM	Size	-3		-1		Units
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	9.0	-	7.7	-	ns
T_{WCTS}		32x1	9.0	-	7.7	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.5	-	3.9	-	ns
T_{WPTS}		32x1	4.5	-	3.9	-	ns
T_{ASS}	Address setup time before clock K	16x2	2.2	-	1.7	-	ns
T_{ASTS}		32x1	2.2	-	1.7	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	0	-	ns
T_{AHTS}		32x1	0	-	0	-	ns
T_{DSS}	D_{IN} setup time before clock K	16x2	2.0	-	1.7	-	ns
T_{DSTS}		32x1	2.5	-	2.1	-	ns
T_{DHS}	D_{IN} hold time after clock K	16x2	0	-	0	-	ns
T_{DHTS}		32x1	0	-	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.0	-	1.6	-	ns
T_{WSTS}		32x1	1.8	-	1.5	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	0	-	ns
T_{WHTS}		32x1	0	-	0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.8	-	5.8	ns
T_{WOTS}		32x1	-	8.1	-	6.9	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	4.5	-	2.6	-	ns
T_{RCT}		32x1	6.5	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.6	-	1.3	ns
T_{IHO}		32x1	-	2.7	-	2.2	ns
T_{ICK}	Address setup time before clock K	16x2	1.1	-	0.9	-	ns
T_{IHCK}		32x1	2.2	-	1.7	-	ns

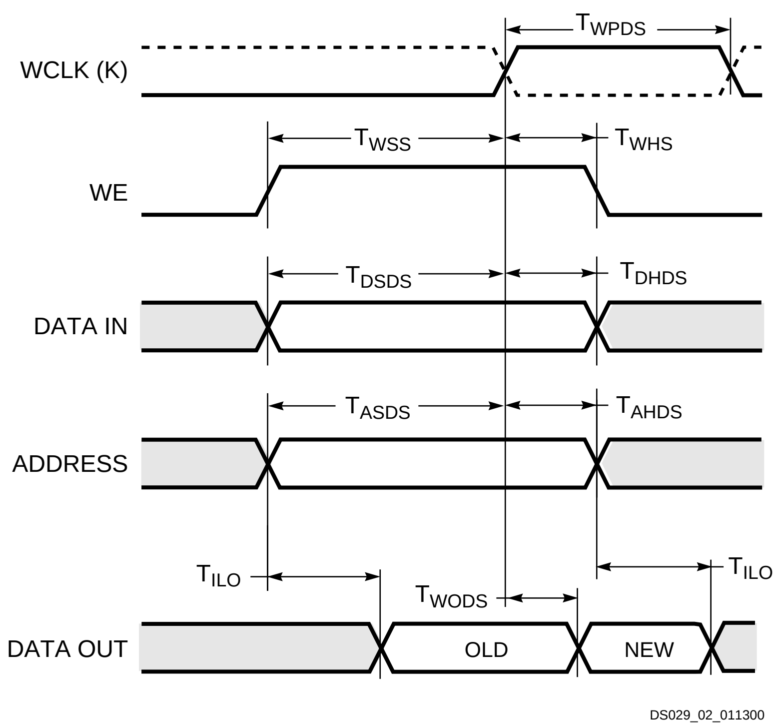
Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Dual Port RAM	Size(1)	-3		-1		Units
			Min	Max	Min	Max	
Write Operation							
T_{WCDS}	Address write cycle time (clock K period)	16x1	9.0		7.7		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	4.5	-	3.9	-	ns
T_{ASDS}	Address setup time before clock K	16x1	2.5	-	1.7	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T_{DSDS}	D_{IN} setup time before clock K	16x1	2.5	-	2.0	-	ns
T_{DHDS}	D_{IN} hold time after clock K	16x1	0	-	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.8	-	1.6	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	7.8	-	6.7	ns

XQ4000XL CLB Single-Port RAM Synchronous (Edge-Triggered) Write Timing



XQ4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



XQ4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Output Flip-Flop, Clock to Out[1,2,3]

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{ICKOF}	Global low skew clock to output using OFF[4]	XQ4013XL	1.5	8.6	-	ns
		XQ4036XL	2.0	9.8	-	ns
		XQ4062XL	2.3	11.3	-	ns
		XQ4085XL	2.5	-	9.5	ns
T_{SLOW}	For output SLOW option add	All Devices	3.0	3.0	3.0	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
3. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
4. OFF = Output Flip-Flop

Output Flip-Flop, Clock to Out, BUFGEs 1, 2, 5, and 6

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{ICKEOF}	Global early clock to output using OFF Values are for BUFGEs 1, 2, 5, and 6.	XQ4013XL	1.3	7.4	-	ns
		XQ4036XL	1.2	8.1	-	ns
		XQ4062XL	1.2	9.9	-	ns
		XQ4085XL	1.3	-	8.5	ns

Notes:

1. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Output Flip-Flop, Clock to Out, BUFGEs 3, 4, 7, and 8

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{ICKEOF}	Global early clock to output using OFF Values are for BUFGEs 3, 4, 7, and 8.	XQ4013XL	1.8	8.8	-	ns
		XQ4036XL	1.8	9.7	-	ns
		XQ4062XL	2.0	10.9	-	ns
		XQ4085XL	2.2	-	9.3	ns

Notes:
1. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

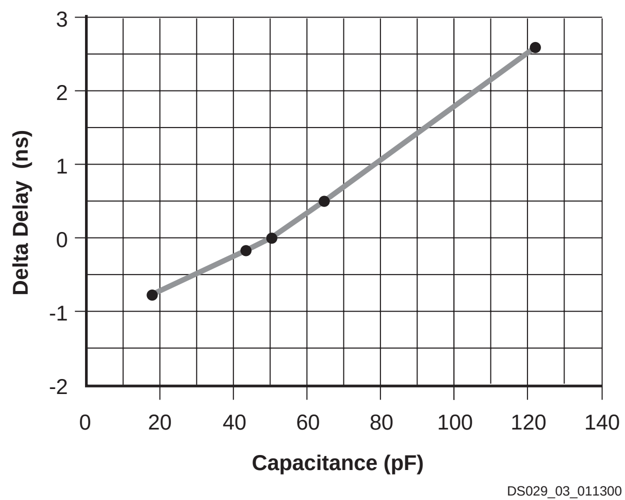


Figure 1: **Delay Factor at Various Capacitive Loads**

XQ4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Global Low Skew Clock, Input Setup and Hold Times[1,2]

2

Symbol	Description	Device[1]	-3 Min	-1 Min	Units
No Delay					
T_{PSN}/T_{PHN}	Global early clock and IFF[3] Global early clock and FCL[4]	XQ4013XL	1.2 / 3.2	-	ns
		XQ4036XL	1.2 / 5.5	-	ns
		XQ4062XL	1.2 / 7.0	-	ns
		XQ4085XL	-	0.9 / 7.1	ns
Partial Delay					
T_{PSP}/T_{PHP}	Global early clock and IFF[3] Global early clock and FCL[4]	XQ4013XL	6.1 / 0.0	-	ns
		XQ4036XL	6.4 / 1.0	-	ns
		XQ4062XL	6.7 / 1.2	-	ns
		XQ4085XL	-	9.8 / 1.2	ns
Full Delay					
T_{PSD}/T_{PHD}	Global early clock and IFF[3]	XQ4013XL	6.4 / 0.0	-	ns
		XQ4036XL	6.6 / 0.0	-	ns
		XQ4062XL	6.8 / 0.0	-	ns
		XQ4085XL	-	9.6 / 0.0	ns

Notes:
1. The XQ4013XL, XQ4036XL, and XQ4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

Global Early Clock BUFEs 1, 2, 5, and 6 Setup and Hold for IFF and FCL[1,2]

Symbol	Description	Device	-3	-1
			Min	Min
No Delay				
T_{PSEN}/T_{PHEN} T_{PFSEN}/T_{PFHEN}	Global early clock and IFF[3] Global early clock and FCL[4]	XQ4013XL	1.2 / 4.7	-
		XQ4036XL	1.2 / 6.7	-
		XQ4062XL	1.2 / 8.4	-
		XQ4085XL	-	0.9 / 6.6
Partial Delay				
T_{PSEPN}/T_{PHEP} T_{PFSEP}/T_{PFHEP}	Global early clock and IFF[3] Global early clock and FCL[4]	XQ4013XL	6.4 / 0.0	-
		XQ4036XL	7.0 / 0.8	-
		XQ4062XL	9.0 / 0.8	-
		XQ4085XL	-	11.0 / 0.0
Full Delay				
T_{PSEPD}/T_{PHED}	Global early clock and IFF[3]	XQ4013XL	12.0 / 0.0	-
		XQ4036XL	13.8 / 0.0	-
		XQ4062XL	13.1 / 0.0	-
		XQ4085XL	-	13.6 / 0.0

Notes:
1. The XQ4013XL, XQ4036XL, and XQ4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

Global Early Clock BUFEs 3, 4, 7, and 8 Setup and Hold for IFF and FCL[1,2]

Symbol	Description	Device	-3	-1
			Min	Min
No Delay				
T_{PSEN}/T_{PHEN}	Global early clock and IFF[3]	XQ4013XL	1.2 / 4.7	-
T_{PFSEN}/T_{PFHEN}	Global early clock and FCL[4]	XQ4036XL	1.2 / 6.7	-
		XQ4062XL	1.2 / 8.4	-
		XQ4085XL	-	0.9 / 6.6
Partial Delay				
T_{PSEPN}/T_{PHEP}	Global early clock and IFF[3]	XQ4013XL	5.4 / 0.0	-
T_{PFSEP}/T_{PFHEP}	Global early clock and FCL[4]	XQ4036XL	6.4 / 0.8	-
		XQ4062XL	8.4 / 1.5	-
		XQ4085XL	-	11.0 / 0.0
Full Delay				
T_{PSEPD}/T_{PHED}	Global early clock and IFF[3]	XQ4013XL	10.0 / 0.0	-
		XQ4036XL	12.2 / 0.0	-
		XQ4062XL	13.1 / 0.0	-
		XQ4085XL	-	13.6 / 0.0

Notes:
1. The XQ4013XL, XQ4036XL, and XQ4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

2

XQ4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	-3		-1		Units
			Min	Max	Min	Max	
Clocks							
T_{ECIK}	Clock enable (EC) to clock (IK)	All devices	0.1	-	0.1	-	ns
T_{OKIK}	Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	All devices	2.2	-	1.6	-	ns
Setup Times							
T_{PICK}	Pad to clock (IK), no delay	All devices	1.7	-	1.3	-	ns
T_{PICKF}	Pad to clock (IK), via transparent fast capture latch, no delay	All devices	2.3	-	1.8	-	ns
T_{POCK}	Pad to fast capture latch enable (OK), no delay	All devices	1.2	-	0.9	-	ns
Hold Times							
	All Hold Times	All devices	0	-	0	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	-	19.8	-	15.0	ns
T_{RRI}	Delay from GSR input to any Q(2)	XQ4013XL	-	15.9	-	-	ns
		XQ4036XL	-	22.5	-	-	ns
		XQ4062XL	-	29.1	-	-	ns
		XQ4085XL	-	-	-	26.0	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	1.6	-	1.7	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	3.1	-	2.4	ns
T_{PFLI}	Pad to I1, I2 via transparent FCL and input latch, no delay	All devices	-	3.7	-	2.8	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.7	-	1.3	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.8	-	1.4	ns
T_{OKLI}	FCL enable (OK) active edge to I1, I2 (via transparent standard input latch)	All devices	-	3.6	-	2.7	ns

Notes:
1. IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch
2. Indicates Minimum Amount of Time to Assure Valid Data.

XQ4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	-3		-1		Units
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High	3.0	-	2.5	-	ns
T_{CL}	Clock Low	3.0	-	2.5	-	ns
Propagation Delays						
T_{OKPOF}	Clock (OK) to pad	-	5.0	-	3.8	ns
T_{OPF}	Output (O) to pad	-	4.1	-	3.1	ns
T_{TSHZ}	High-Z to pad High-Z (slew-rate independent)	-	4.4	-	3.0	ns
T_{TSONF}	High-Z to pad active and valid	-	4.1	-	3.3	ns
T_{OFPF}	Output (O) to pad via fast output MUX	-	5.5	-	4.2	ns
T_{OKFPF}	Select (OK) to pad via fast MUX	-	5.1	-	3.9	ns
Setup and Hold Times						
T_{OOK}	Output (O) to clock (OK) setup time	0.5	-	0.3	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	0	-	0	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	0.3	-	0.1	-	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	19.8	-	15.0	-	ns
T_{RPO}	Delay from GSR input to any pad(2)					
	XQ4013XL	-	20.5	-	-	ns
	XQ4036XL	-	27.1	-	-	ns
	XQ4062XL	-	33.7	-	-	ns
	XQ4085XL	-		-	29.5	ns
Slew Rate Adjustment						
T_{SLOW}	For output SLOW option add	-	3.0	-	2.0	ns

Notes:
1. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.
2. Indicates Minimum Amount of Time to Assure Valid Data.

CB228 Pinouts

Table 2: **CB228 Package Pinouts**

Pin Name	CB228
VTT	
GND	P1
BUFGP_TL_A16_GCK1_IO	P2
A17_IO	P3
IO	P4
IO	P5
TDI_IO	P6
TCK_IO	P7
IO	P8
IO	P9
IO	P10
IO	P11
IO	P12
IO	P13
GND	P14
IO_FCLK1	P15
IO	P16
TMS_IO	P17
IO	P18
IO	P19
IO	P20
IO	P21
IO	P22
IO	P23
IO	P24
IO	P25
IO	P26
GND	P27
V_{CC}	P28
IO	P29
IO	P30
IO	P31
IO	P32
IO	P33
IO	P34
IO	P35
IO	P36
V_{CC}	P37
IO	P38

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P39
IO	P40
IO_FCLK2	P41
GND	P42
IO	P43
IO	P44
IO	P45
IO	P46
IO	P47
IO	P48
IO	P49
IO	P50
IO	P51
IO	P52
IO	P53
BUFGS_BL_GCK2_IO	P54
M1	P55
GND	P56
M0	P57
V_{CC}	P58
M2	P59
BUFGP_BL_GCK3_IO	P60
HDC_IO	P61
IO	P62
IO	P63
IO	P64
LDC_IO	P65
IO	P66
IO	P67
IO	P68
IO	P69
IO	P70
IO	P71
GND	P72
IO	P73
IO	P74
IO	P75
IO	P76
IO	P77
IO	P78

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P79
IO	P80
IO	P81
IO	P82
IO	P83
/ERR_INIT_IO	P84
V_{CC}	P85
GND	P86
IO	P87
IO	P88
IO	P89
IO	P90
IO	P91
IO	P92
IO	P93
IO	P94
V_{CC}	P95
IO	P96
IO	P97
IO	P98
IO	P99
GND	P100
IO	P101
IO	P102
IO	P103
IO	P104
IO	P105
IO	P106
IO	P107
IO	P108
IO	P109
IO	P110
IO	P111
BUFGS_BR_GCK4_IO	P112
GND	P113
DONE	P114
V_{CC}	P115
/PROGRAM	P116
D7_IO	P117
BUFGP_BR_GCK5_IO	P118

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P119
IO	P120
IO	P121
IO	P122
D6_IO	P123
IO	P124
IO	P125
IO	P126
IO	P127
IO	P128
GND	P129
IO	P130
IO	P131
IO_FCLK3	P132
IO	P133
D5_IO	P134
/CS0_IO	P135
IO	P136
IO	P137
IO	P138
IO	P139
D4_IO	P140
IO	P141
V_{CC}	P142
GND	P143
D3_IO	P144
/RS_IO	P145
IO	P146
IO	P147
IO	P148
IO	P149
D2_IO	P150
IO	P151
V_{CC}	P152
IO	P153
IO_FCLK4	P154
IO	P155
IO	P156
GND	P157
IO	P158

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P159
IO	P160
IO	P161
IO	P162
IO	P163
D1_IO	P164
BUSY_/RDY_RCLK_IO	P165
IO	P166
IO	P167
D0_DIN_IO	P168
BUFGS_TR_GCK6_DOUT_IO	P169
CCLK	P170
V_{CC}	P171
TDO	P172
GND	P173
A0_/WS_IO	P174
BUFGP_TR_GCK7_A1_IO	P175
IO	P176
IO	P177
CSI_A2_IO	P178
A3_IO	P179
IO	P180
IO	P181
IO	P182
IO	P183
IO	P184
IO	P185
GND	P186
IO	P187
IO	P188
IO	P189
IO	P190
V_{CC}	P191
A4_IO	P192
A5_IO	P193
IO	P194
IO	P195
A21_IO	P196
A20_IO	P197
A6_IO	P198

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
A7_IO	P199
GND	P200
V_{CC}	P201
A8_IO	P202
A9_IO	P203
A19_IO	P204
A18_IO	P205
IO	P206
IO	P207
A10_IO	P208
A11_IO	P209
V_{CC}	P210
IO	P211
IO	P212
IO	P213
IO	P214
GND	P215
IO	P216
IO	P217
IO	P218
IO	P219
A12_IO	P220
A13_IO	P221
IO	P222
IO	P223
IO	P224
IO	P225
A14_IO	P226
BUFGS_TL_GCK8_A15_IO	P227
V_{CC}	P228

Ordering Information

Example for QPRO™ military temperature part:

XQ 4062XL -3 PG 475 M

Mil-PRF-38535 (QML) Processed

Device Type
XQ4085XL
XQ4062XL
XQ4036XL
XQ4013XL

Speed Grade
-3
-1 (XQ4085XL only)

Package Type
CB = Top Brazed Ceramic Quad Flat Pack
PG = Ceramic Pin Grid Array
PQ/HQ = Plastic Quad Flat Back
BG = Plastic Ball Grid Array

Number of Pins

Temperature Range
M = Military Ceramic (T_C = –55°C to +125 °C)
N = Military Plastic (T_J = –55°C to +125°C)

2

Example for SMD part:

5962 98511 01 Q X C

Generic Standard Microcircuit Drawing (SMD) Prefix

Device Type
XQ4013XL = 98513
XQ4036XL = 98510
XQ4062XL = 98511
XQ4085XL = 99575

Speed Grade
01 = -3 for XQ4103XL/4036XL/4062XL
01 = -1 for XQ4085XL

Q = QML Certified
N = QML Plastic (N - Grade)

Package Type
X = Pin Grid
Y = Ceramic Quad Flat Pack (Base Mark)
Z = Ceramic Quad Flat Pack (Lid Mark)
T = Plastic Quad Flat Pack
U = Plastic Ball Grid

Lead Finish
C = Gold
B = Solder

Revision History

The following table shows the revision history for this document

Date	Version	Description
05/01/98	1.0	Original document release.
01/01/99	1.1	Addition of new packages, clarification of parameters.
02/09/00	1.2	Addition of XQ4085XL-1 speed grade part.
06/25/00	1.3	Updated timing specifications to match with commercial data sheet. Updated format.