ANALOG DEVICES

Low Power PCM Repeaters

RPT-86/RPT-87

FEATURES

- **Low Power Consumption (56mW)**
- **Single-Supply Operation**
- **Wide Data Rate Range <100kbit/s to >3Mbit/s**
- **Dual ALBO Diodes; Dynamic Range >50dB**
- **Clock-Shutdown Circuit (RPT-87)**

ORDERING INFORMATION†

PACKAGE			OPERATING TEMPERATURE
CERDIP	PLASTIC	SO	RANGE
RPT86FQ	RPT86FP	RPT86FS††	XIND
RPT87FQ	RPT87FP	RPT87FS††	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

GENERAL DESCRIPTION

The RPT-86 and RPT-87 are monolithic repeater circuits containing all the active functions required in regenerative PCM repeaters. These devices automatically adjust gain to optimize signal levels, determine if a pulse is present, and re-transmit the reconstructed pulses. The RPT-86 and RPT-87 operate at data rates from under 100kbit/s to over 3Mbit/s and are compatible with T1 (1.544Mbit/s), CEPT/E1 (2.048Mbit/s), and T1C (3.152Mbit/s) systems.

A key feature of the RPT-86/RPT-87 repeaters is the ability to operate on a single supply of 5.6V with a typical quiescent supply current of only 10mA. In addition, the RPT-86 and RPT-87 have two Automatic Line Build-Out (ALBO) diodes coupled with a high-gain preamplifier that allows for a dynamic input signal range exceeding 50dB.

The RPT-87 also contains a clock-shutdown circuit. This shutdown circuit senses the incoming signal level and disables the clock drive to the output latches if the incoming signal is below the level where accurate pulse reconstruction is possible. This prevents noise or crosstalk from being mistaken as valid data and retransmitted.

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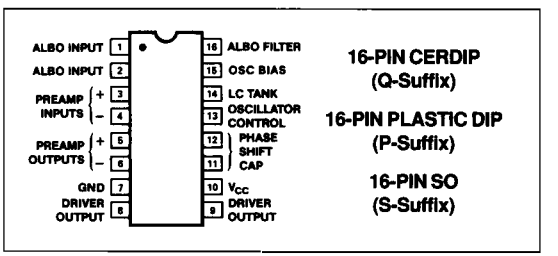
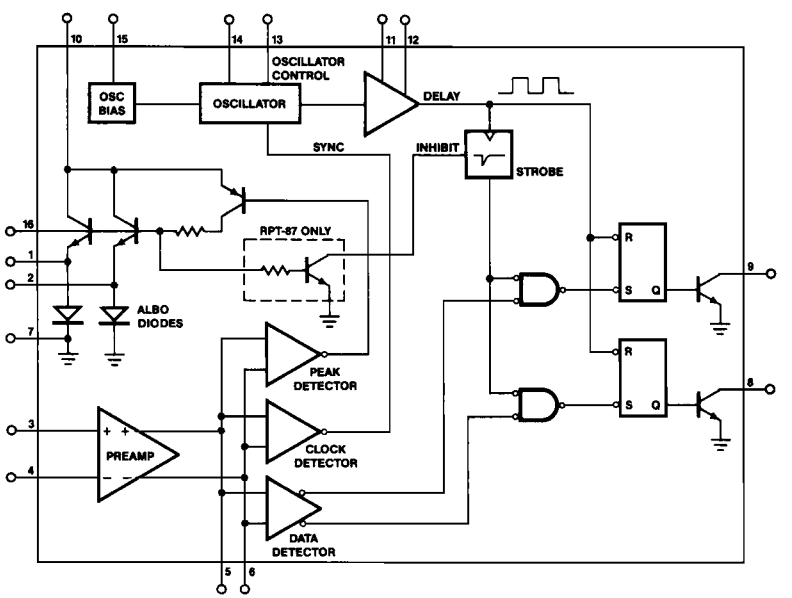
PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Pin 10 to Pin 7, 20ms Pulse, Duty Cycle ≤0.05 ..... 35V, –1.0V
Voltage Pin 10 to Pin 7, Continuous 50Hz Half-Wave Sinusoid ..... 25V, –1.0V
Pin 10 to Pin 7, Continuously ..... 13.5V, –0.7V
Voltage Pins 8 or 9 to Pin 7, Continuously ..... 35V, –1.0V
Voltage Pins 3,4,5,6,11,12,14 to Pin 7 ..... V_{CC}
Sinking Current at Pin 8 or 9 ..... 300mA
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Soldering Temperature ..... 300°C
Junction Temperature ..... 150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
16-Pin SO (S)	111	35	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_{CC} = 5.6V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. $V_{PIN\ 7}$ = $V_{PIN\ 13}$ = GND.

PARAMETER	SYMBOL	CONDITIONS	RPT-86F/RPT-87F MIN	TYP	MAX	UNITS
SUPPLY						
Supply Current	I_{CC}	(Note 1)	5	9.8	10.5	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain	A_O		46	49	54	dB
Preamplifier Bandwidth	B_W	–3dB (Note 3)	3	5	–	MHz
Preamplifier Input Impedance, Differential	Z_{IN}	f = 1.544 MHz	–	50	–	kΩ
Preamplifier Input Offset Voltage	V_{OS}	(Note 1)	–	0.5	2.5	mV
Preamplifier Output Impedance	Z_{OUT}	(Note 2)	–	200	300	Ω
Preamplifier Output High	V_{OHA}	T_A = +25°C	3.30	3.50	–	V
Preamplifier Output Low	V_{OLA}	T_A = +25°C	–	1.20	1.45	V
Preamplifier Input Bias Current	I_B	(Note 1)	–	1	4	µA
Preamplifier Input Offset Current	I_{OS}	(Note 1)	–	0.01	0.1	µA
Preamplifier Output Self-Bias Voltage	V_{DC}	T_A = +25°C (Note 1)	2.35	2.45	2.60	V
OUTPUT DRIVE						
Output Voltage Low	V_{OL}	I_{LOAD} = 20mA	0.65	0.85	1.05	V
Differential Output Voltage, Low	V_{OLD}	I_{LOAD} = 20mA	–	0.02	0.1	V
Output Leakage Current	I_{OH}	$V_{PIN\ 14}$ = 4.9V, $V_{PIN\ 8}$ = $V_{PIN\ 9}$ = 20V (Note 1)	–	0.05	50	µA
Output Pulse Rise-Time	T_{OR}	(Note 2)	–	30	50	ns
Output Pulse Fall-Time	T_{OF}	(Note 2)	–	10	60	ns
Output Pulse Width	P_W	f = 1.544MHz	–	324	–	ns
Pulse-Width Differential	P_{WD}	(Note 2)	–	3	12	ns
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I_{TB}	$I_{PIN\ 14}$, $V_{PIN\ 14}$ = 4.9V (Note 1)	–	3	10	µA

ELECTRICAL CHARACTERISTICS at V_{CC} = 5.6V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted. $V_{PIN\ 7} = V_{PIN\ 13}$ = GND. *Continued*

PARAMETER	SYMBOL	CONDITIONS	RPT-86F/RPT-87F MIN	TYP	MAX	UNITS
Oscillator Bias Current	I_{OSC}	$V_{PIN\ 14}$ = 3.9V, ($I_{OSC} - I_{TB}$) (Note 1)	10	30	50	µA
Oscillator Injection Current	I_{INJ}	Set $V_{PIN\ 6} - V_{PIN\ 5}$ = ±1.4V, $V_{PIN\ 14}$ = 3.9V, ($I_{INJ} - I_{OSC}$)	80	110	140	µA
Data Sampling Interval	T_{DS}	(Note 3)	–	70	95	ns
Delay Circuit Resistor	R_d	Measured from pin 11, or pin 12 to pin 15 T_A = +25°C	3.6	4.4	5.2	kΩ
Oscillator Bias Voltage	V_{BIAS}	$V_{PIN\ 15}$	–	4.4	–	V
ALBO						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 6 and 5, required to activate the Peak Detector.	1.25	1.45	1.65	V
ALBO Threshold ± Differential	V_{TAD}		–	–	100	mV
ALBO ON Voltage	V_{O16}	Measured at pin 16, [$V_{PIN\ 6} - V_{PIN\ 5}$] = ALBO Threshold + 20mV	1.0	1.6	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16, pin 1, and pin 2 (Note 1)	–	–	75	mV
Minimum ALBO Diode Resistance	R_D MIN	Forced ΔI of 6 mA to 7 mA, measure voltage at pins 1 and 7, Calculate R_D by 1/2.	–	6	10	Ω
Maximum ALBO Diode Resistance	R_D MAX	f = 1.544MHz (Note 4)	20	30	–	kΩ
ALBO Diode Impedance Matching		$R_{DMIN} \leq R_D \leq R_{DMAX}$	–	10	–	%
DATA / CLOCK THRESHOLDS						
Clock Threshold	V_{TC}	Differential voltage, measured between pins 6 and 5, required to activate the Clock Detector.	0.85	1.0	1.15	V
Clock Threshold as % of ALBO Voltage	$V_{TC\%}$		63	69	75	%
Data Threshold	V_{TL}	Differential voltage, measured between pins 6 and 5, required to activate the Data Detector.	0.65	0.75	0.85	V
Data Threshold as % of ALBO Voltage	$V_{TL\%}$		46	51	56	%

NOTES:
1. Preamplifier self-biased. $V_{PIN\ 3} \cong V_{PIN\ 4} \cong V_{PIN\ 5} \cong V_{PIN\ 6}$.
2. Sample tested.
3. Guaranteed by correlation to other tested parameters.
4. Guaranteed by design.

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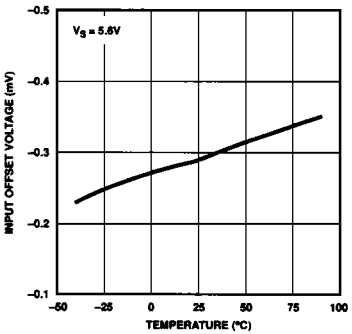
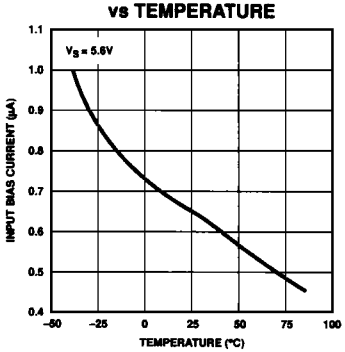
TYPICAL PERFORMANCE CHARACTERISTICS

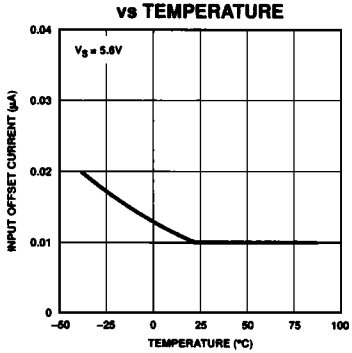
INPUT OFFSET VOLTAGE vs TEMPERATURE



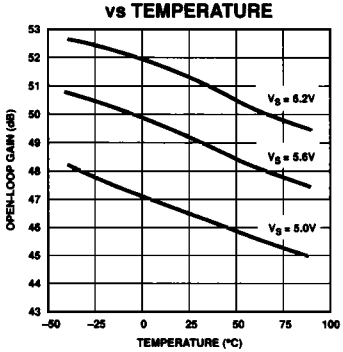
INPUT BIAS CURRENT vs TEMPERATURE



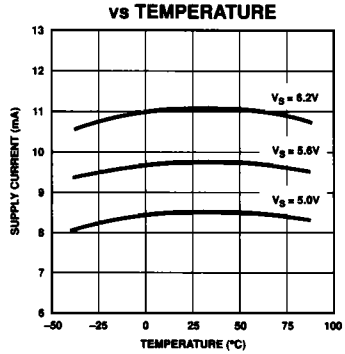
INPUT OFFSET CURRENT vs TEMPERATURE



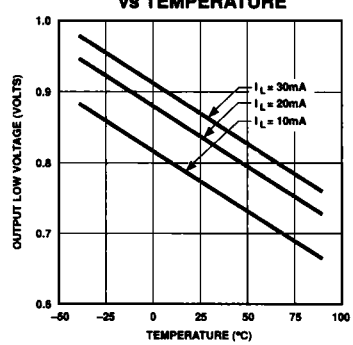
OPEN-LOOP GAIN vs TEMPERATURE



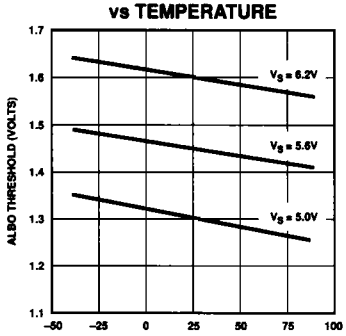
SUPPLY CURRENT vs TEMPERATURE



OUTPUT LOW VOLTAGE (V_{OL}) vs TEMPERATURE



ALBO THRESHOLD vs TEMPERATURE



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The Preamplifier: The RPT-86 and RPT-87 repeater ICs contain a differential input, differential output preamplifier. From the differential input to the noninverting output, it behaves as a conventional op amp. The preamplifier has typically 5MHz, –3dB bandwidth. Its open-loop gain-phase frequency response is shown in Figure 1. In order to operate the preamplifier under a stable condition, some amount of external feedback is necessary to control the frequency response. The open-loop frequency response suggests that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

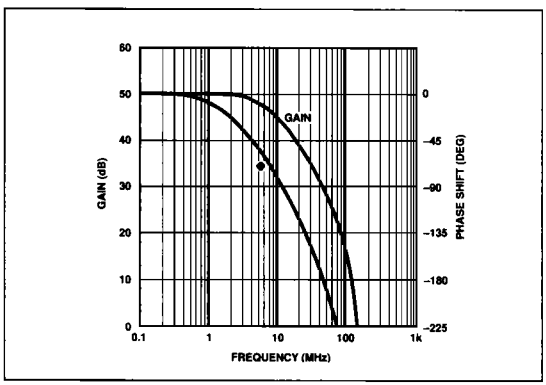


FIGURE 1: *Gain-Phase Frequency Response of the Preamplifier*

TABLE 1: Typical Preamp Gain/Phase Response

FREQUENCY (MHz)	AVOL(dB)	PHASE(DEG)
1.0	50	–12
1.544	50	–20
6.2	47	–60
20	39	–119
25.3	36.3	–135
45	29.5	–180

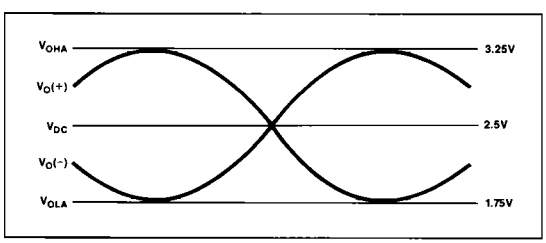


FIGURE 2: *The differential outputs of the RPT-86/87 preamplifier swing symmetrically around a DC bias point of about 2.5V. $V_O^{(-)}$ is inverted with respect to $V_O^{(+)}$ about this point.*

The RPT-86/87's preamp is designed to operate around a balanced DC common-mode bias level roughly equal to 2.5V on both its inputs and outputs. This allows the outputs to achieve maximum swing when amplifying an AC-coupled, bipolar signal. It also produces zero differential preamp output voltage for zero input signal. Operating from a +5.6V supply, the preamp outputs will balance at approximately +2.5V allowing an output voltage swing of ±0.75V around its bias level as illustrated in Figure 2.

Figures 3 and 4 show two methods of configuring the preamp to automatically self-bias both the inputs and outputs to an optimum level. The single resistor and capacitor used in Figure 3 extracts the DC average of the inverting output and feeds it back to the noninverting input to establish the input common-mode level. This negative feedback will force the outputs to center their swing around the DC level at which V_O(Diff) = 0V. This type of self-biasing is practical only when the preamp is passing a balanced, AC coupled, bipolar signal. If the preamp must preserve the DC level of an unbalanced, unipolar signal, then a self-biasing scheme as is shown in Figure 4 is required. This network sets the input common-mode level by establishing the DC average of both differential outputs. In this way, the input common-mode level will always be that voltage at which V_O(Diff) = 0V regardless of the input signal.

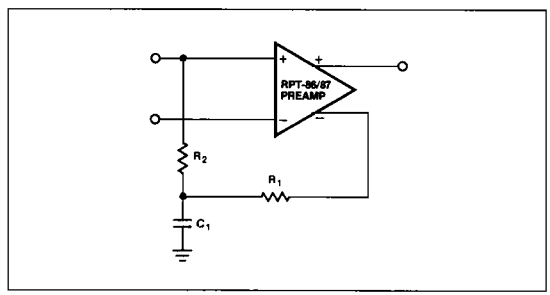


FIGURE 3: *Preamp self-biasing for use with AC coupled, balanced bipolar signals.*

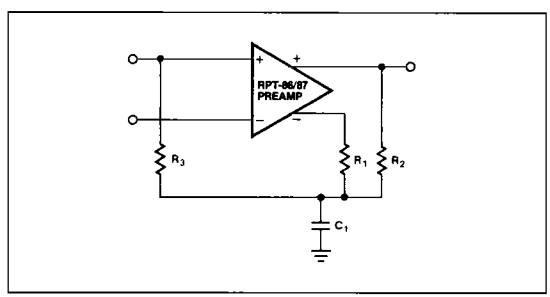


FIGURE 4: *Universal preamplifier self-biasing technique allowing unipolar signal amplification.*

Threshold Comparators: The RPT-86/87 contains three pairs of threshold comparators to monitor the differential outputs of the preamplifier. Each of the six comparators is set to detect a specific differential preamp output level. Three comparators measure positive differentials and three measure negative differentials. The individual threshold comparators are labeled as positive and negative Peak, Clock, and Data detector, as shown in Figure 5.

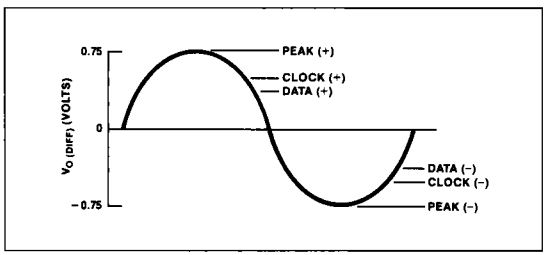


FIGURE 5: *Six threshold comparators detect positive and negative differential preamp output levels.*

The data Detector thresholds are set at 50% of the Peak levels for maximum noise immunity. The outputs of these comparators contain the digital data and are presented to the output R-S flip-flops. The Clock Detector thresholds are set at 70% of the Peak levels. When the Clock thresholds are reached, the comparators send a synchronization pulse to the on-board oscillator to lock its frequency and phase to that of the incoming signal. The peak detectors trip when the signal exceeds the peak thresholds. Peak Detector outputs are used to perform an AGC function to maintain a constant preamp peak output level. Thresholds and waveforms are shown in Figure 6.

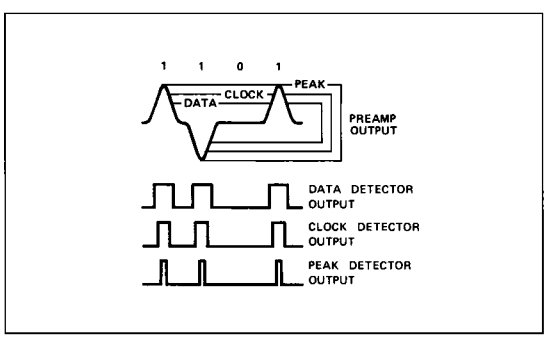


FIGURE 6: *Comparator Thresholds and Waveforms*

ALBO: The ALBO function is driven from the Peak threshold detector outputs. The ALBO (Automatic Line Build-Out) circuitry consists of two current-driven diodes which act as variable impedance elements enabling the RPT-86/87 to close an AGC loop around the preamplifier. As a peak level is detected, a current pulse is sourced into the ALBO diodes. These pulses are averaged to a DC current by an external ALBO filter capacitor. As the current flowing through the diodes increases, their incremental impedance is lowered as described by the exponential I-V curve for a diode-connected NPN transistor shown in Figure 7. The impedance of the NPN transistor emitters which source the current to the ALBO diodes follows an identical curve. Because the bases of these transistors look like an AC short to ground by virtue of the external ALBO filter capacitor, the total AC impedance of each ALBO port looks like the parallel combination of two diodes.

Equation 1: $R_D \cong \frac{0.026V}{2I_D} + R_{STRAY}$

where I_D is equal to the DC current flowing through the diodes and R_{STRAY} represents the stray resistance inherent in the RPT-86/87, about 3Ω.

The longer a peak level is detected, the greater I_D becomes, lowering R_D. When no peak levels are detected, the voltage on the ALBO filter capacitor becomes zero, shutting off current to the diodes. Under this condition, the stray pin capacitance of about 3pF will limit maximum ALBO impedance. A 1.544MHz signal will see an effective port ALBO impedance of about 30kΩ.

In the RPT-87 only, a low voltage at the ALBO filter enables a clock-shutdown circuit when there is no input signal. The clock-shutdown circuit disables the clock strobe, preventing it from latching the output flip-flops. This prevents the RPT-87 from sending false data that is triggered by noise or crosstalk when the incoming signal level is too low.

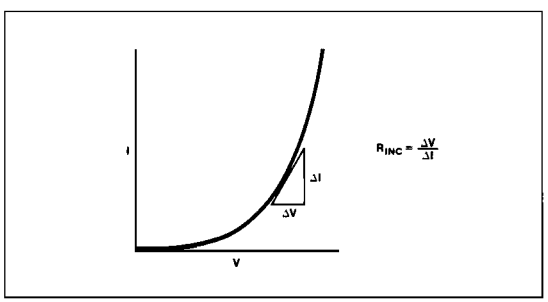


FIGURE 7: *The incremental impedance of the diode-connected NPN transistor used as the ALBO diode is dependent on the DC bias current flowing through it.*

The Oscillator: The RPT-86/87's on-board oscillator is designed to be free-running at a frequency, f_o, set by an external inductor and capacitor across pins 14 and 15, where $f_o = 1/(2\pi\sqrt{LC})$. The phase and exact frequency of the oscillator are synchronized to the incoming data signal by the Clock threshold comparators. Each time the preamplifier's differential output exceeds the Clock thresholds, the comparator's outputs inject a current pulse into the LC tank oscillator aligning its oscillation with the incoming signal. During periods where no Clock levels are detected by the comparators, the LC tank's oscillation will relax back to its own resonant frequency. An internal comparator is used to square the LC tank's sinusoidal oscillation into digital level clock. This comparator incorporates a delay function (a capacitor across pins 11 and 12) that provides additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses, thus allowing the user to control when the clock strobe will reach the output latches.This provides optimum timing for determining if a "1" or a "0" is present. A 0 to 30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

Data Output: When the incoming signal is detected as valid data, it is strobed into the two output R-S flip-flops. Their respective outputs are open-collector drivers that allows driving directly into a center-tapped isolation transformer. This recreates a full amplitude bipolar, AMI signal and transmits it down the next length of transmission line.

DESIGNING WITH THE RPT-86 AND RPT-87

DESIGNING A WIDEBAND AMPLIFIER

Figure 8 shows a typical configuration using the RPT-86/87's preamplifier to create a high-gain, wideband amplifier. The capacitor C_1 determines the amplifier's low frequency gain roll-off while resistors R_1 and R_2 set the AC closed-loop gain. At DC, the amplifier is in unity gain. A zero at $\omega_1 = 1/(R_2C_1)$ causes the AC gain to rise until a pole is reached at $\omega_2 = 1/(R_1C_2)$. The final value of closed-loop signal gain is equal to:

$$\text{Equation 2: } A_{VCL} = \frac{A_{VOL}}{1 + \left(\frac{A_{VOL}\,R_1}{R_2}\right)}$$

To ensure preamp stability, the ratio R_2/R_1 must be a minimum of 100 to a bandwidth of at least 20MHz. Low value resistors should be used for R_2 and R_1 to minimize the effects of stray capacitance in the feedback loop. Since PC board applications exhibit at least 2pF of stray feedback capacitance (equal to about 4kΩ impedance at 20MHz), R_1 should be less than 40Ω.

Because the preamp's differential output voltage is monitored by the internal threshold comparators, any output offset will degrade the symmetry of positive and negative threshold levels. Operating the preamplifier in DC unity gain is instrumental in minimizing the output offset voltage. Offset can be further reduced by balancing the preamp's DC input source impedance.

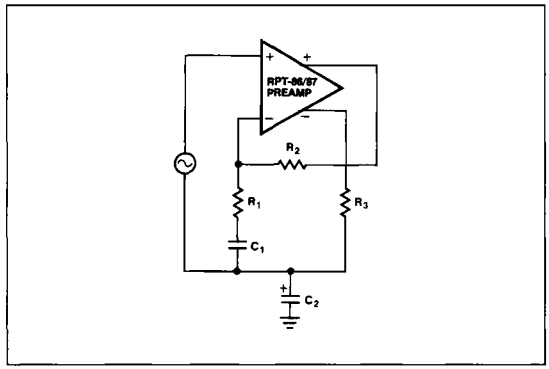


FIGURE 8: *Typical noninverting preamplifier gain configuration with self-biasing.*

Preamp output loading in the form of feedback and biasing networks should also be balanced to ensure uniform inverting action between the two preamp outputs.

AGC USING THE ALBO DIODES

The variable impedance action of the RPT-86/87's internal ALBO diodes can be used to create a wide dynamic range AGC loop with the preamplifiers as shown in Figure 9. While the preamp operates at a fixed AC gain, the input signal is variably attenuated by the impedance-divider networks of R_1/Z_{D1} and R_2/Z_{D2}. As the input signal magnitude increases and the preamp's outputs cross the Peak thresholds, ALBO diode impedance decreases providing more signal attenuation prior to the preamplifier input. If input signal magnitude decreases, diode impedance will increase, reducing signal attenuation. The result is a constant preamp input level creating a constant preamp output amplitude.

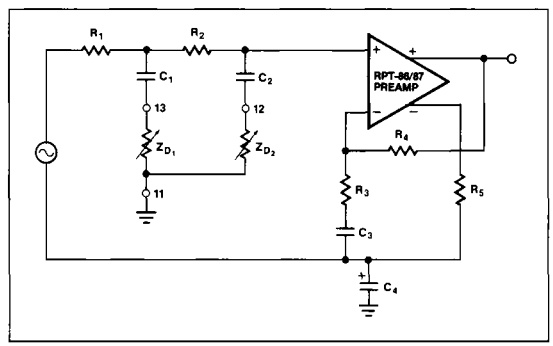


FIGURE 9: *By attenuating the input signal through impedance dividers, the ALBO network simulates the attenuation and frequency characteristics of maximum line length.*

The DC blocking capacitors C_1 and C_2 are required to remove, from the signal path, the DC bias voltage, 0V to 0.8V, of the ALBO diodes. These capacitors also create a frequency dependency by adding a pole/zero pair in the attenuation characteristics of each ALBO diode stage. Figure 10 illustrates the gain vs. frequency response of the first ALBO stage assuming that $R_1 \ll R_2$ and $Z_{D1} \ll R_1$. As Z_{D1} changes depending on input signal amplitude, ω_Z also changes. At $Z_{D1}=R_D MAX$, $\omega_Z = \omega_P$, and the stage gain equals unity with flat frequency response. At $Z_{D1} = R_D MIN$, there is maximum separation between ω_Z and ω_P and a maximum attenuation equal to approximately Z_{D1}/R_1. Combining the effects of two ALBO stages allows the programming of two variable-duration poles and a gain ranging from unity to $(Z_{D1}Z_{D2})/(R_1R_2)$.

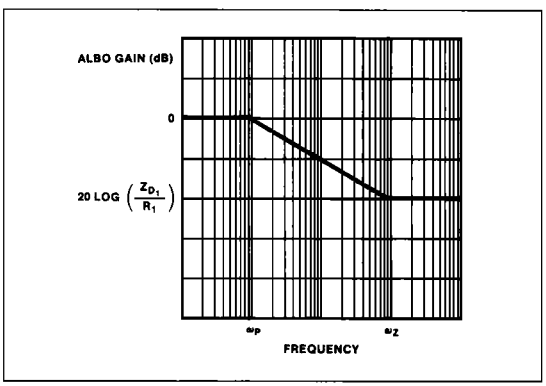


FIGURE 10: *The ALBO impedance creates frequency dependent attenuation.*

DESIGNING THE LC TANK OSCILLATOR

The oscillator on board the RPT-86/87 is based on a pulsed LC resonant tank and produces a continuous "square-wave" clock output even in the absence of an incoming data signal. Connected as shown in Figure 11, the oscillator input, Pin 14, oscillates sinusoidally about the 4V oscillator bias, Pin 15. The nominal oscillation frequency, f_o, is given by the formula:

Equation 3: $$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$

which takes into account the effect of the damping resistor, R. The damping resistor is used to reduce the Q of the LC tank where:

Equation 4: $$Q = R\sqrt{\frac{C}{L}}$$

As the Q of the tank is reduced, the oscillation frequency becomes more easily pulled away from f_o by the synchronizing pulses of the Clock threshold comparators. A low Q is desirable for the repeater's

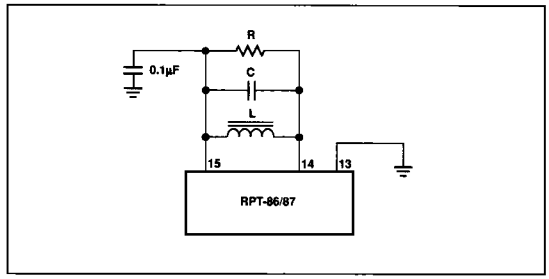


FIGURE 11: *A simple LRC resonant tank oscillator is used by the RPT-86/87 to recover the encoded clock from an incoming data signal.*

oscillator because often the incoming data bit stream is timed at a clock rate slightly different from f_o. The bit stream may also contain timing jitter where each data bit or packet of bits arrives with a slightly different clock timing. To ensure that no data bits are missed under these conditions, the RPT-86/87's oscillator must be flexible enough to track the clock frequency carried within the incoming bit stream.

The damping resistor also determines the amplitude of the LC tank's oscillation. Assuming R is the only dissipative element in the tank, its value can be calculated as a function of the peak-to-peak oscillation amplitude on Pin 14:

Equation 5: $$R = \frac{\pi V_{p\text{-}p}}{4(30\mu A)}$$

where 30µA equals the oscillator bias current, I_{OSC}. To avoid driving the tank oscillation onto the oscillator clamping diode contained within the RPT-86/87, V_{p-p} should be set less than $1.2V_{p-p}$. Letting R = 24kΩ sets an optimum oscillation level of $1V_{p-p}$ for the RPT-86/87.

The values for L and C can be calculated by choosing the desired Q and f_o and then substituting Equation 4 into Equation 3. The generalized formulas for L and C become:

Equation 6: $$C = \frac{\sqrt{4Q^2 - 1}}{4\pi f_o R}$$

Equation 7: $$L = \frac{CR^2}{Q^2}$$

Note that to maintain a sustained oscillation during the absence of an incoming data bit stream, the Q of the LC tank must be greater than 1.

When an incoming data bit stream is of sufficient amplitude to cross the Clock Detector's thresholds, a pulse of current is injected into the tank to synchronize the oscillator frequency to that of the incoming encoded clock. When synchronization is achieved, the various voltage and current waveforms are aligned as shown in Figure 12.

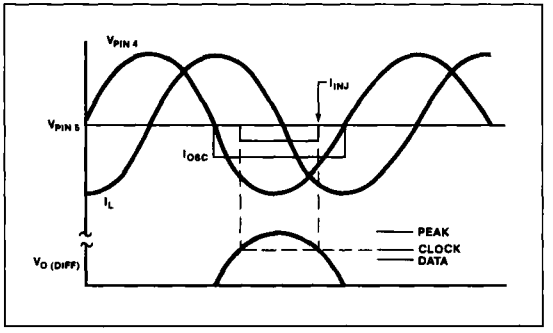


FIGURE 12: *The LC tank is synchronized to the incoming data when the clock detector injection current, I_{INJ}, is entered inside the oscillator's bias current pulse.*

TYPICAL APPLICATIONS

The circuit shown in Figure 13 is a typical T1, 1.544Mbit/s repeater system. The repeater is placed in series with a #22AWG unshielded, twisted-pair transmission line at distances of up to every 9,000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T_1 and output transformer T_2, and is converted to a 5.6V supply voltage that powers the RPT-86/87 by the Zener diodes Z_D. The incoming signal is coupled into the input network by the transformer T_1. One end of T_1's secondary winding is held at AC ground by capacitors C_9 and C_{10}; and the other end is terminated by the line-matching resistor R_1. The line-matching resistor is followed by a line equalization network, which includes the preamplifier feedback circuit and ALBO diodes. This network is designed to compensate for the losses and distortion of the #22AWG twisted-

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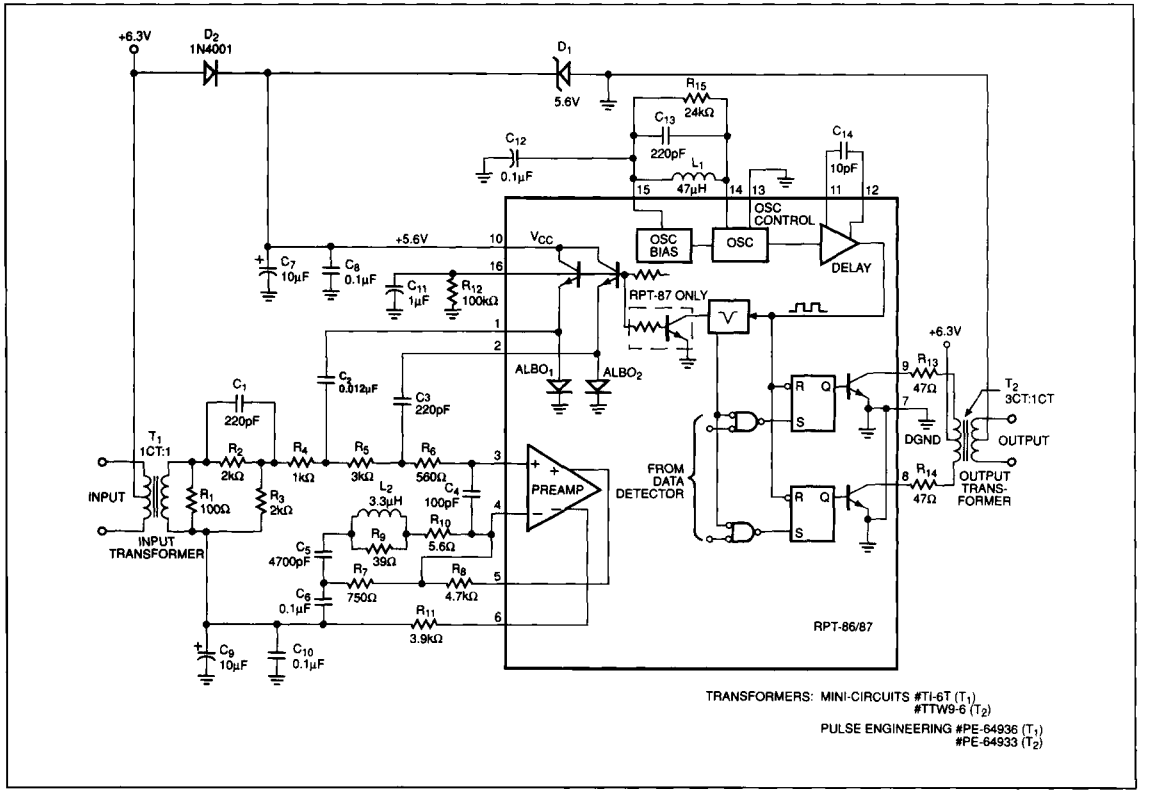

FIGURE 13: *A complete 1.544Mbit/s T1 Repeater Design. For additional details, see application note AN-140. (Note: for 2.048 Mbit/s E1 application, this same circuit works well to –44dB. The only changes necessary are R_1 = 120Ω, C_{13} = 150pF, and L_1 = 39µH. See application note AN-118).*

pair wire transmission line whose characteristics of loss vs. frequency vs. length are shown in Figure 14. The goal of the repeater's equalization network is to allow the recovery of the 1.544 Mbit/s T1 format data with an input level that varies from 0dB ($6V_{p-p}$) to –36dB ($95mV_{p-p}$) measured at a frequency 1/2 the data rate, or 772kHz. As evidenced in Figure 14, at 0 feet of transmission line, the receiver's incoming signal has 0dB attenuation with no frequency distortion. By 3000 feet, the signal amplitude reduces to –12dB level and falling at –6dB/octave, single-pole roll-off, between 770kHz and 1.544MHz. At 6000 feet of transmission line, the signal falls to –26dB with –12dB/octave, double-pole frequency roll-off.

Data rate and transmission line characteristics play an important role in determining the maximum line length from which the RPT-86/87 can recover data. From figure 14 it can be seen that #22AWG twisted-pair wire exhibits much less loss and frequency distortion at lower frequencies. Thus, the RPT-86/87 can recover data from much longer transmission lines if a lower data rate is used. Similarly, using a transmission line with less loss and frequency distortion will allow the RPT-86/87 to recover higher speed data over longer line lengths.

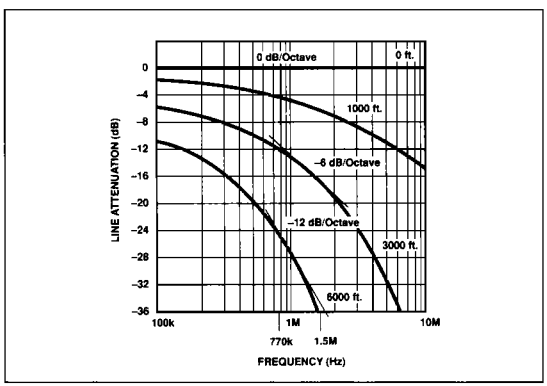

FIGURE 14: *Both line attenuation and frequency distortion become worse as line length increases.*

In the repeater's equalization network, R_2, R_3 and C_1 form one zero while the preamp feedback, R_7, R_8, R_9, R_{10}, C_5, C_6, and L_2 create a second zero in addition to signal gain. At long transmission line length, this provides a double-zero rise plus gain to equalize the lines double-pole roll-off and attenuation. At short line length, the two ALBO diodes will be driven ON by the increased input signal amplitude and will create two poles in the equalization network as well as attenuation. At 0 feet, the two ALBO poles cancel the two network zeros, matching the line's flat frequency response and reducing the overall network gain to –12dB to accommodate the peak threshold comparators. The oscilloscope photos of Figure 15 show: a) both 0dB and –36dB incoming signal levels; and b) the reconstucted data.

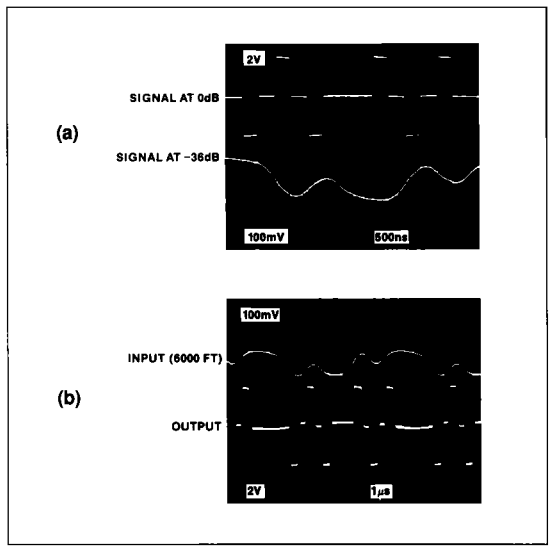

FIGURE 15: *The RPT-86/87 receives the transmitted signal, as shown in (a), ranging in amplitude from 0dB to –36dB. It then recovers and reconstructs the data for retransmission in (b).*

In the repeater application of Figure 13, resistor R_1 terminates the incoming line matching its characteristic impedance. Because the preamplifier is operating at high gain over a wide bandwidth, impedances in the signal path must be kept as low as is practical to minimize their noise contributions. A low impedance at the preamp input also helps reduce the pick-up of stray radiated system noise including noise capacitively coupled from the RPT-86/87's own digital outputs.