

**General Description**

- Trench Power AlphaMOS-II technology
- Low $R_{DS(ON)}$
- Low C_{iss} and C_{rss}
- High Current Capability
- RoHS and Halogen Free Compliant

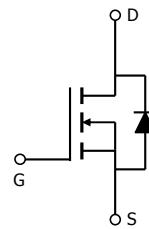
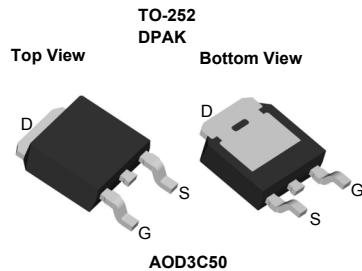
Product Summary

$V_{DS} @ T_{j,max}$	600V
I_{DM}	12A
$R_{DS(ON),max}$	< 1.4Ω
$Q_{g,typ}$	12nC
$E_{oss} @ 400V$	1.5μJ

Applications

- General Lighting for LED and CCFL
- AC/DC Power supplies for Industrial, Consumer, and Telecom

100% UIS Tested
100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD3C50	TO-252	Tape & Reel	2500

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	3*	A
$T_C=100^\circ C$		3	
Pulsed Drain Current ^C	I_{DM}	12	
Avalanche Current ^C $L=1mH$	I_{AR}	3	A
Repetitive avalanche energy ^C	E_{AR}	4.5	mJ
Single pulsed avalanche energy ^H	E_{AS}	152	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Peak diode recovery dv/dt		20	
Power Dissipation ^B	P_D	83	W
$T_C=25^\circ C$		0.7	$W/^\circ C$
Derate above $25^\circ C$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	°C

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	45	55	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	-	0.5	°C/W
Maximum Junction-to-Case ^{D,F}	$R_{\theta JC}$	1.2	1.5	°C/W

* I_D limited by Rated I_D

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$	500			V
		$I_D=250\mu\text{A}, V_{GS}=0\text{V}, T_J=150^\circ\text{C}$		600		
$\text{BV}_{\text{DSS}}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$		0.4		$\text{V}/^\circ\text{C}$
		$V_{DS}=500\text{V}, V_{GS}=0\text{V}$			1	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=400\text{V}, T_J=125^\circ\text{C}$			10	μA
		$V_{DS}=500\text{V}, V_{GS}=0\text{V}$				
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=5\text{V}, I_D=250\mu\text{A}$	3	4.1	5	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=2.2\text{A}$		1.1	1.4	Ω
g_{FS}	Forward Transconductance	$V_{DS}=40\text{V}, I_D=1.5\text{A}$		2.5		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.78	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
I_{SM}	Maximum Body-Diode Pulsed Current ^C				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=100\text{V}, f=1\text{MHz}$		662		pF
C_{oss}	Output Capacitance			26		pF
$C_{\text{o(er)}}$	Effective output capacitance, energy related ^I	$V_{GS}=0\text{V}, V_{DS}=0 \text{ to } 400\text{V}, f=1\text{MHz}$		19		pF
$C_{\text{o(tr)}}$	Effective output capacitance, time related ^J			35		pF
C_{rss}	Reverse Transfer Capacitance	$V_{GS}=0\text{V}, V_{DS}=100\text{V}, f=1\text{MHz}$		9.7		pF
R_g	Gate resistance	$f=1\text{MHz}$		3		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=400\text{V}, I_D=3\text{A}$		12	25	nC
Q_{gs}	Gate Source Charge			3.4		nC
Q_{gd}	Gate Drain Charge			4.4		nC
$t_{\text{D(on)}}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=250\text{V}, I_D=3\text{A}, R_G=25\Omega$		21		ns
t_r	Turn-On Rise Time			28		ns
$t_{\text{D(off)}}$	Turn-Off Delay Time			32		ns
t_f	Turn-Off Fall Time			21		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3\text{A}, dI/dt=100\text{A}/\mu\text{s}, V_{DS}=100\text{V}$		260		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=3\text{A}, dI/dt=100\text{A}/\mu\text{s}, V_{DS}=100\text{V}$		2.3		μC

- A. The value of R_{qJA} is measured with the device in a still air environment with $T_A=25^\circ\text{C}$.
- B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$ in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.
- D. The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$.
- G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.
- H. L=60mH, $I_{AS}=2.25\text{A}$, $V_{DD}=150\text{V}$, $R_G=10\Omega$, Starting $T_J=25^\circ\text{C}$.
- I. $C_{\text{o(er)}}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(\text{BR})\text{DSS}}$.
- J. $C_{\text{o(tr)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(\text{BR})\text{DSS}}$.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

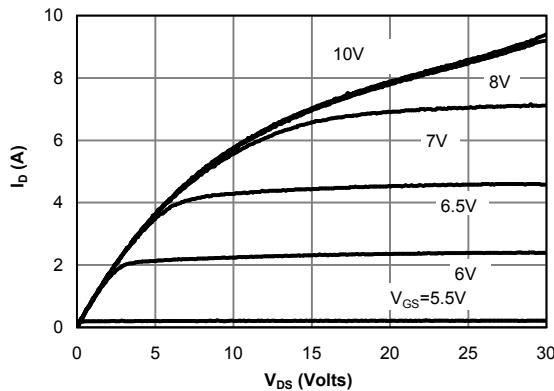


Figure 1: On-Region Characteristics

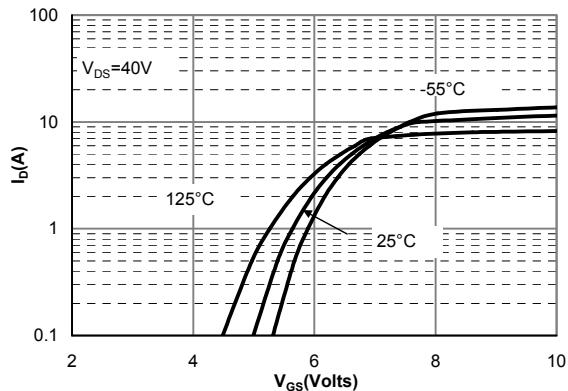


Figure 2: Transfer Characteristics

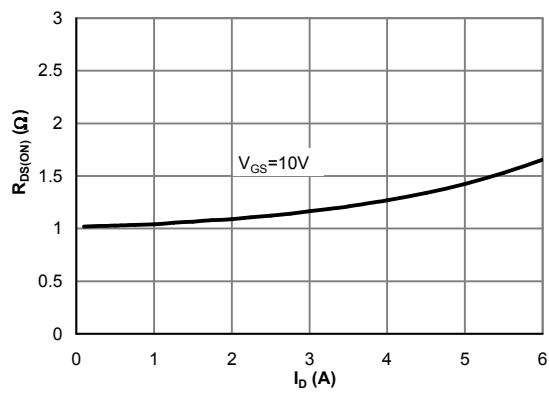


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

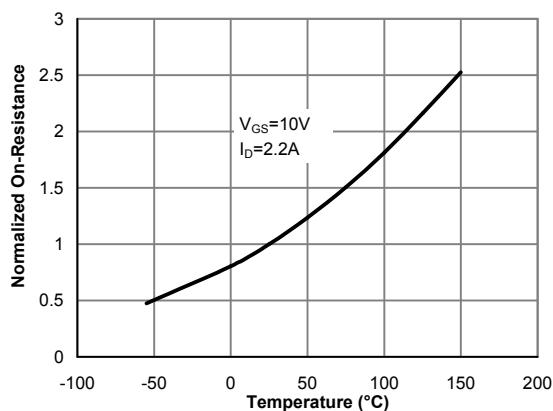


Figure 4: On-Resistance vs. Junction Temperature

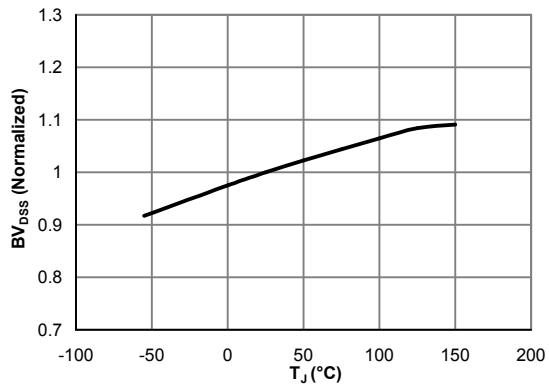


Figure 5: Break Down vs. Junction Temperature

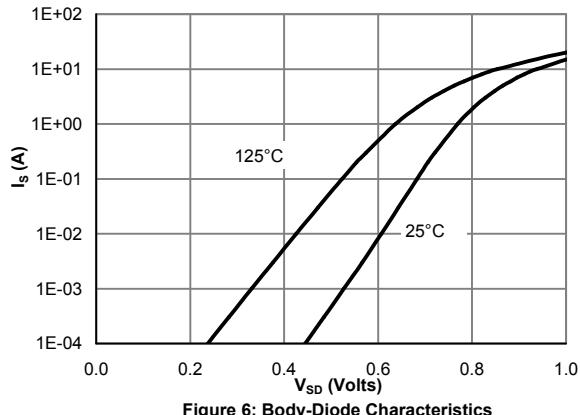
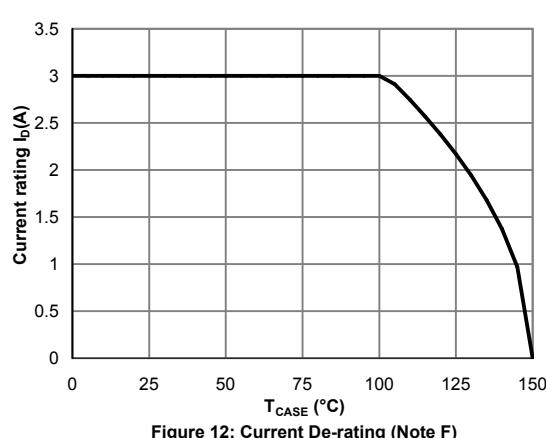
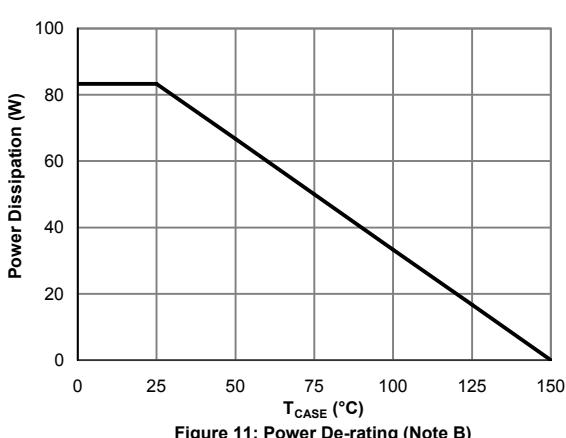
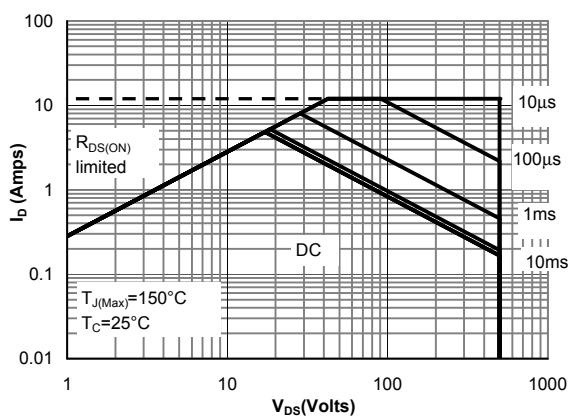
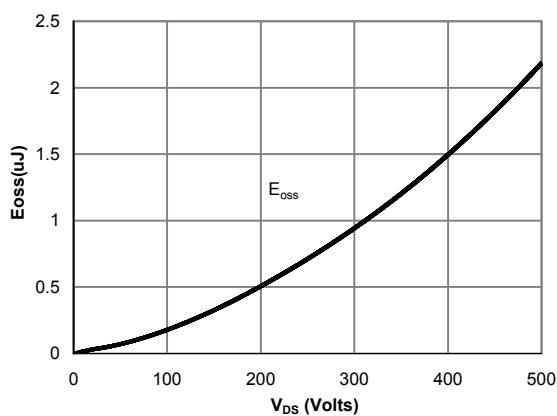
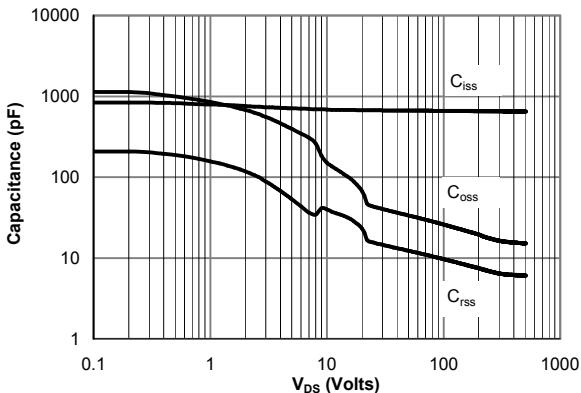
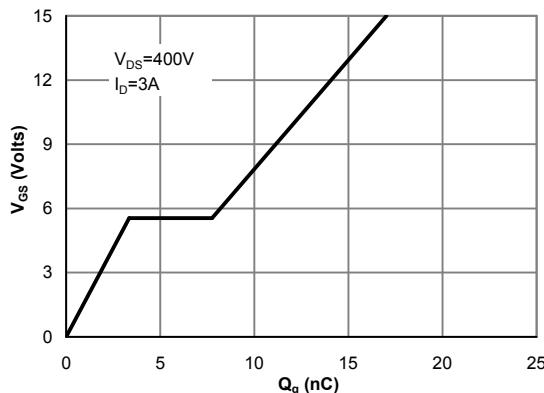


Figure 6: Body-Diode Characteristics

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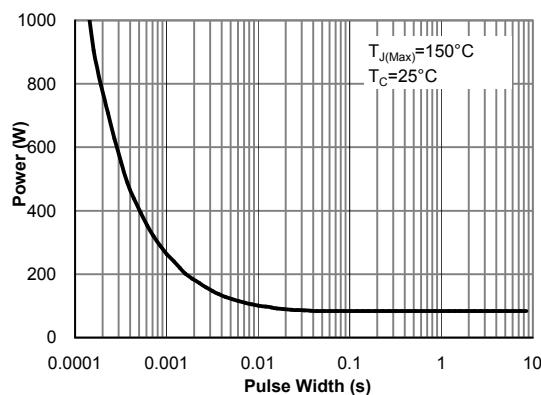


Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)

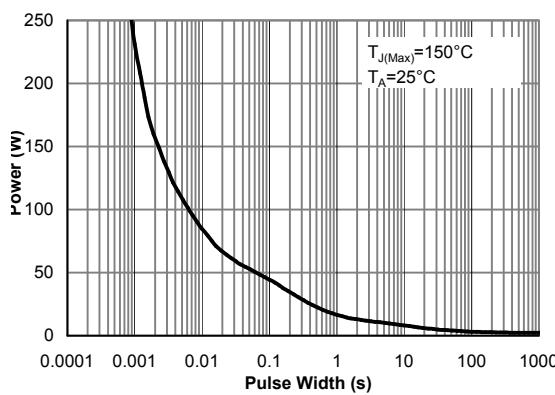


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

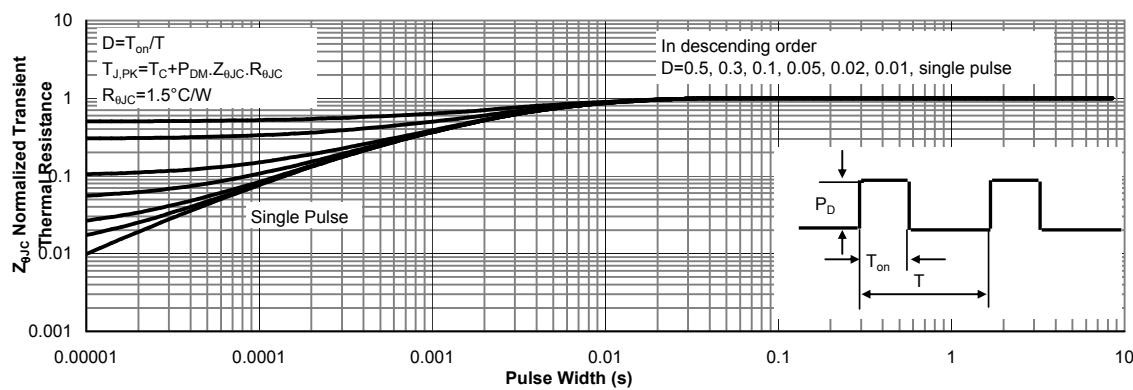


Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

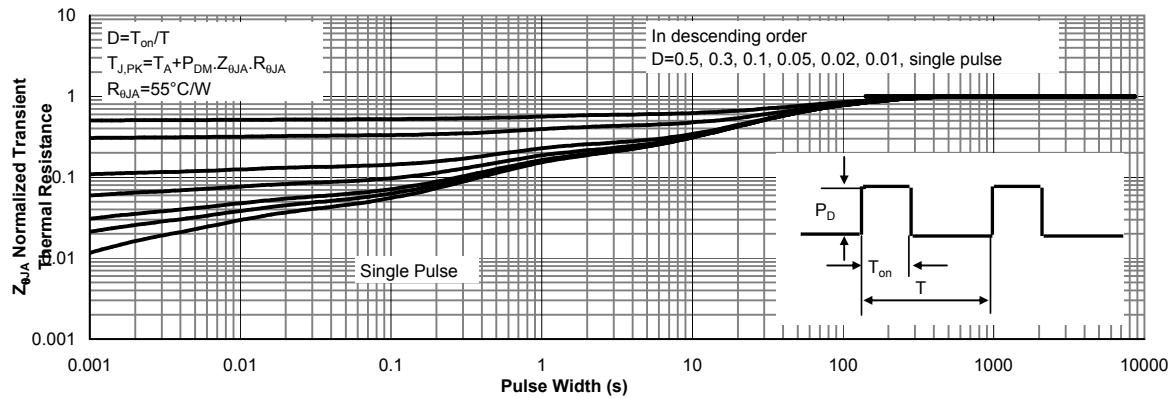
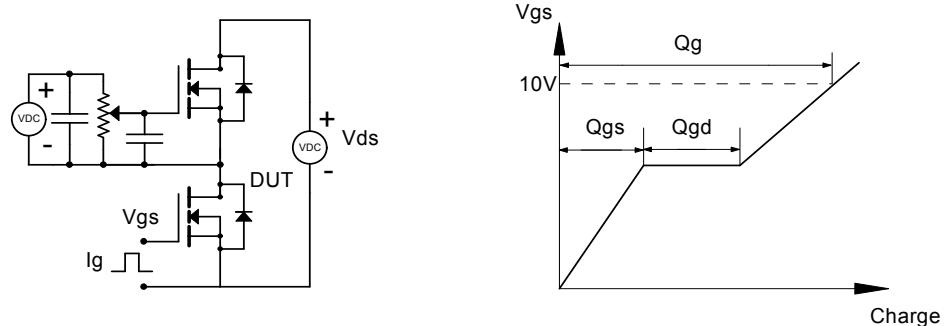
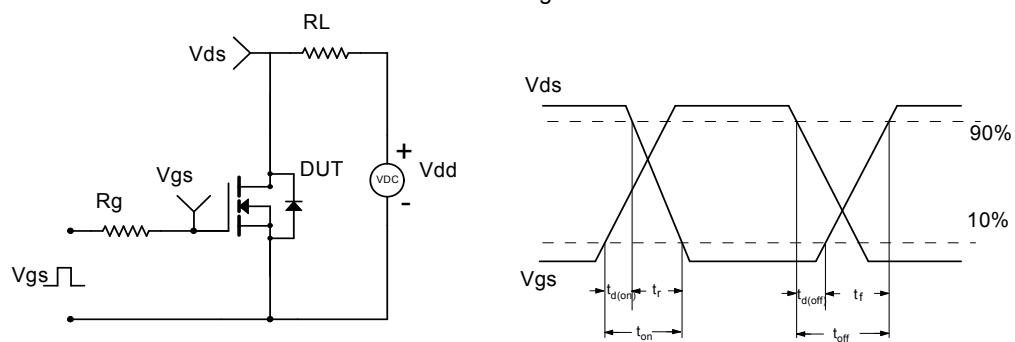


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

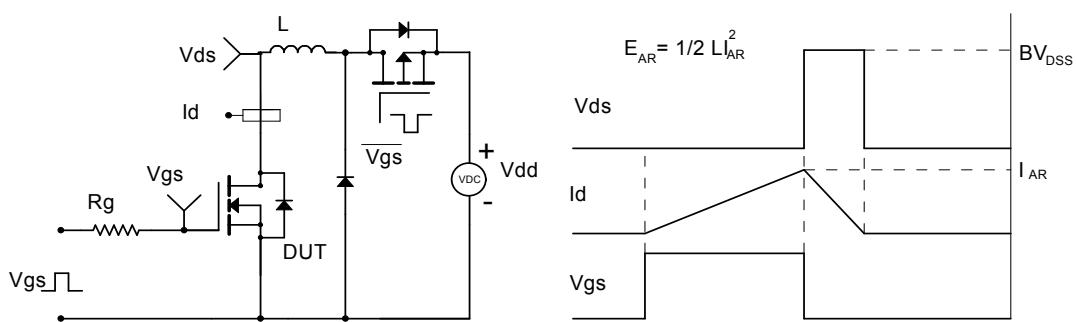
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

