ML2612 FAMILY DATASHEET

(DIGEST)
Version 3
Revised on 31-Oct-07

Contents

General Description

The ML2612 family is a low power small size monaural CODEC with in-built speaker amplifier, ideally suited for portable playback and recording applications. The microphone interface (1bit digital) supports MEMS (silicon) digital microphones for low noise recording systems. For digital signal processing, the ML2612 uses high-pass filters and a 5-band programmable equalizer including 5 channel notch filter to enable flexible sound processing.

Features

1) CPU Interface
   2 modes support
   1-1) 2 wire serial interface
   1-2) 3 wire serial interface

2) Serial Audio Interface (SAI)
   - Sampling frequency: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k Hz
   -Master/Slave selectable
   - SAI_LRCLK transfer mode/Frame sync. Transfer mode selectable
   - Channel data length: 16bit
   - SAI_LRCLK positive/negative selectable
   - 1bit delay/Left Justified selectable
   - MSB first/LSB first selectable
   - SAI_BCLK frequency
     Master mode: 32fs/64fs selectable
     Slave mode : ～128fs

3) Digital Signal Processing
   - High pass filter for wind noise reduction
   - 5 band programmable equalizer(5 channel programmable notch filter)

4) Microphone input
   - Programmable gain amplifier: -12～+35.25dB(0.75dB/step)
   - Gain boost amplifier: 0dB、+9.75dB、+19.5dB、+29.25dB
   - ALC Function
   - MEMS (silicon) microphone digital interface

5) ADC、DAC
   - 16bit Compact ADC、DAC

6) Speaker amplifier
   - BTL Speaker amplifier
   - Can be use as line output- Lin input 1 channel mixing capability
   - Pop noise reduction function

7) Clock
   - 11.2896～54MHz
   - 256fs / 512fs / 1024fs

8) Power supply voltage
   - LVDD : 1.65～2.75V
   - HVDD: 2.7～3.6V

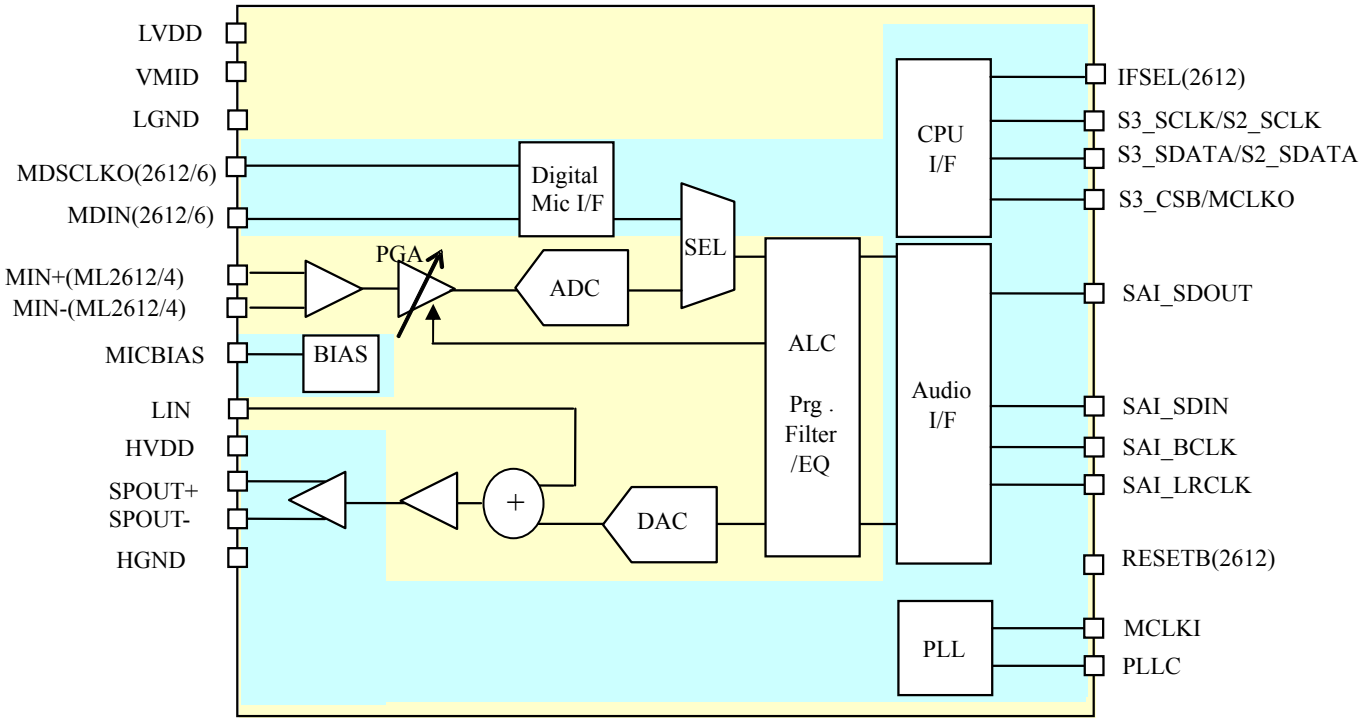
9) Package

Size:	4.0mm×4.0mm	0.5mm pitch 24pin QFN
	2.0mm×2.5mm	0.5mm pitch 20pin WCSP

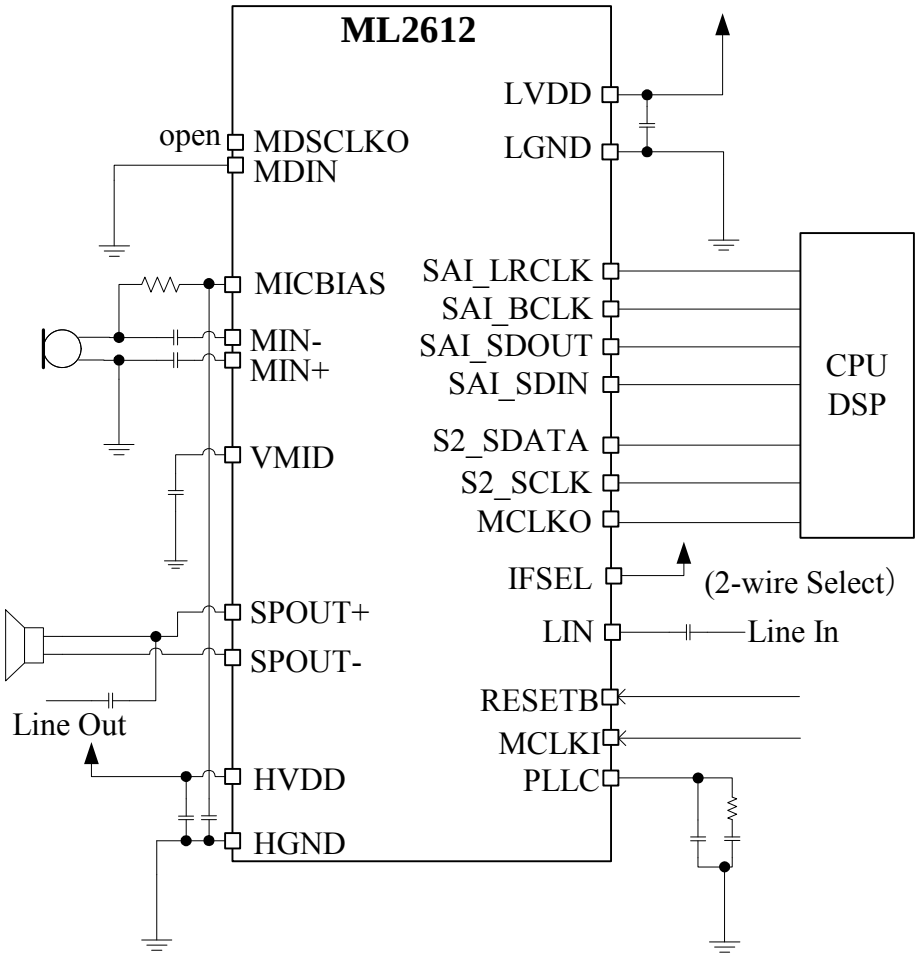
10) Product Line up

Part #	Package	CPU I/F	MIC I/F
ML2612GD	QFN	2 / 3-wire selectable	Analog/Digital selectable
ML2614HB	WCSP	3-wire	Analog MIC I/F
ML2616HB	WCSP	3-wire	Digital MIC I/F

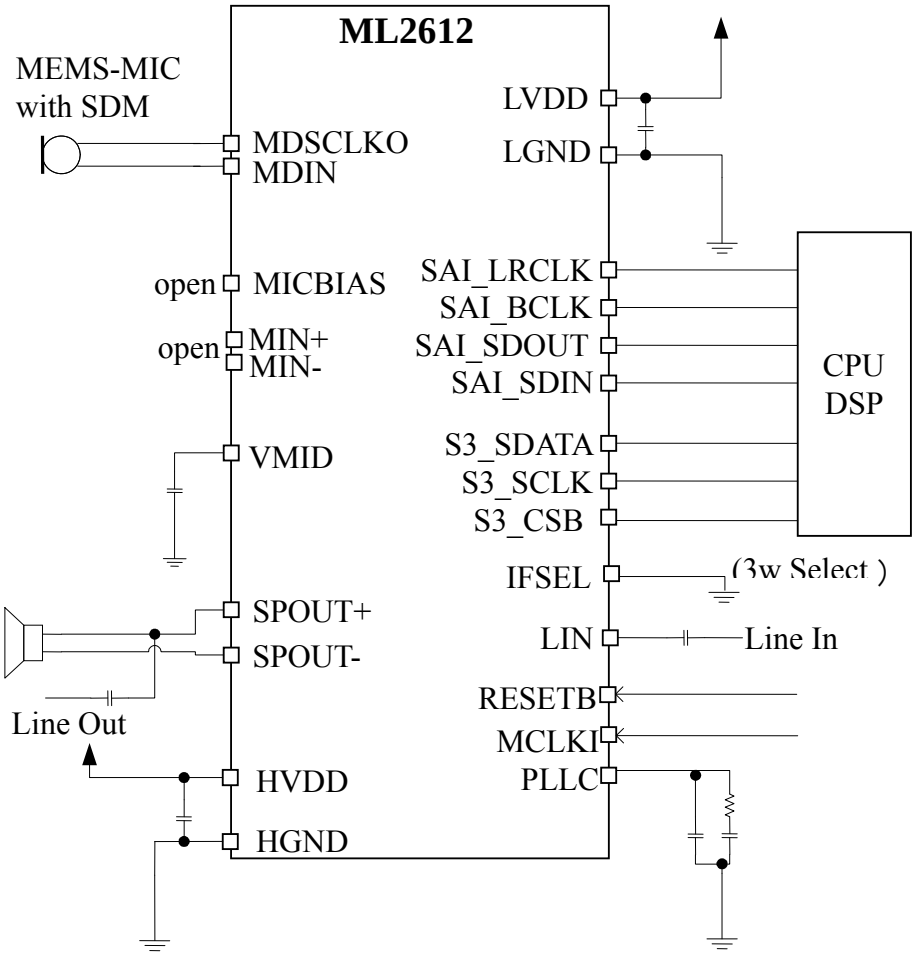
Block Diagram



Application Example



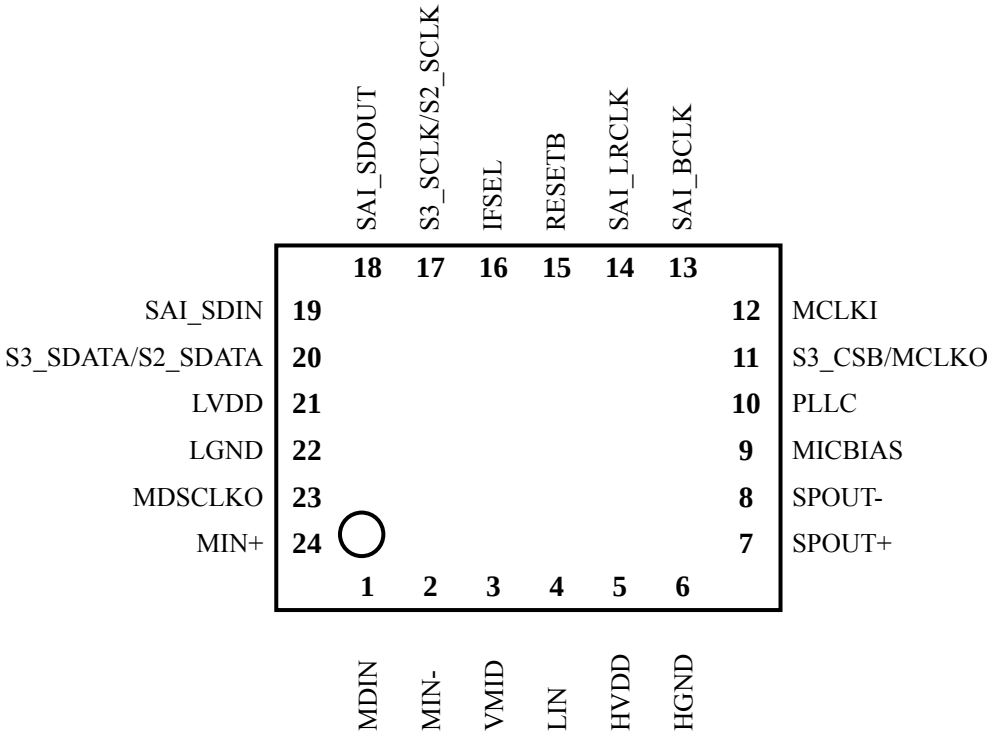
●Application example for MEMS microphone with SDM



Pin Layout

ML2612GD (24Pin QFN)

Top View



ML2614HB (20Pin WCSP)

Bottom View

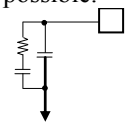
SAI_SDIN	S3_SCLK	SAI_LRCLK	MCLKI	**5**
S3_SDATA	SAI_SDOUT	SAI_BCLK	PLLC	**4**
LVDD	LIN	S3_CSB	MICBIAS	**3**
LGND	MIN-	HGND	SPOUT-	**2**
MIN+	VMID	HVDD	SPOUT+	**1**
D	**C**	**B**	**A**	

ML2616HB (20Pin WCSP)

Bottom View

SAI_SDIN	S3_SCLK	SAI_LRCLK	MCLKI	**5**
S3_SDATA	SAI_SDOUT	SAI_BCLK	PLLC	**4**
LVDD	LIN	S3_CSB	MICBIAS	**3**
LGND	MDIN	HGND	SPOUT-	**2**
MDSCLKO	VMID	HVDD	SPOUT+	**1**
D	**C**	**B**	**A**	

Pin Description

Pin No.		Pin Name	IO	Power	Description	Reset state	Unused pin
QFN	WCSP						
Common terminals for all family products							
8	A2	SPOUT-	O	HVDD	Speaker – output	Hi-Z	Open
7	A1	SPOUT+	O	HVDD	Speaker + output	Hi-Z	Open
12	A5	MCLKI	I	HVDD	Master clock input	(input)	-
10	A4	PLLC	O	HVDD	Capacitor and resistor connect pin for PLL stable operation. Please set following circuit near by pins as possible.  PLLC pin	HGND	Open
3	C1	VMID	O	LVDD	Capacitor connect pin for Analog reference voltage. Please connect 1.0µF capacitor between this pin and LGND.	LGND	-
9	A3	MICBIAS	O	HVDD	Microphone bias voltage output. Please connect 2.2µF capacitor between this pin and HGND.	HGND	Open
14	B5	SAI_LRCLK	IO	HVDD	SAI LR clock input	(input)	-
13	B4	SAI_BCLK	IO	HVDD	SAI bit clock input/output	(input)	-
19	D5	SAI_SDIN	I	HVDD	SAI serial data input	(input)	-
18	C4	SAI_SDOUT	O	HVDD	SAI serial data output	L	-
21	D3	LVDD	P	-	Low voltage power supply. Please connect bypass capacitor between this pin and LGND.	-	-
22	D2	LGND	P	-	Low voltage ground	-	-
5	B1	HVDD	P	-	High voltage power supply. Please connect bypass capacitor between this pin and HGND.	-	-
6	B2	HGND	P	-	High voltage ground	-	-
4	C3	LIN	I	LVDD	Lin input	Hi-Z	Open
Terminals depends on product ML2612GD has all terminals. Some pins are limited according with WCSP products.							
2	C2	MIN-	I	LVDD	Analog microphone - input Apply for ML2612GD and ML2614HB	Hi-Z	Open
24	D1	MIN+	I	LVDD	Analog microphone + input Apply for ML2612GD and ML2614HB	Hi-Z	Open
1	C2	MDIN	I	HVDD	Digital microphone input Apply for ML2612GD and ML2616HB	(input)	Open
23	D1	MDSCLKO	O	HVDD	Digital microphone data synchronous clock output Apply for ML2612GD, and ML2616HB	L	Open
16	N/A	IFSEL	I	HVDD	Control interface mode select L: 3 wire serial interface H: 2 wire serial interface Apply for ML2612GD	(input)	-
20	D4	S3_SDATA /S2_SDATA	IO	HVDD	3 or 2 wire serial interface data IO. When 3 wire serial is selected, output interface becomes CMOS type. When 2 wire serial is selected, output interface becomes open drain type. Please use this pin with external pull-up resister when 2 wire serial is selected. If this pin is used with external pull-up resistor, it possibly gets noise from power. Therefore tamper noise design is required in the noisy environment.	(input)	-

17	C5	S3_SCLK /S2_SCLK	I	HVDD	3 or 2 wire serial interface clock IO. If this pin is used with external pull-up resistor, it possibly gets noise from power. Therefore tamper noise design is required in the noisy environment.	(input)	-
11	B3	S3_CSB /MCLKO	IO	HVDD	When IFSEL=L, chip select input for 3 wire serial interface. When IFSEL=H,256fs clock output.	(input)/L	-/ Open
15	N/A	RESETB	I	HVDD	Active-low reset input. Apply for ML2612GD	(input)	-

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
LVDD Supply Voltage	LVDD	—	-0.3~3.5	V
HVDD Supply Voltage	HVDD	—	-0.3~4.5	V
Input Voltage	Vin	—	-0.3～VDD+0.3	V
Storage Temperature	Tstg	—	-55～+125	°C
Power Dissipation*1	Pd	Ta=25°C	500	mW
Output Current1	IOSP	SPOUT+/- pin	-560~+560	mA
Output Current2	IOO	Except SPOUT+/-	-8 ~ +8	mA

Note) Do not short the output pin to another output pin, power supply pin or GND pin.
(Output pin includes an IO pin which is in output mode)*1Please reffer to the.

Recommended Operating Condition

Parameter	Symbol	Condition	Rating	Unit
LVDD Supply Voltage	LVDD	LVDD≦HVDD	1.65~2.75	V
HVDD Supply Voltage	HVDD	LVDD≦HVDD	2.7~3.6	V
Operating Temperature	Top	—	-20~+85	°C

Electrical Characteristics

DC Characteristics

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pin
"H" Input Voltage	VIH	HGND=0V	HVDD×0.8	—	VDD	V	All Digital Input
"L" Input Voltage	VIL	HGND=0V	0	—	HVDD×0.2	V	All Digital Input
"H" Output Voltage	VOH	IOH=-1mA	HVDD×0.85	—	—	V	Except S2_DATA
"L" Output Voltage 1	VOL1	IOL=1mA	—	—	HVDD×0.15	V	Except S2_DATA
"L" Output Voltage2	VOL2	IOL=3mA, HVDD>2V HVDD<2V	—	—	0.4 VDD×0.2	V	S2_DATA
"H" Input leakage current	IIH	VIH=HVDD	—	—	10	µA	All Digital Input
"L" Input leakage current	IIL	VIL=HGND	-10	—	—	µA	All Digital Input
Operating Current1 LVDD	IDDO1L	Playback no Load Sin1kHz-Full Scale output	—	—	9	mA	
Operating Current1 HVDD	IDDO1H		—	—	9	mA	
Operating Current2 LVDD	IDDO2L	Record Sin1kHz-Full Scale input	—	—	13	mA	
Operating Current2 HVDD	IDDO2H		—	—	6	mA	
Standby Current1	IDDS1	-20~25°C	—	—	5	µA	
Standby Current2	IDDS2	-20~50°C	—	—	15	µA	
Standby Current3	IDDS3	-20~85°C	—	—	75	µA	

Note) Please reffer to the followingpage describing tpical current value.
Note) Standby current is total value for all power supply currents.

Power Consumption

The following table shows typical operating current under the following conditions

(LVDD=1.8V, HVDD=3.0V, Ta=25°C, no-load, no-signal, PLL off)

Operating Condition	Symbol	LVDD(mA)	HVDD(mA)	TOTAL(mW)
8Ω BTL Speaker playback (48kHz-Sampling)	IDDO1	2.4	2.1	10.62
Line output playback (48kHz-Sampling)	IDDO2	2.1	1.4	7.98
Line input8Ω BTL speaker output(Clock stopped)	IDDO3	0.7	1.7	6.36
Line input Line output(Clock stopped)	IDDO4	0.5	0.5	2.40
Analog Mic I/F recording (48kHz-Sampling)	IDDO5	5.2	0.7	11.46
Digital Mic I/F recording(48kHz-Sampling)	IDDO6	1.7	0.4	4.26

Note) MCLKI=12.288MHz(256fs), SAI – Master, 3wire Serial IF
Recording condition: ALC and HPF1 are enabled. HPF2 and 5band-Programmable Equalizer are disabled.
Playback condition: Playback Limiter and 5band-Programmable Equalizer are disabled.

(LVDD=2.5V, HVDD=3.0V, Ta=25°C, no-load, no-signal, PLL off)

Operating Condition	Symbol	LVDD(mA)	HVDD(mA)	TOTAL(mW)
8Ω BTL Speaker playback (48kHz-Sampling)	IDDO1	3.8	2.1	15.80
Line output playback(48kHz-Sampling)	IDDO2	3.4	0.9	11.20
Line input8Ω BTL speaker output(Clock stopped)	IDDO3	1.2	1.7	8.10
Line input Line output(Clock stopped)	IDDO4	0.8	0.5	3.50
Analog Mic I/F recording (48kHz-Sampling)	IDDO5	7.4	0.7	20.60
Digital Mic I/F recording(48kHz-Sampling)	IDDO6	2.4	0.4	7.20

Note) MCLKI=12.288MHz(256fs), SAI – Master, 3wire Serial IF
Recording condition: ALC and HPF1 are enabled. HPF2 and 5band-Programmable Equalizer are disabled.
Playback condition: Playback Limiter and 5band-Programmable Equalizer are disabled.

(LVDD=1.8V, HVDD=3.0V, Ta=25°C, no-load, no-signal, PLL on)

Operating Condition	Symbol	LVDD(mA)	HVDD(mA)	TOTAL(mW)
8Ω BTL Speaker playback (48kHz-Sampling)	IDDO1	2.9	3.5	15.72
Line output playback (48kHz-Sampling)	IDDO2	2.7	2.4	12.06
Line input8Ω BTL speaker output(Clock stopped)	IDDO3	0.7	1.7	6.36
Line input Line output(Clock stopped)	IDDO4	0.5	0.5	2.40
Analog Mic I/F recording (48kHz-Sampling)	IDDO5	5.9	2.1	16.92
Digital Mic I/F recording(48kHz-Sampling)	IDDO6	2.4	1.9	10.02

Note) MCLKI=27MHz, SAI – Master, 3wire Serial IF
Recording condition: ALC and HPF1 are enabled. HPF2 and 5band-Programmable Equalizer are disabled.
Playback condition: Playback Limiter and 5band-Programmable Equalizer are disabled.

(LVDD=2.5V, HVDD=3.0V, Ta=25°C, no-load, no-signal, PLL on)

Operating Condition	Symbol	LVDD(mA)	HVDD(mA)	TOTAL(mW)
8Ω BTL Speaker playback (48kHz-Sampling)	IDDO1	4.6	3.5	22.00
Line output playback(48kHz-Sampling)	IDDO2	4.2	2.4	17.70
Line input8Ω BTL speaker output(Clock stopped)	IDDO3	1.2	1.7	8.10
Line input Line output(Clock stopped)	IDDO4	0.8	0.5	3.50
Analog Mic I/F recording (48kHz-Sampling)	IDDO5	8.2	2.1	26.80
Digital Mic I/F recording(48kHz-Sampling)	IDDO6	3.2	2.9	13.70

Note) MCLKI=27MHz, SAI – Master, 3wire Serial IF
Recording condition: ALC and HPF1 are enabled. HPF2 and 5band-Programmable Equalizer are disabled.
Playback condition: Playback Limiter and 5band-Programmable Equalizer are disabled.

Standby Current typical value is follows

(LVDD=2.75V, HVDD=3.6V)

Parameter	Symbol	Condition	Current value	Unit
Standby Current1	IDDST1	25°C	1	µA
Standby Current2	IDDST2	50°C	3	µA
Standby Current3	IDDST3	85°C	15	µA

Note) Pop noise reduction bias resistor of SPOUT+ is off state

AC Characteristics

Clock

PLL not used

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C)

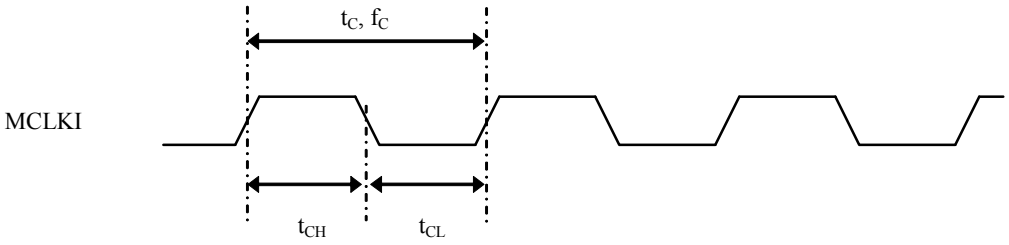
Parameter	Symbol	Min	Max.	Unit
MCLKI Frequency	f_C	2.048	49.152	MHz
MCLKI Period	t_C	$1/f_C$	$1/f_C$	ns
MCLKI "H" Length	t_{CH}	tC*0.4	—	ns
MCLKI "L" Length	t_{CL}	tC*0.4	—	ns

PLL used (SAI Master)

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C)

Parameter	Symbol	Min	Max.	Unit
MCLKI Frequency	f_C	11.2896	54	MHz
MCLKI Period	t_C	$1/f_C$	$1/f_C$	ns
MCLKI "H" Length	t_{CH}	tC*0.4	—	ns
MCLKI "L" Length	t_{CL}	tC*0.4	—	ns

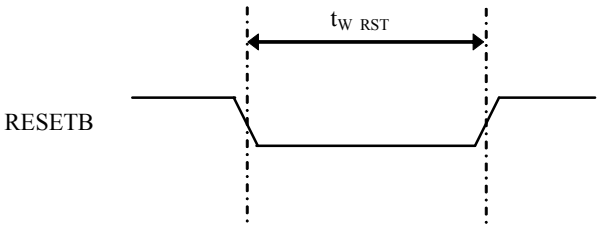
Note) SAI Slave can be operated without MCLKI input because internal clock is generated from SAI_LRCLK



Reset

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C)

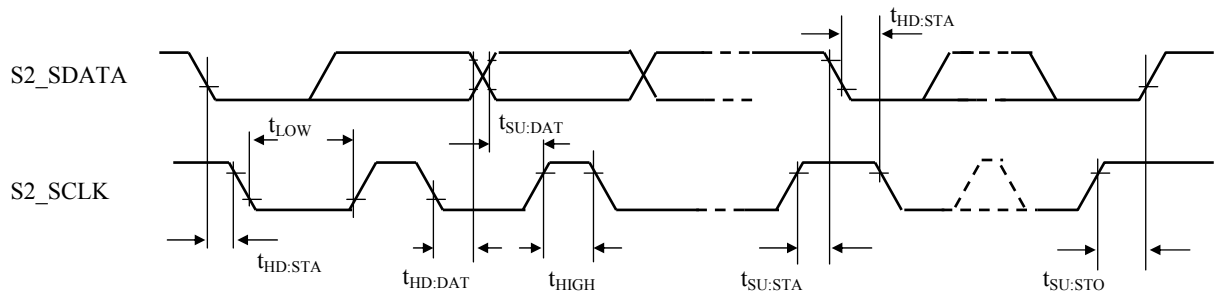
Parameter	Symbol	Min	Max.	Unit
RESETB pulse width	t_{W_RST}	5	—	µs



2 wire serial interface

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C, CL=30pF)

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max.	Min	Max.	
S2_SCLK Frequency	f_{SCL}	—	100	—	400	kHz
S2_SCLK "L" Length	t_{LOW}	4.7	—	1.3	—	µs
S2_SCLK "H" Length	t_{HIGH}	4.0	—	0.6	—	µs
Hold time under Repeat [Start] Condition	$t_{HD:STA}$	4.0	—	0.6	—	µs
Setup Time under Repeat[Start] Condition	$t_{SU:STA}$	4.0	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU:DAT}$	250	—	100	—	ns
Setup Time under [Stop] Condition	$t_{SU:STO}$	4.0	—	0.6	—	µs

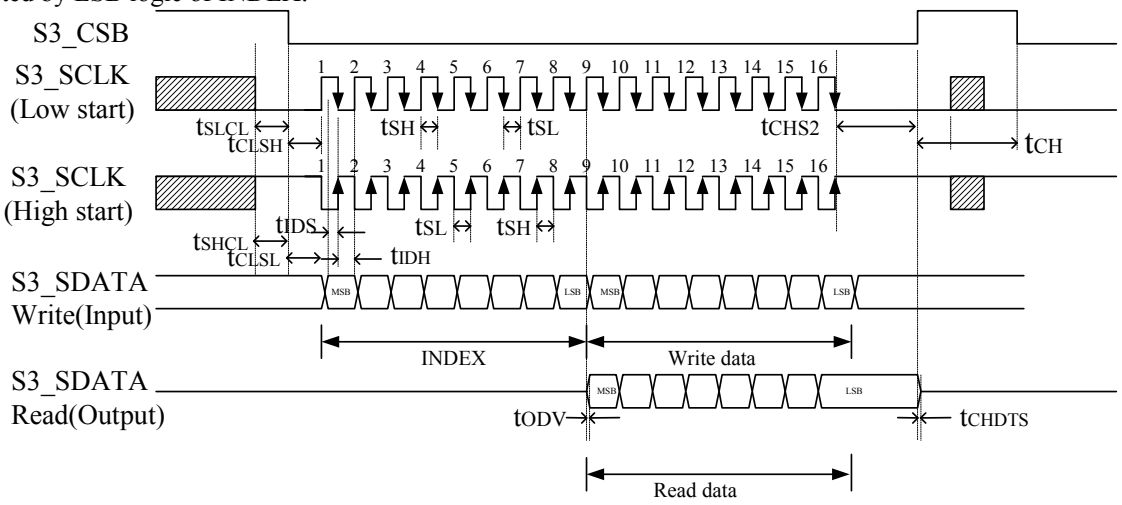


3 wire serial interface

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C, CL=30pF)

Parameter	Symbol	Min	Max.	Unit
SCLK Low to Chip Select enable	t_{SLCL}	100	—	ns
Chip Select enable to SCLK Low	t_{CLSL}	100	—	ns
Chip Select enable to SCLK High	t_{CLSH}	100	—	ns
SCLK High to Chip Select enable	t_{SHCL}	100	—	ns
SCLK High Pulse Width	t_{SH}	50	—	ns
SCLK Low Pulse Width	t_{SL}	50	—	ns
Input Data Hold time	t_{IDH}	30	—	ns
Input Data Setup time	t_{IDS}	30	—	ns
SCLK last edge to Chip Select disable	t_{CHS2}	100	—	ns
Chip Select High Pulse Width	t_{CH}	100	—	ns
Output Data Valid	t_{ODV}	—	40	ns
Chip Select High to Data Transition	t_{CHDTS}	—	40	ns

Two kinds of timing is supported depends on the S3_SCLK pin level at data transfer start.Read or Write is selected by LSB logic of INDEX.

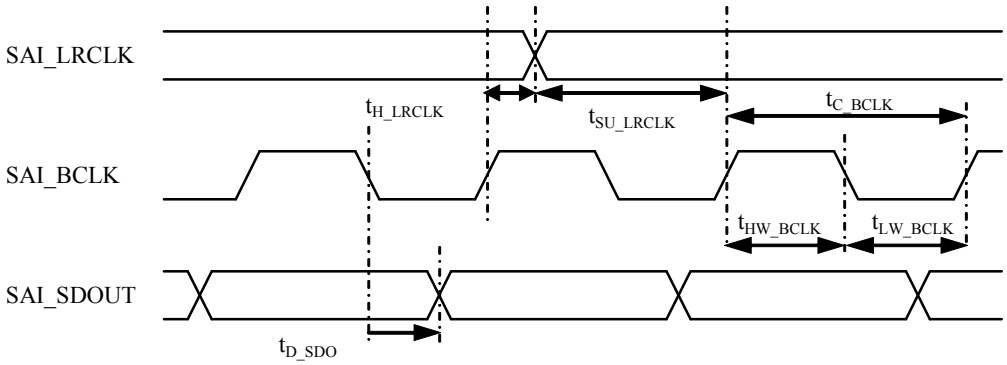


SAI (Slave)

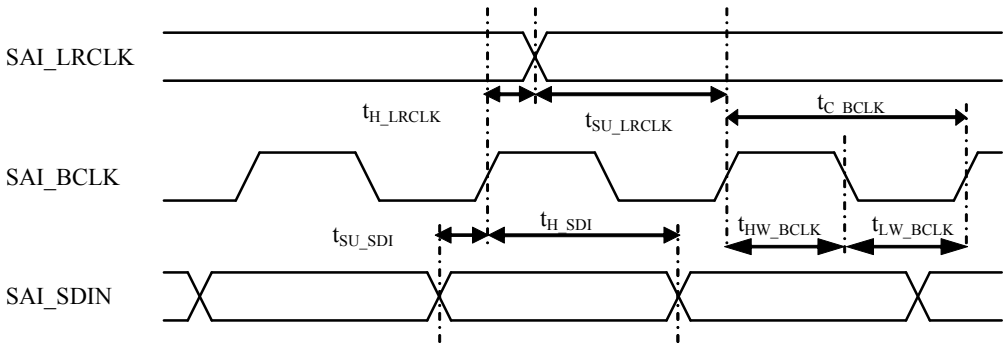
(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C, CL=30pF)

Parameter	Symbol	Min	Max.	Unit
SAI_BCLK Period	t_{C_BCLK}	—	128fs	Hz
SAI_BCLK "H" Length	t_{HW_BCLK}	73	—	ns
SAI_BCLK "L" Length	t_{LW_BCLK}	73	—	ns
SAI_LRCLK Hold Time	t_{H_LRCLK}	20	—	ns
SAI_LRCLK Setup Time	t_{SU_LRCLK}	20	—	ns
SAI_SDOUT Delay Time	t_{D_SDO} *1	—	50	ns
SAI_SDIN Setup Time	t_{SU_SDI}	20	—	ns
SAI_SDIN Hold Time	t_{H_SDI}	20	—	ns

*1t_{D_SDO} is the delay time from later one of SAI_BCLK transition and SAI_LRCLK transition.



SAI Transmit

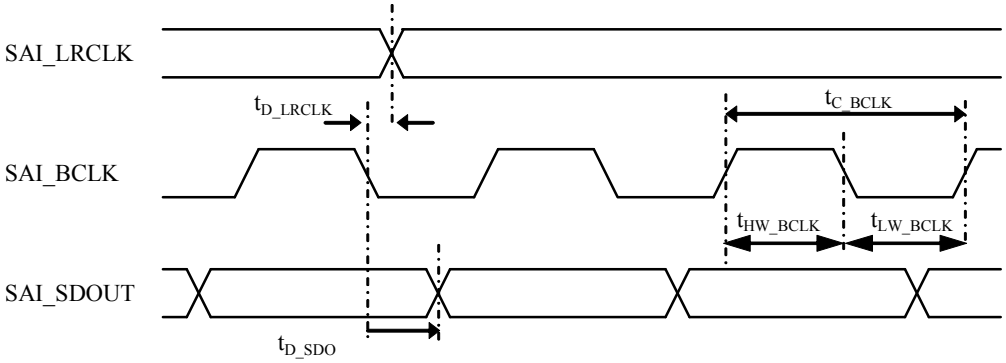


SAI Receive

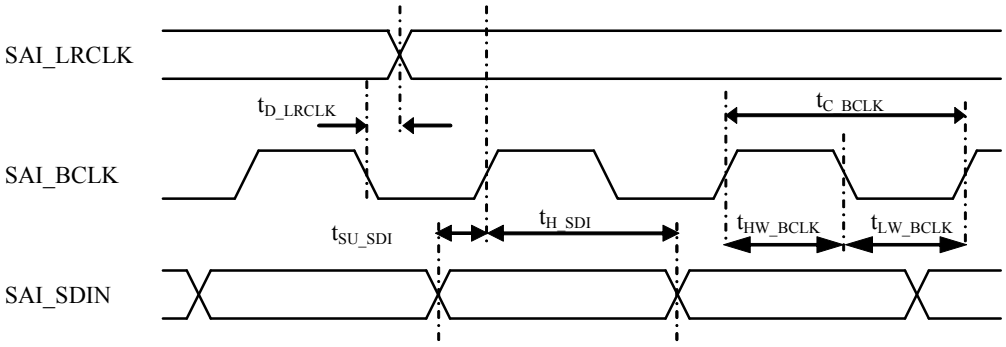
SAI (Master)

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C, CL=30pF)

Parameter	Symbol	Min	Max.	Unit
SAI_BCLK Period	t_{C_BCLK}	—	64fs	Hz
SAI_BCLK "H" Length	t_{HW_BCLK}	146	—	ns
SAI_BCLK "L" Length	t_{LW_BCLK}	146	—	ns
SAI_LRCLK Delay Time	t_{D_LRCLK}	—	20	ns
SAI_SDOUT Delay Time	t_{D_SDO}	—	20	ns
SAI_SDIN Setup Time	t_{SU_SDI}	50	—	ns
SAI_SDIN Hold Time	t_{H_SDI}	0	—	ns



SAI Transmit



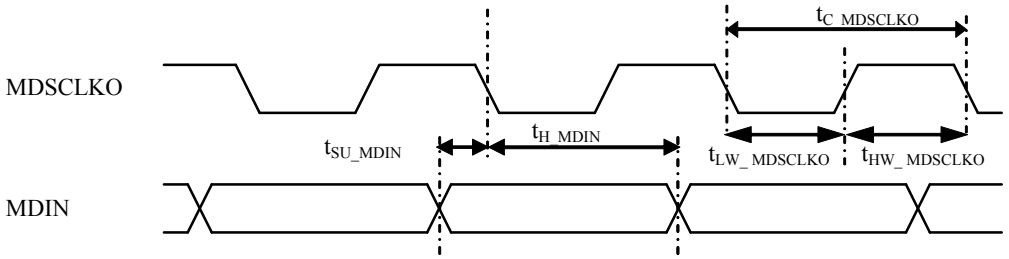
SAI Receive

Digital Microphone Interface

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C)

Parameter	Symbol	Min	Max.	Unit
MDSCLKO Period	$t_{C\_MDSCLKO}$	—	64fs	Hz
MDSCLKO “H” Length	$t_{HW\_MDSCLKO}$	146	—	ns
MDSCLKO “L” Length	$t_{LW\_MDSCLKO}$	146	—	ns
MDIN Setup Time	t_{SU_MDIN}	50	—	ns
MDIN Hold Time	t_{H_MDIN}	0	—	ns

ML2612GD and ML2616HB support 64fs 1 bit digital audio data transfer. Please input 1 bit digital audio data synchronized with MDCLKO 64fs into MDIN.

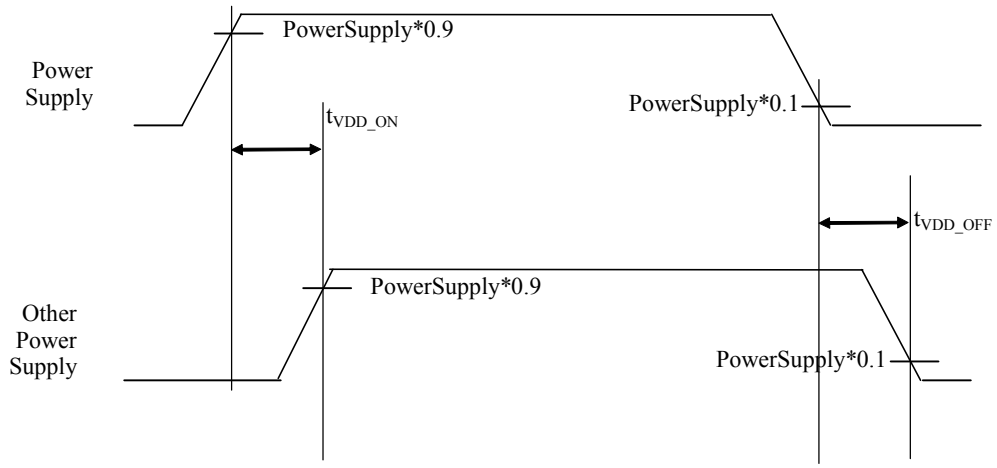


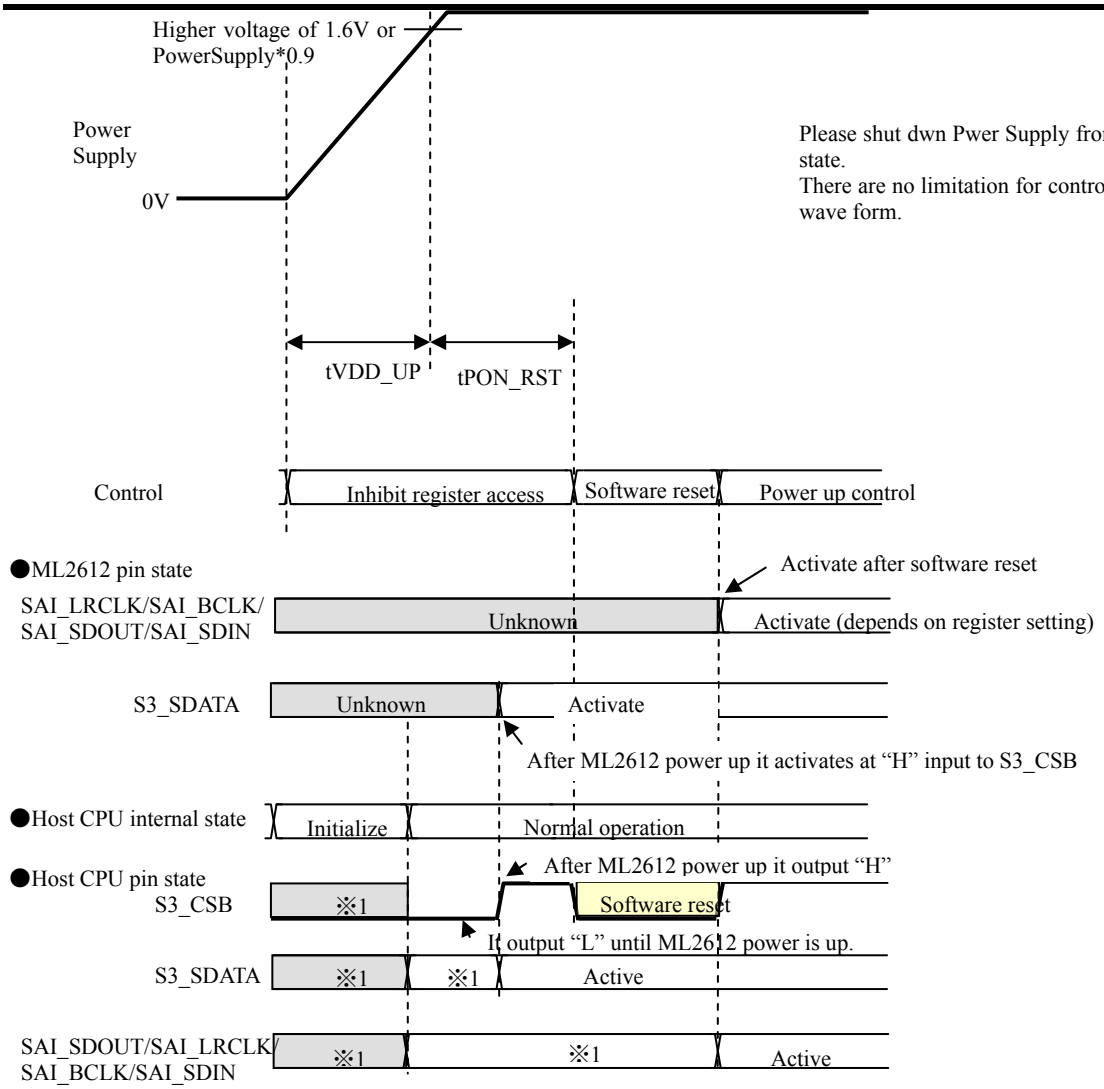
Power Supply Sequence

Please power on/off the LSI with all kind of power at the same time. Each power supply should power up/down in 50ms.Also keep all power supply in the ON state or the OFF state. Please avoide partial ON or partial OFF status.

All of the LSI circuit is initialized by power on reset when power on. To be a certain operation of Power On Reset, Please start VDD level from 0V(GND level).
After power on, this LSI can be controled from the time passed Reset Time(t_{PON_RST}).
All of the pins status are Hi-Z during Power On Reset.

Parameter	Symbol	Min	Typ	Max	Unit
Power On Delay Time	t_{VDD_ON}	0	—	50	ms
Power Off Delay Time	t_{VDD_OFF}	0	—	50	ms
Power Up Time	t_{VDD_UP}	—	—	10	ms
Reset Time after Power On	t_{PON_RST}	—	—	150	ms





※1 Input or PullUP or PullDown

Analog Characteristics

The following specification is only guarantied when specification is optimized by using ML2612 family Trimming Registers.

(LVDD=1.65~2.75V, HVDD=2.7~3.6V, Ta=-20~+85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Line Input						
Full Scale Input Signal Level	V_{LINFS}	LIN	—	—	0.7x LVDD	Vp-p
Input Resistance	R_{LIN}	—	15	20	25	kΩ
Mic Input						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	V_{MINFS}	MIN-	—	—	0.7x LVDD	Vp-p
		MIN+	—	—	0.4	Vp-p
Input Resistance MIN-	R_{MIN-}	PGA Volume = +35.25dB	0.6	1.5	—	kΩ
		PGA Volume = 0dB	—	44.2	—	kΩ
		PGA Volume = -12dB	—	70.7	88.4	kΩ
Input Resistance MIN+	R_{MIN+}	—	66.3	88.4	111.5	kΩ
Line OUT(SPOUT+, with 10kΩ /50pF load)						
Full Scale Output Signal Level (for 0dB Input at 0dB Gain)	V_{LOUTFS}	DAC to Line OUT	0.591x LVDD	0.695x LVDD	0.766x LVDD	Vp-p
		Lin to Line OUT	0.667x LVDD	0.785x LVDD	0.867x LVDD	Vp-p
Analog Reference Level(VMID-pin)						
Analog Reference Voltage	V_{REF}	—	0.90x LVDD/2	LVDD/2	1.10x LVDD/2	V
Microphone Bias(MICBIAS-pin)						
Output Voltage Vmic<HVDD*0.85	V_{MIC}	IMIC =1mA, VBCON=0 Vmic<HVDD*0.85	1.12x LVDD/2	1.25x LVDD/2	1.38x LVDD/2	V
		IMIC =1mA, VBCON=1 Vmic<HVDD*0.85	1.21x LVDD/2	1.35x LVDD/2	1.49x LVDD/2	V
		IMIC =1mA, VBCON=2 Vmic<HVDD*0.85	1.44x LVDD/2	1.60x LVDD/2	1.76x LVDD/2	V
		IMIC =1mA, VBCON=3 Vmic<HVDD*0.85	1.48x LVDD/2	1.65x LVDD/2	1.82x LVDD/2	V
		IMIC =1mA, VBCON=4 Vmic<HVDD*0.85	1.66x LVDD/2	1.85x LVDD/2	2.04x LVDD/2	V
		IMIC =1mA, VBCON=5 Vmic<HVDD*0.85	1.84x LVDD/2	2.05x LVDD/2	2.26x LVDD/2	V
		IMIC =1mA, VBCON=6 Vmic<HVDD*0.85	2.20x LVDD/2	2.45x LVDD/2	2.70x LVDD/2	V
		IMIC =1mA, VBCON=7 Vmic<HVDD*0.85	2.52x LVDD/2	2.80x LVDD/2	3.08x LVDD/2	V
Output Current	I_{MIC}	—	—	—	2	mA

(LVDD=2.5V, HVDD=3.3V, Ta=25°C, 1kHz signal, fs=48kHz)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Analog Inputs to ADC out						
Signal to Noise Ratio	SNR	A-weighted Speaker Amp Off *1	—	90	—	dB
Total Harmonic Distortion	THD	1kHz,input-3dBFS Speaker Amp Off *1	—	86	—	dB
Power Supply Rejection Ratio	PSRR	LVDD on 100mVp-p, 10kHz noise, no signal input	—	40	—	dB
DAC to Line OUT(SPOUT+, with 10kΩ /50pF load)						
Total Harmonic Distortion	THD	1kHz,input 0dBFS	—	60	—	dB
Signal to Noise Ratio	SNR	A-weighted	—	94	—	dB
Power Supply Rejection Ratio	PSRR	HVDD on 100mVp-p,10kHz noise, no signal input	—	50	—	dB
		LVDD on 100mVp-p,10kHz noise, no signal input	—	35	—	dB
DAC to Speaker OUT(SPOUT+/-, with 8Ω /50pF load)						
Output Power	Po	THD=10%	—	420	—	mW
Total Harmonic Distortion	THD	Po=310mW, 1kHz signal	—	40	—	dB
Signal to Noise Ratio	SNR	A-weighted	—	84	—	dB
Power Supply Rejection Ratio	PSRR	HVDD on 100mVp-p,10kHz noise	—	60	—	dB
		LVDD on 100mVp-p,10kHz noise	—	35	—	dB
Microphone Bias(MICBIAS-pin)						
Output Noise Voltage	V_{MICN}	22Hz to 22kHz, V_{MIC} =1.6 x V_{REF}	—	8.2	—	uV
Power Supply Rejection Ratio	PSRR	HVDD on 100mVp-p,10kHz noise	—	60	—	dB

*1 Speaker Amplifier Power Management Register($26h/$27h) SPCON = 00h

Digital Filter Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ADC Decimation Filter						
Passband	DM_{PS1}	+/-0.05dB	0	—	0.455fs	—
	DM_{PS2}	-6dB	—	0.5fs	—	—
Passband Ripple	DM_{lp1}		-0.05	—	+0.05	dB
Stopband	DM_{st1}		0.5465fs			—
Stopband Attenuation	DM_{at1}	0.5465fs<Freq	-56			dB
Group Delay	DM_{gd1}		—	20fs	—	—
ADC High Pass Filter 1 (DC-Cut)						
Corner Frequency	$HP1_{f1}$	-3dB, fs=48kHz	—	3.744	—	Hz
	$HP1_{f2}$	-0.5dB, fs=48kHz	—	10.656	—	Hz
	$HP1_{f3}$	-0.1dB, fs=48kHz	—	24.192	—	Hz
DAC Interpolation Filter						
Passband	IT_{PS1}	+/-0.03dB	0	—	0.452fs	—
	IT_{PS2}	-6dB	—	0.5fs	—	—
Passband Ripple	IT_{lp1}		-0.03	—	+0.03	dB
Stopband	IT_{st1}		0.5488fs			—
Stopband Attenuation	IT_{at1}	0.5488fs<Freq	-54			dB
Group Delay	IT_{gd1}		—	18fs	—	—

Note) $HP1_{f1}$, $HP1_{f2}$ and $HP1_{f3}$ are in proportion to fs

Revision history

Date	Page	Notes	Revision
07/05/15	All	Preliminary datasheet Release	1.0
07/06/19	All	Delete ML2613 and ML2615	1.2
07/06/19	3	Add Sampling Frequency 12kHz	1.2
07/06/19	14	Change Power Consumption value	1.2
07/06/19	18	Add t_{D_SDO} Condition	1.2
07/06/19	21	Change Power up time MAX value	1.2
07/06/19	23	Change Analog Characteristics condition and value	1.2
07/09/07	12	Absoute Maximum Rating: Delete (T.B.D.) for Powwer Disipation and add Output Current.	2
07/09/07	13	Change operating current value amd delete (T.B.D.)	2
07/09/07	15	Change MCLKI Length Min value	2
07/09/07	21	Change Pwer Up Time and Reset Time after Power On	2
07/09/07	22	Change Power Supply Sequence	2
07/09/07	23	Change Analog Characteristics	2
07/09/07	25	Digital Filter Characteristics: Change value and delete (T.B.D.)	2
07/10/31	3	Change General Description	3
07/10/31	23	Change Analog Characteristics(RMIN+, VLOUTFS)	3

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