Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (Vcc = 4.5 V to 5.5 V)**
  - **3.0 V (Vcc = 2.7 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Three-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **8-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages**

3-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Preliminary

Description

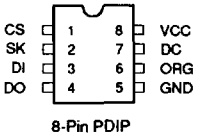
The AT93C46/56/66 provides 1024/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to Vcc and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/66 is available in space saving 8-pin PDIP and 8-pin JEDEC and EIAJ SOIC packages.

The AT93C46/56/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

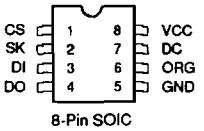
Atmel's E²PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT93C46/56/66 is available in 5.0 V ± 10% and 2.7 Vto 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
DC	Don't Connect

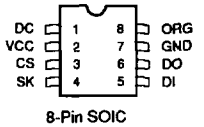


8-Pin PDIP



8-Pin SOIC

Rotated (R)
(1K JEDEC Only)



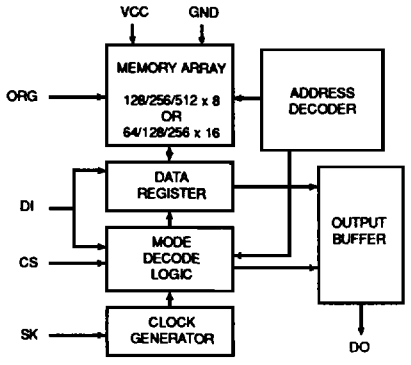
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

D.C. Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.7 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +2.7 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{IH},	SK = 1.0 MHz(1) SK = 0.5 MHz(1)		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH},	SK = 1.0 MHz(1) SK = 0.5 MHz(1)		3 3	mA
I_{CC3}	Standby Current	CS = 0 V	SK = 1.0 MHz(1) SK = 0.5 MHz(1)		100 100	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}		-2.5 -10	2.5 10	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}		-2.5 -10	2.5 10	µA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V		-0.1 2	0.6 VCC + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 2.1 mA I_{OH} = -400 µA		 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 10 µA I_{OH} = -10 µA		 V_{CC} - 0.2	0.2	V V

Note: 1. Devices operate at 1.0 MHz at VCC = 5.0 V ± 10% at commercial temperature. All low voltage and industrial parts operate at 0.5 MHz.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.7 V to +5.5 V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
f_{SK}	SK Clock Frequency		0 0	1 0.5	MHz
t_{SKH}	SK High Time	Note 1 Note 2	500 500		ns
t_{SKL}	SK Low Time	Note 1 Note 2	250 500		ns
t_{CS}	Minimum CS Low Time	Note 3 Note 4	250 500		ns
t_{CSS}	CS Setup Time	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time	Relative to SK	0		ns
t_{DIH}	DI Hold Time	Relative to SK	100 200		ns
t_{PD1}	Output Delay to '1'	AC Test		500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	AC Test		500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time			10	ms
	Endurance	Number of Data Changes per Bit	Typical 100,000		Cycles

Notes:
1. The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 µs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 µs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.
2. The SK frequency specification for extended Temperature parts specifies a minimum SK clock period of 2 µs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 µs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 µs in order to meet the SK frequency specification.
3. For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.
4. For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT93C46/56/66 is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by 7 instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Instruction Set for the AT93C46

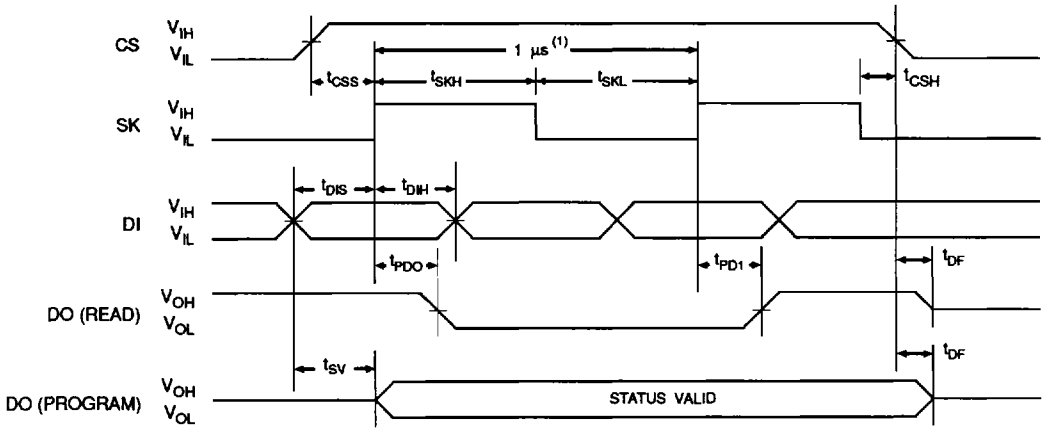
Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6-A_0	A_5-A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXX	01XXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8-A_0	A_7-A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



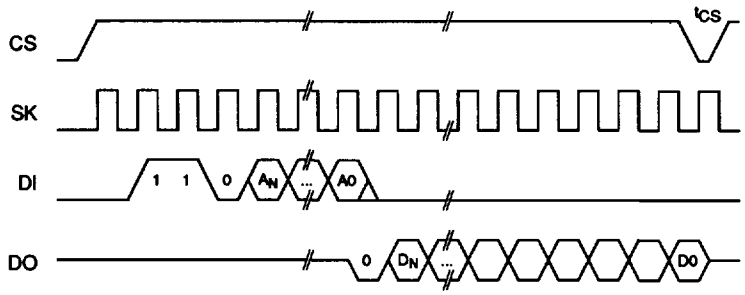
Note: 1. This is the minimum SK period.

Organization Key for Timing Diagrams

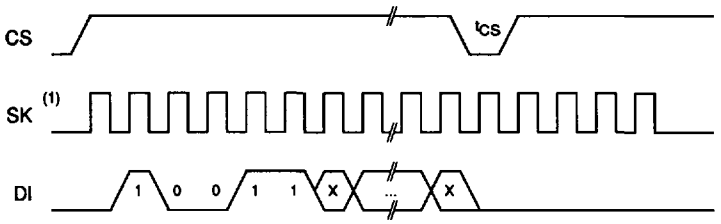
I/O	Density 1K x 8	Density 1K x 16	Density 2K x 8	Density 2K x 16	Density 4K x 8	Density 4K x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

Timing Diagrams (Continued)

READ Timing

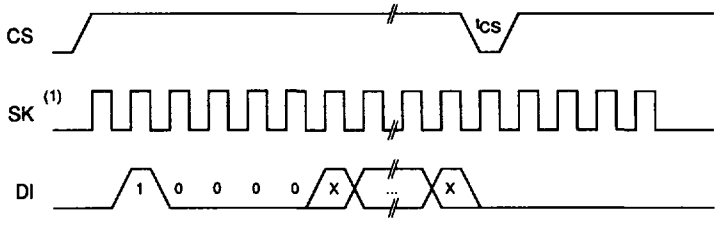


EWEN Timing



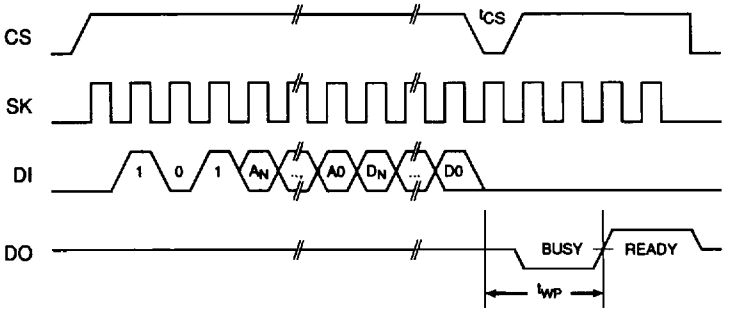
Note: 1. The AT93C56 and AT93C66 require a minimum of 11 clocks. The AT93C46 requires a minimum of 9 clock cycles.

EWDS Timing



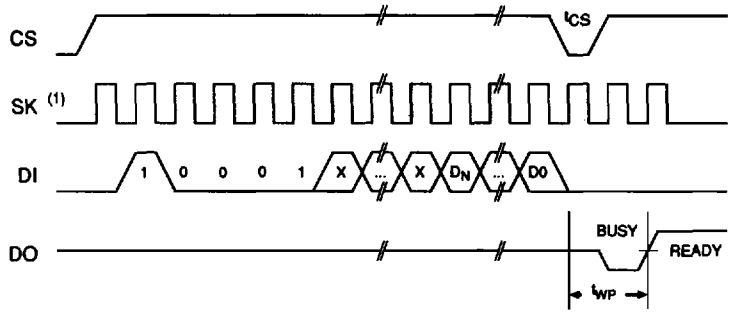
Note: 1. The AT93C56 and AT93C66 require a minimum of 11 clocks. The AT93C46 requires a minimum of 9 clock cycles.

WRITE Timing



Timing Diagrams (Continued)

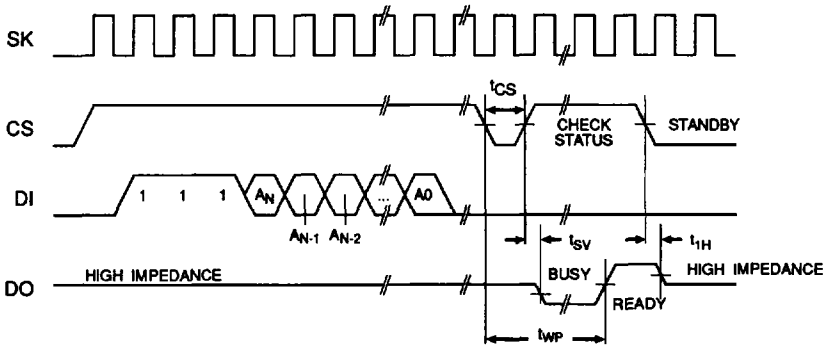
WRAL Timing [2]



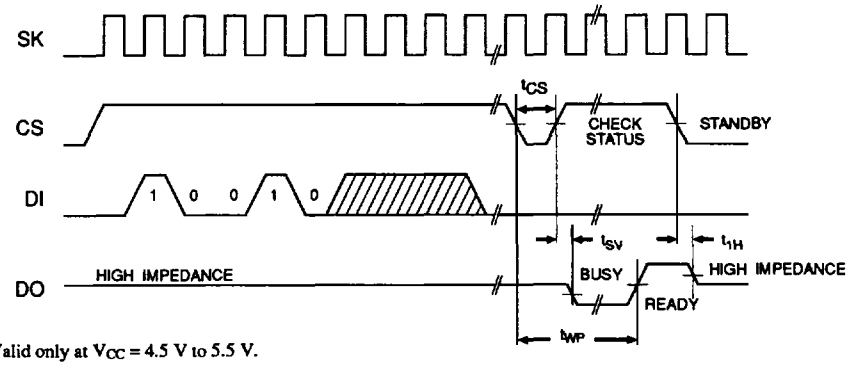
Notes: 1. The AT93C56 and AT93C66 require a minimum of 11 clocks. The AT93C46 requires a minimum of 9 clock cycles.

2. Valid only at V_{CC} = 4.5 V to 5.5 V.

ERASE Timing



ERAL Timing [1]



Note: 1. Valid only at V_{CC} = 4.5 V to 5.5 V.

Ordering Information

t_{WP} (ms)	I_{CC} (mA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3.0	1000	AT93C46-10PC (-2.7) AT93C46-10SC (-2.7) AT93C46R-10SC (-2.7) AT93C46W-10SC (-2.7)	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
			AT93C46-10PI (-2.7) AT93C46-10SI (-2.7) AT93C46R-10SI (-2.7) AT93C46W-10SI (-2.7)	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
			AT93C46-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT93C56-10PC (-2.7) AT93C56-10SC (-2.7) AT93C56W-10SC (-2.7)	8P3 8S1 8S2	Commercial (0°C to 70°C)
			AT93C56-10PI (-2.7) AT93C56-10SI (-2.7) AT93C56W-10SI (-2.7)	8P3 8S1 8S2	Industrial (-40°C to 85°C)
			AT93C56-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT93C66-10PC (-2.7) AT93C66-10SC (-2.7) AT93C66W-10SC (-2.7)	8P3 8S1 8S2	Commercial (0°C to 70°C)
			AT93C66-10PI (-2.7) AT93C66-10SI (-2.7) AT93C66W-10SI (-2.7)	8P3 8S1 8S2	Industrial (-40°C to 85°C)
			AT93C66-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
R	Rotated Pinout