NTF6P02, NVF6P02

Power MOSFET
-10 Amps, -20 Volts

P−Channel SOT−223

ON Semiconductor®

http://onsemi.com

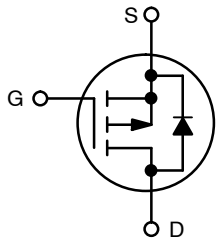
−10 AMPERES
−20 VOLTS
$R_{DS(on)}$ = 44 mΩ (Typ.)

Features

- Low $R_{DS(on)}$
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- NVF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable*
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Power Management in Portables and Battery−Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards



P−Channel MOSFET

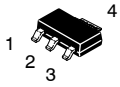
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−20	Vdc
Gate−to−Source Voltage	V_{GS}	±8.0	Vdc
Drain Current (Note 1) − Continuous @ T_A = 25°C − Continuous @ T_A = 70°C − Single Pulse (t_p = 10 μs)	 I_D I_D I_{DM}	 −10 −8.4 −35	 Adc Apk
Total Power Dissipation @ T_A = 25°C	P_D	8.3	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −20 Vdc, V_{GS} = −5.0 Vdc, $I_{L(pk)}$ = −10 A, L = 3.0 mH, R_G = 25Ω)	E_{AS}	150	mJ
Thermal Resistance − Junction to Lead (Note 1) − Junction to Ambient (Note 2) − Junction to Ambient (Note 3)	 $R_{\theta JL}$ $R_{\theta JA}$ $R_{\theta JA}$	 15 71.4 160	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

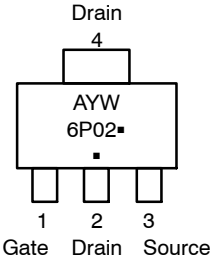
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Steady State.
2. When surface mounted to an FR4 board using 1” pad size, (Cu. Area 1.127 sq in), Steady State.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu. Area 0.412 sq in), Steady State.

MARKING DIAGRAM & PIN ASSIGNMENT



SOT−223
CASE 318E
STYLE 3



A	= Assembly Location
Y	= Year
W	= Work Week
6P02	= Specific Device Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTF6P02T3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NVF6P02T3G*	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Note 4) (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	−20 −	−25 −11	− −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = −20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = −20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)	I_{DSS}	− −	− −	−1.0 −10	μAdc
Gate−Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	−	−	± 100	nAdc
ON CHARACTERISTICS (Note 4)					
Gate Threshold Voltage (Note 4) (V_{DS} = V_{GS}, I_D = −250 μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	−0.4 −	−0.7 2.6	−1.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 4) (V_{GS} = −4.5 Vdc, I_D = −6.0 Adc) (V_{GS} = −2.5 Vdc, I_D = −4.0 Adc) (V_{GS} = −2.5 Vdc, I_D = −3.0 Adc)	$R_{DS(on)}$	− − −	44 57 57	50 70 −	mΩ
Forward Transconductance (Note 4) (V_{DS} = −10 Vdc, I_D = −6.0 Adc)	g_{fs}	−	12	−	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = −16 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	−	900	1200	pF
Output Capacitance		C_{oss}	−	350	500	
Transfer Capacitance		C_{rss}	−	90	150	
Input Capacitance	(V_{DS} = −10 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	−	940	−	pF
Output Capacitance		C_{oss}	−	410	−	
Transfer Capacitance		C_{rss}	−	110	−	
SWITCHING CHARACTERISTICS (Note 5)						
Turn−On Delay Time	(V_{DD} = −5.0 Vdc, I_D = −1.0 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	7.0	12	ns
Rise Time		t_r	−	25	45	
Turn−Off Delay Time		$t_{d(off)}$	−	75	125	
Fall Time		t_f	−	50	85	
Turn−On Delay Time	(V_{DD} = −16 Vdc, I_D = −6.0 Adc, V_{GS} = −4.5 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	−	8.0	−	ns
Rise Time		t_r	−	30	−	
Turn−Off Delay Time		$t_{d(off)}$	−	60	−	
Fall Time		t_f	−	60	−	
Gate Charge	(V_{DS} = −16 Vdc, I_D = −6.0 Adc, V_{GS} = −4.5 Vdc) (Note 4)	Q_T	−	15	20	nC
		Q_{gs}	−	1.7	−	
		Q_{gd}	−	6.0	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = −3.0 Adc, V_{GS} = 0 Vdc) (Note 4) (I_S = −2.1 Adc, V_{GS} = 0 Vdc) (I_S = −3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	− − −	−0.82 −0.74 −0.68	−1.2 − −	Vdc
Reverse Recovery Time	(I_S = −3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 4)	t_{rr}	−	42	−	ns
		t_a	−	17	−	
		t_b	−	25	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.036	−	μC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

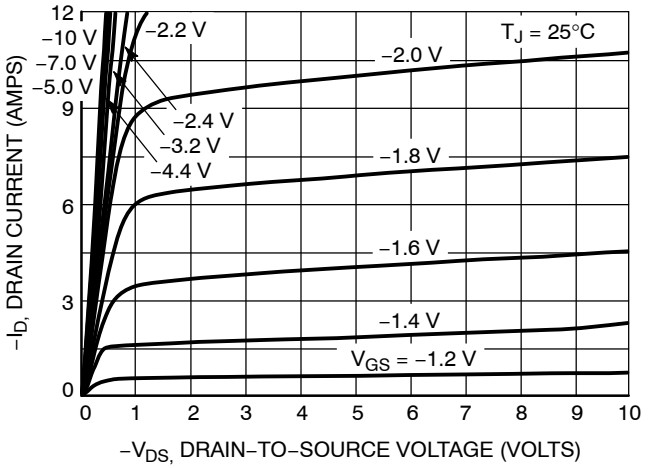


Figure 1. On−Region Characteristics

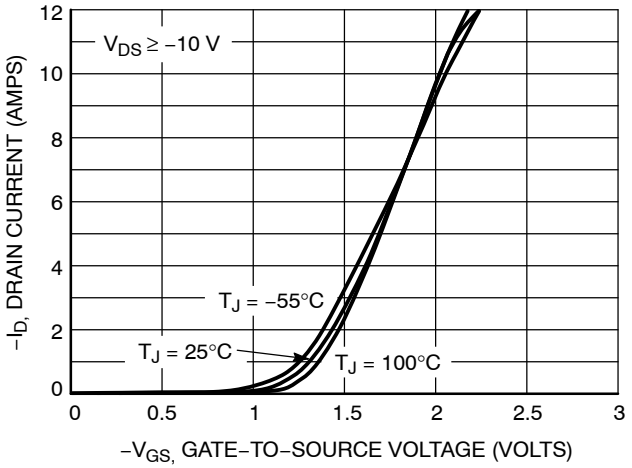


Figure 2. Transfer Characteristics

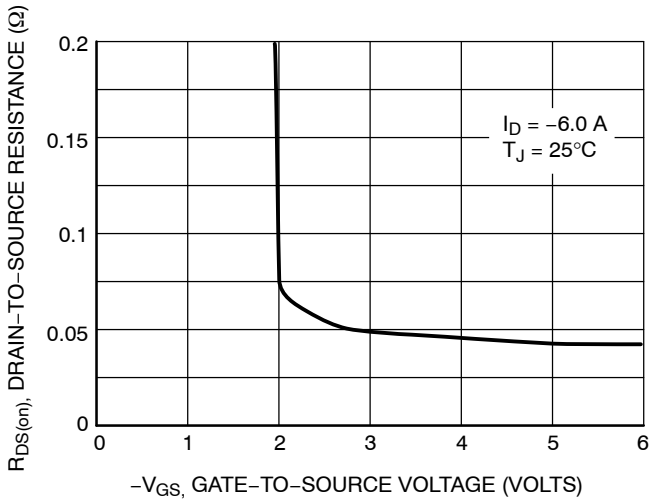


Figure 3. On−Resistance versus Gate−to−Source Voltage

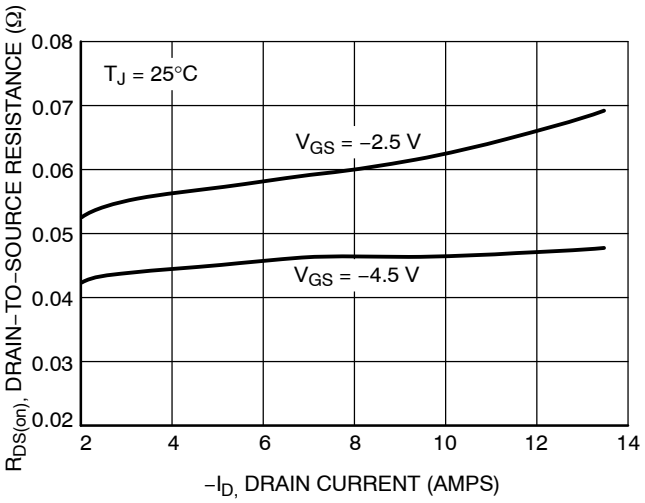


Figure 4. On−Resistance versus Drain Current and Gate Voltage

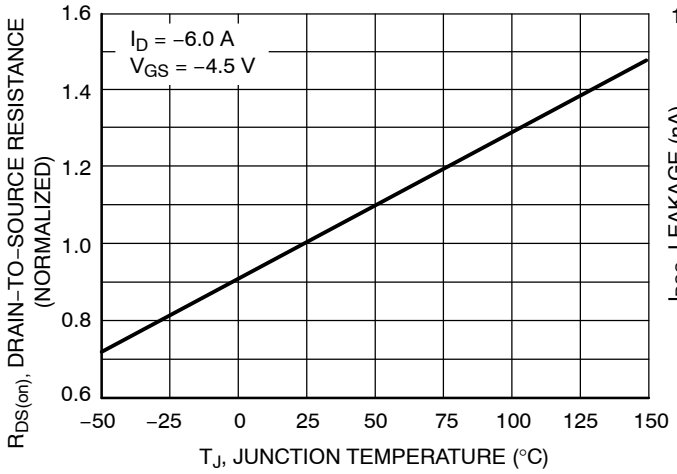


Figure 5. On−Resistance Variation with Temperature

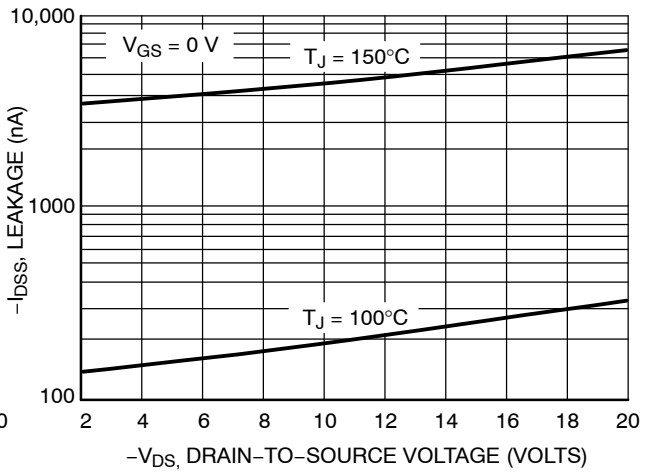


Figure 6. Drain−to−Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

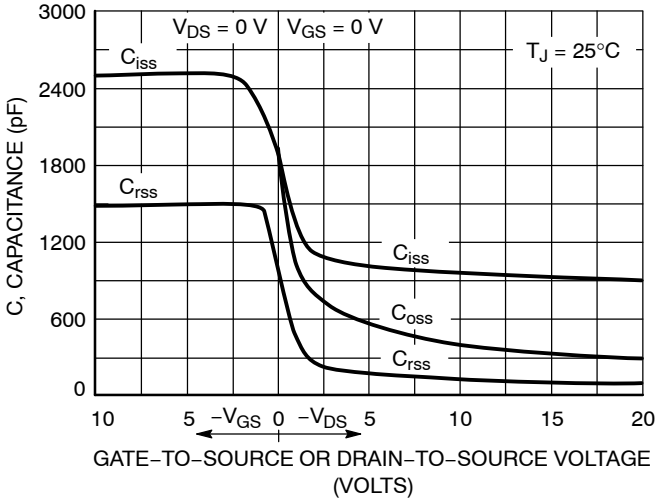


Figure 7. Capacitance Variation

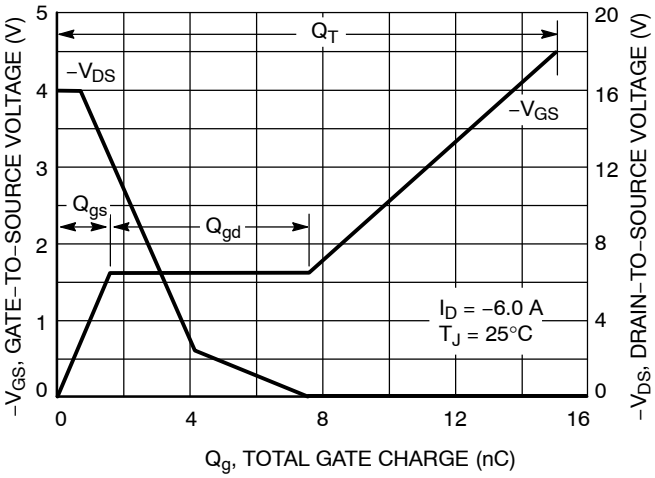


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

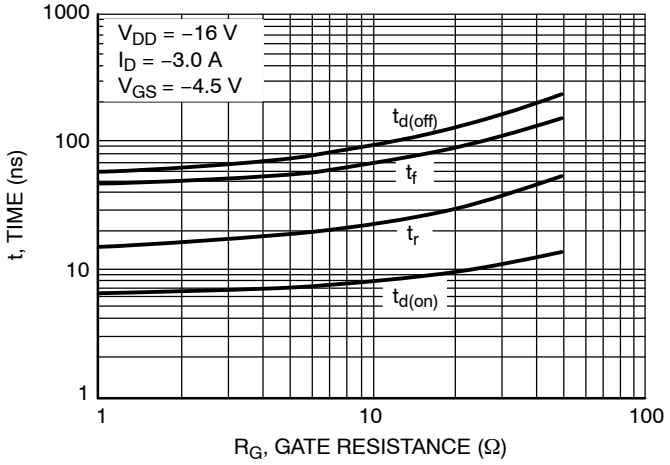


Figure 9. Resistive Switching Time Variation versus Gate Resistance

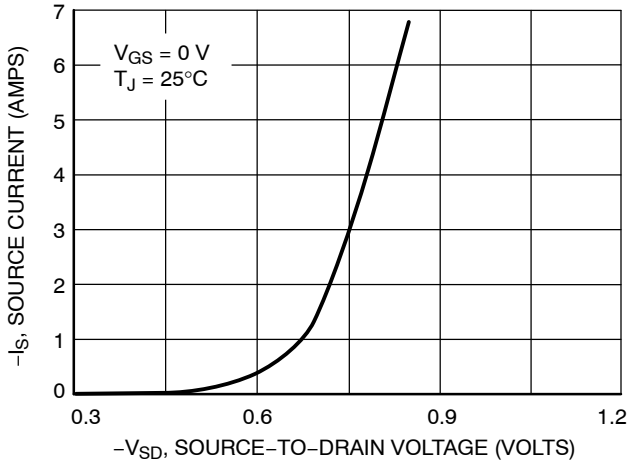


Figure 10. Diode Forward Voltage versus Current

TYPICAL ELECTRICAL CHARACTERISTICS

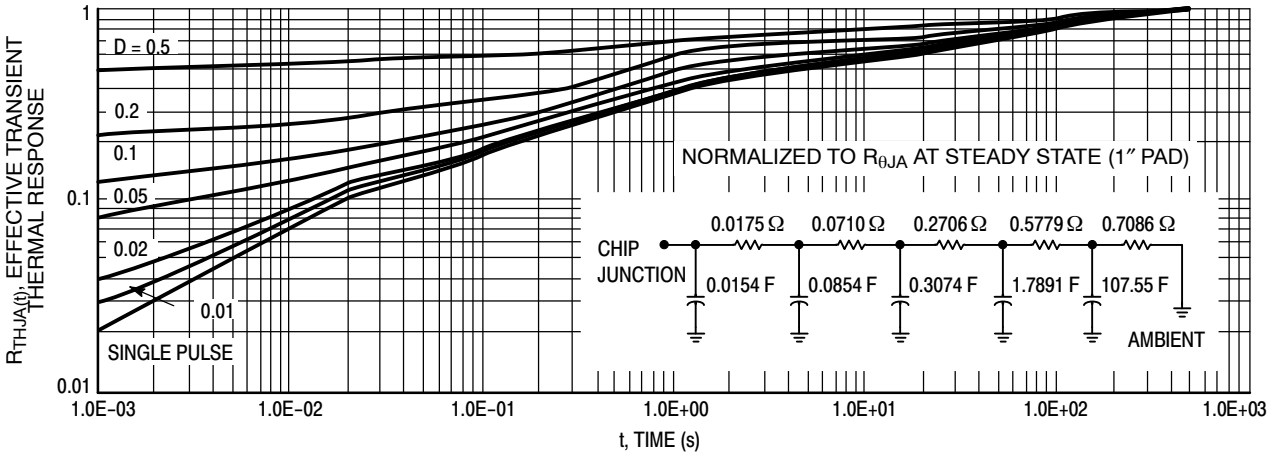
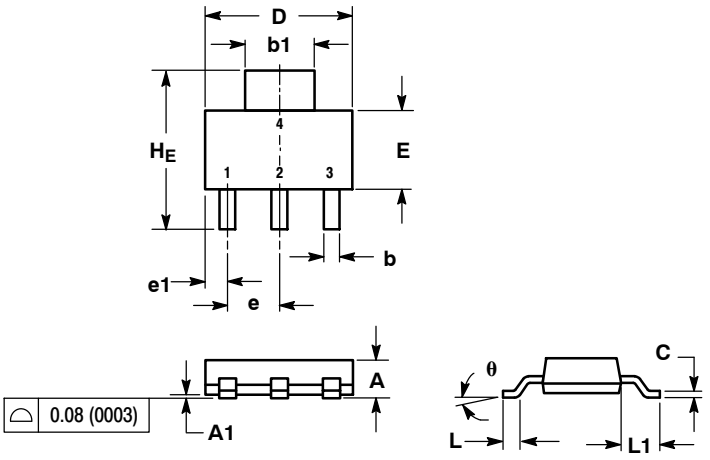


Figure 11. FET Thermal Response

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

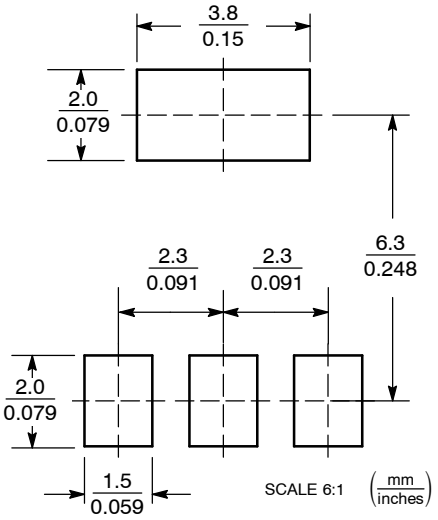


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	−−−	−−−	0.008	−−−	−−−
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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