

54AC/74AC398 • 54ACT/74ACT398
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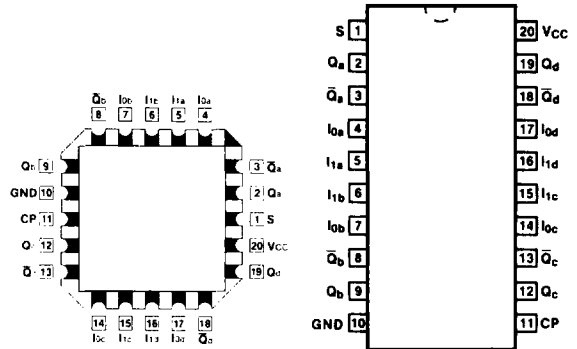
Quad 2-Port Register

Description

The 'AC/ACT398 and 'AC/ACT399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock. The 'AC/ACT399 is the 16-pin version of the 'AC/ACT398, with only the Q outputs of the flip-flops available.

- Select Inputs from Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complement Outputs—'AC/ACT398
- Outputs Source/Sink 24 mA
- 'ACT398 and 'ACT399 have TTL-Compatible Inputs

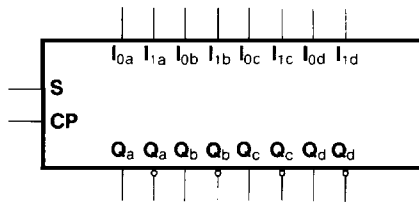
Connection Diagrams



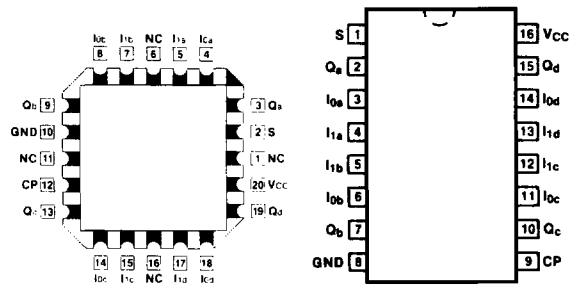
'AC/ACT398

Ordering Code: See Section 6

Logic Symbols



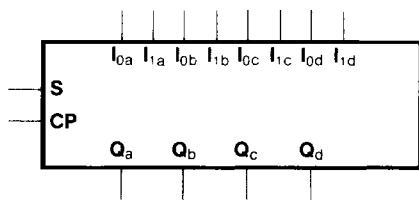
'AC/ACT398



'AC/ACT399

Pin Assignment
for LCC

Pin Assignment
for DIP, Flatpak and SOIC



'AC/ACT399

Pin Names

- S Common Select Input
- CP Clock Pulse
- I0a - I0d Data Inputs from Source 0
- I1a - I1d Data Inputs from Source 1
- Qa - Qd Register True Outputs
- Qa-bar - Qd-bar Register Complementary Outputs ('AC/ACT398)

Functional Description

The 'AC/ACT398 and 'AC/ACT399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x} , I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'AC/ACT398 has both Q and \bar{Q} outputs.

Function Table

Inputs				Outputs	
S	I_0	I_1	CP	Q	\bar{Q}^*
L	L	X	⌄	L	H
L	H	X	⌄	H	L
H	X	L	⌄	L	H
H	X	H	⌄	H	L

H = HIGH Voltage Level

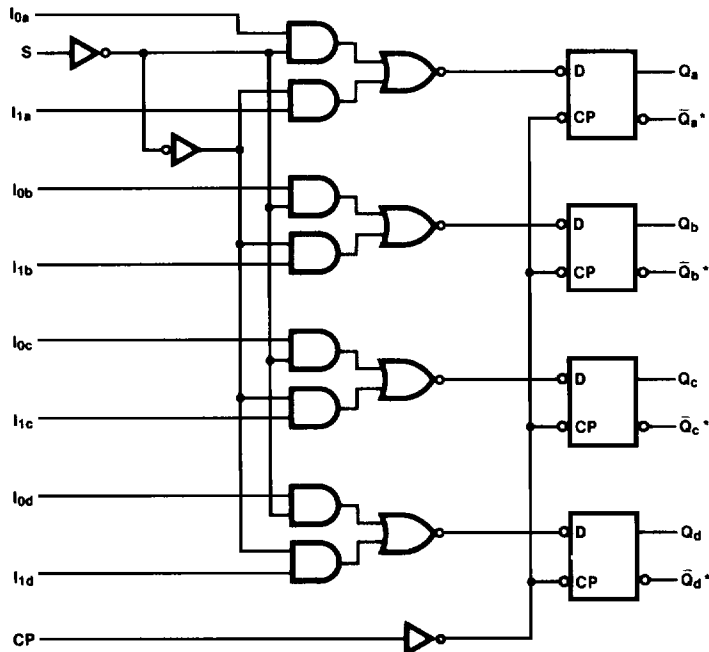
L = LOW Voltage Level

X = Immaterial

⌄ = LOW-to-HIGH Clock Transition

* = 'AC/ACT398 only

Logic Diagram



**AC/ACT398 only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input (ACT398/399)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Input Clock Frequency	3.3 5.0	160	160					MHz	3-3	
t _{PLH}	Propagation Delay CP to Q ₀ or \bar{Q}	3.3 5.0	9.5	7.0					ns	3-6	
t _{PHL}	Propagation Delay CP to Q ₀ or \bar{Q}	3.3 5.0	8.5	6.0					ns	3-6	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC	74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum					
ts	Setup Time, HIGH or LOW In to CP	3.3 5.0	4.5 3.0					ns	3-9
th	Hold Time, HIGH or LOW In to CP	3.3 5.0	0 0					ns	3-9
ts	Setup Time, HIGH or LOW S to CP (*398)	3.3 5.0	4.5 3.0					ns	3-9
ts	Setup Time, HIGH or LOW S to CP (*399)	3.3 5.0	4.5 3.0					ns	3-9
th	Hold Time, HIGH or LOW S to CP	3.3 5.0	-1.5 -1.0					ns	3-9
tw	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0					ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Input Clock Frequency	5.0		160					MHz	3-3	
tPLH	Propagation Delay CP to Q or Q̄	5.0		7.0					ns	3-6	
tPHL	Propagation Delay CP to Q or Q̄	5.0		6.0					ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum					
ts	Setup Time, HIGH or LOW In to CP	5.0	3.0					ns	3-9
th	Hold Time, HIGH or LOW In to CP	5.0	0					ns	3-9
ts	Setup Time, HIGH or LOW S to CP ('398)	5.0	3.0					ns	3-9
ts	Setup Time, HIGH or LOW S to CP ('399)	5.0	3.0					ns	3-9
th	Hold Time, HIGH or LOW S to CP	5.0	-1.0					ns	3-9
tw	CP Pulse Width HIGH or LOW	5.0	5.5					ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance		pF	Vcc = 5.5 V