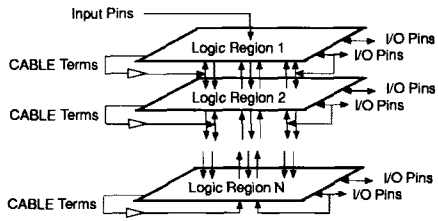
Features

- **High Throughput - Uniform and Predictable Performance**
- **High I/O Pin Counts**
- **High Speed - Over 80 MHz System Clock Rate Operation**
- **Flexible Interconnect Architecture - Universal Routing**
- **Multiple Flip-Flop Types - Synchronous or Asynchronous Registers**
- **Complete Third Party Software Support**
  - **No Placement, Routing or Layout Software Required**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **Commercial, Industrial and Military Temperature Grades**

Block Diagram



Description

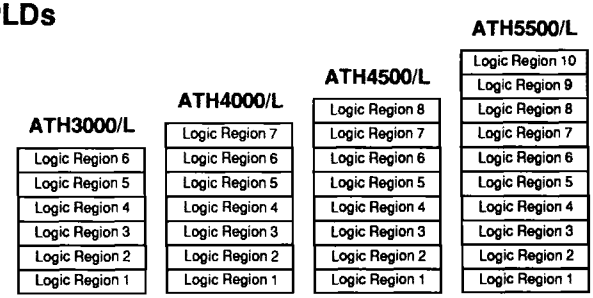
The Atmel H-Series Programmable Logic Devices are easy to use, high throughput devices. Their simple, regular architecture translates into increased utilization and high performance.

The Atmel H-Series EPLDs have one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. Sum terms, which are easy to use blocks of gates, provide combinatorial AND/OR logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. Sum terms or registers can drive the I/O pins.

All registers are configurable as D- or T-types without using extra logic gates. Individual sum terms and clocks give each flip-flop added flexibility. A direct "clock-from-pin" option guarantees synchronization and fast clock to output performance.

(Continued on next page)

H-Series EPLDs



Part Number	ATH3000/L	ATH4000/L	ATH4500/L	ATH5500/L
Pins	68	84	100	132
I/Os	56	68	80	100
Flip-Flops	56	70	80	100
Logic Regions	6	7	8	10

High Throughput UV Erasable Programmable Logic Devices

H-Series EPLDs Overview

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Description (Continued)

Standard off-the-shelf third party software tools and programmers support the H-Series. This minimizes start-up investment and improves product support.

The H-Series addresses applications that need high-frequency operation and a high I/O pin count. It achieves predictably high throughput rates over a wider range of designs than has been possible in the past through the use of innovative architecture and logic cell design. A logic cell with many possible configurations gives a finer logic granularity and maximizes logic resource usage. Complement Array Buried Logic Extender (CABLE) terms increase the connectivity between logic regions. Additional logic increases the number of input terms available to sum terms without degrading performance.

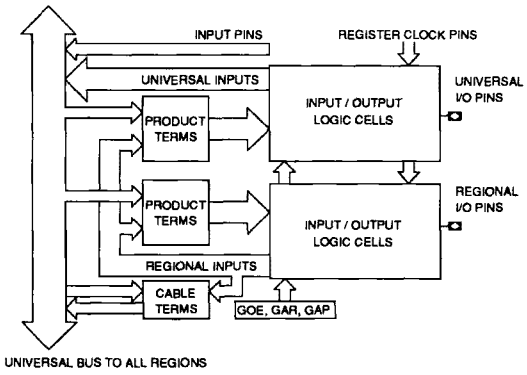
Logic Array Architecture

The block diagram shows the basic structure of the H-Series devices. Like the ATV5000 device currently available from Atmel, the H-Series uses regions within the device. Each region consists of a group of logic cells, CABLE terms, and a programmable AND logic array. Figure 1 shows that regional logic cells generate inputs that feed that region's AND logic array. Universal logic cells generate input that feed into the universal AND array, which provides interconnect to other regions.

The AND logic array for each region receives inputs from four different sources. These include the inputs from each logic cell within the region, from dedicated universal input pins, from universal logic cells, and from CABLE terms.

Each region's AND array provides complete interconnect for signals within that region. In addition, any product terms within a given region also have inputs available as the signals on the universal bus.

Figure 1. Functional Logic Diagram



Logic Cell Architecture

In the H-Series, each logic cell has eight product terms and generates one array feedback term. The product terms provide two three-inputs sum terms, a clock term, and an output enable term. Programmable switches combine sum terms with each other, and with sum terms from adjacent logic cells. This sum term joining is similar to Atmel's V-Series devices, and allows up to 12 product terms with no delay penalty. To further aid logic fit-

Node Feedbacks

Figure 2a. Registered Output, Combined Terms

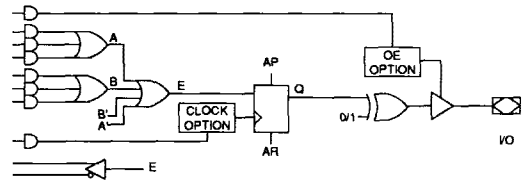


Figure 2b. Registered Output, Separate Terms

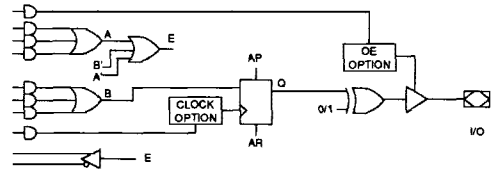


Figure 2c. Combinatorial Output, Combined Terms

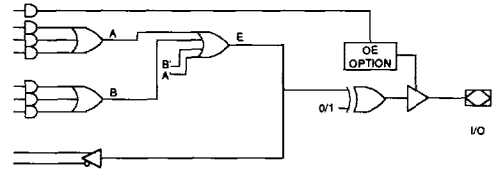
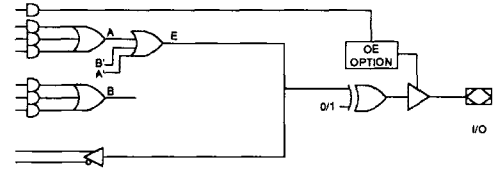


Figure 2d. Combinatorial Output, Separate Terms



ting, sum term joining also operates across region boundaries for two adjoining cells that lie in different regions.

The H-Series logic cell contains a single flip-flop which may be configured as D- or T-Type. Figures 2, 3 and 4 shows the logic cell's possible configurations. Modes are distinguished by output type (registered or combinatorial), feedback source (pin, register, or combinatorial node), and sum term configuration (combined or separate). Atmel's V-Series devices have featured two or three basic modes, whereas the H-Series breaks the logic cell down into smaller elements that may be utilized separately. This finer granularity allows higher gate utilization, while the reduced amount of interconnect guarantees high performance for all applications.

Register Feedbacks

Figure 3a. Register Output, Combined Terms

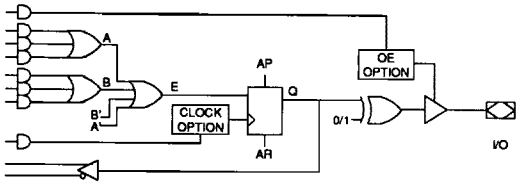


Figure 3b. Register Output, Separate Terms

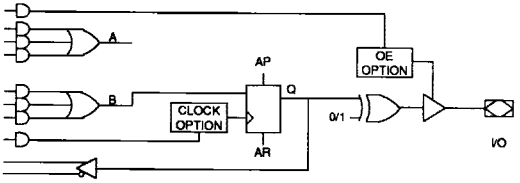


Figure 3c. Combinatorial Output, Combined Terms

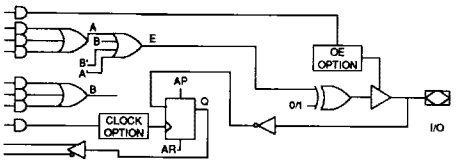
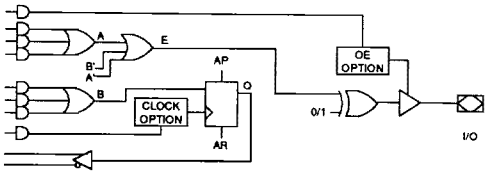


Figure 3d. Combinatorial Output, Separate Terms



Pin Feedbacks

Figure 4a. Register Output, Combined Terms

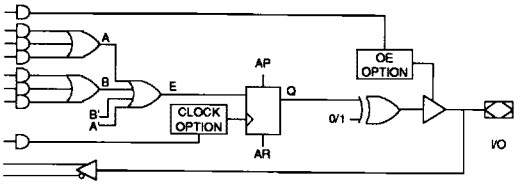


Figure 4b. Register Output, Separate Terms

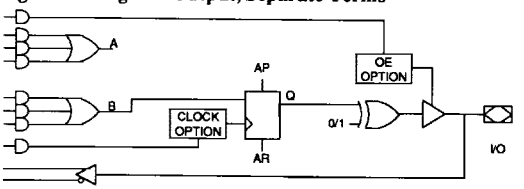


Figure 4c. Combinatorial Output, Combined Terms

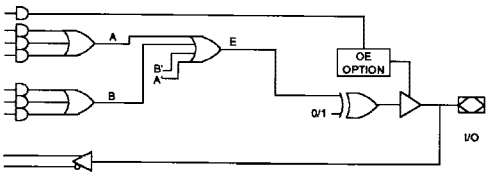
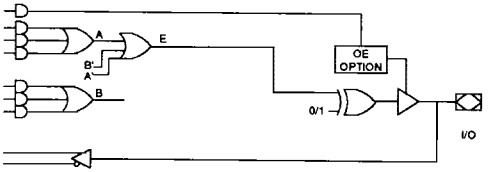


Figure 4d. Combinatorial Output, Separate Terms



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The flip-flop clock option has three modes as shown in Figure 5, and is identical to the clock option used on the ATV5000. The clock product term controls asynchronous operation. A regional clock pin controls synchronous operation. Asynchronous clock gating is possible by ANDing the regional clock pin with the clock product term. As with the ATV5000, using the regional clock input pin results in faster clock-to-output delays than the product terms clock input.

The output enable function has three modes as shown in Figure 6. The output enable comes from the logic cell OE product term, a regional OE term, or an OR function of these. This last option realizes an AND/OR output enable control and uses only one product term per logic cell for this function.

Figure 5. Clock Option

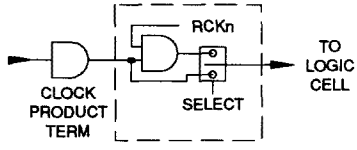
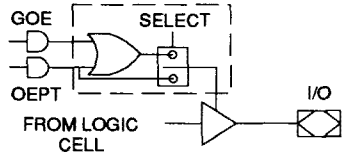


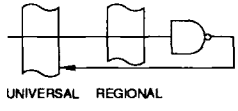
Figure 6. OE Option



CABLE Terms

Figure 7 shows the CABLE logic extender term structure. Each term receives all of the AND array inputs in one region. The NAND output is an output to the ANDs of multiple regions. This technique provides an additional interconnect mechanism between regions, allowing regional signals to be combined and fed onto the universal bus.

Figure 7. CABLE Term Schematic



Applications

The H-Series is ideal for applications requiring high speed and where most logic needs to be accessible to the rest of the system. Examples of such applications include:

- Decoders
- Serial-to-Parallel Data Conversion
- DMA Address Counters
- Integration of Multiple Small PLD Designs
- Signal Synchronization

Decoders are well-suited to the H-Series architecture, as they generally have a modest number of address inputs and a few control inputs. A single region can hold most normal bank decode logic, and if more address inputs are needed, another region could be used with CABLE term interconnection.

Serial-to-parallel data conversion is a natural for the H-Series. Because there is always at least one universal pin in every region, shift registers of any width can be built that operate at the device's maximum clock rate. Since every flip-fop has an output pin available to it, the converted data will be available for the system to read immediately.

DMA address counters also need their outputs available for use in the system, so the availability of I/O pins in H-Series devices again is very useful. The ability to switch between D-type and T-type flip-flops is beneficial here because using T-mode allows large counters to be built without expanding the number of product terms requires. Counters can be easily built across region boundaries using either synchronous carry bits, or sum term sharing across region boundaries.

Integrating multiple small PAL™-type devices into a single H-Series is easily accomplished by putting each small device's logic in its own region. Since a region has eight or ten outputs, a typical PAL™-type device will go into one or two regions (depending on how many input are signals are needed).

Signal synchronization uses a few flip-flops and some simple logic, so a single region can easily handle several such circuits, using regional pins as inputs and putting the new, synchronized signal on one of the universal pins for use anywhere in the chip.

Design Support

Like all of Atmel's PLD products, H-Series PLDs are supported by third-party design and programming tools. Initially, the H-Series devices have support from Data I/O (ABEL™ design software and programmers), and Viewlogic Systems (design software). Other vendors are developing support, and an up-to-date of tools that support the H-Series is available from the Atmel EPLD applications department.

Summary

The H-Series is a complex PLD family designed for high throughput: fast propagation with high I/O count. It achieves fast propagation times over a wide range of applications by using a regionalized interconnect and an innovative logic cell that allows high logic utilization.