

FEATURES/BENEFITS

- QSFCT139D with 4.0ns propagation delay
- Industrial temperature -40°C to 85°C
- $I_{OL} = 48\text{mA IND}, 32\text{mA MIL}$
- TTL-compatible input and output levels
- Mil product compliant with MIL-STD 883, Class B
- CMOS power levels $< 7.5\text{mW}$ static
- Available in DIP, SOIC, QSOP, HQSOP
- JEDEC standard pinouts

DESCRIPTION

The QSFCT139T is a high-speed CMOS TTL-compatible high-speed binary decoder. The QSFCT139T has negative active outputs. The high output current I_{OL} and I_{OH} drive high-capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

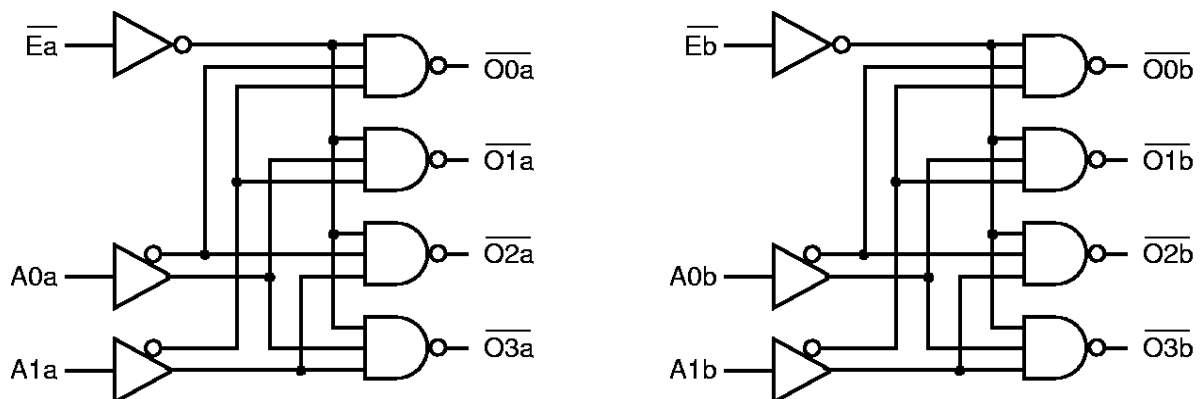
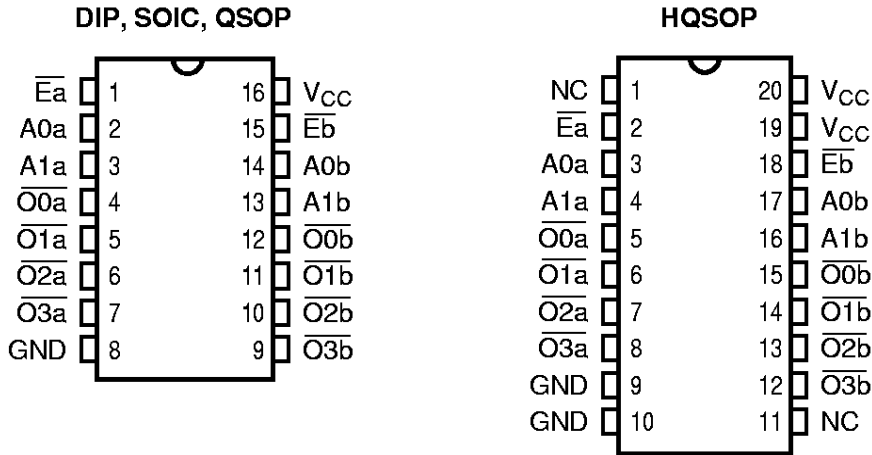


Figure 2. Pin Configurations (All Pins Top View)



Note: Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

Table 1. Pin Description

Name	I/O	Description
A _i	I	Select Inputs
\overline{O}_i	O	Decode Outputs
\overline{E}_i	I	Enable

Table 2. Function Table

Enable $\overline{E}_a, \overline{E}_b$	Select		FCT139 Output				Note
	A1	A0	\overline{O}_3	\overline{O}_2	\overline{O}_1	\overline{O}_0	
H	X	X	H	H	H	H	Disable Decode
L	L	L	H	H	H	L	A1-0 = 0
L	L	H	H	H	L	H	A1-0 = 1
L	H	L	H	L	H	H	A1-0 = 2
L	H	H	L	H	H	H	A1-0 = 3

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V_{OUT}	-0.5V to 7.0V
DC Input Voltage V_{IN}	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Capacitance⁽¹⁾

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins ⁽²⁾	SOIC	QSOP	PDIP	Unit
1-3	4	4	5	pF
7, 9-12	6	6	7	pF
4-6, 13-15	8	8	9	pF

Notes:

1. Capacitance is characterized but not tested.
2. Pin reference for 16-pin package.

Table 5. DC Electrical Characteristics Over Operating Range

Industrial $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12\text{mA (MIL)}$ $I_{OH} = -15\text{mA (IND)}$	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 32\text{mA (MIL)}$ $I_{OL} = 48\text{mA (IND)}$	— —	— —	0.50 0.50	V

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, \text{freq} = 0$ $0V \leq V_{IN} \leq 0.2V$ or $V_{CC}-0.2V \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4V, \text{freq} = 0^{(2)}$	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}, \text{Outputs Open and Enabled}$ One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4V$).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 7. Switching Characteristics Over Operating Range

Industrial $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0V \pm 5\%$ Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0V \pm 10\%$
 $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾		139A		139C		139D		Unit
			Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	Ind	1.5	5.8	1.5	5.0	1.0	4.0	ns
t_{PLH}	A_i to \overline{O}_i	Mil	1.5	7.8	1.5	7.0	—	—	
t_{PHLE}	Propagation Delay	Ind	1.5	5.9	1.5	5.0	1.0	4.0	ns
t_{PLHE}	\overline{E}_i to \overline{O}_i	Mil	1.5	8.0	1.5	7.0	—	—	

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.