

**IN74LS244**

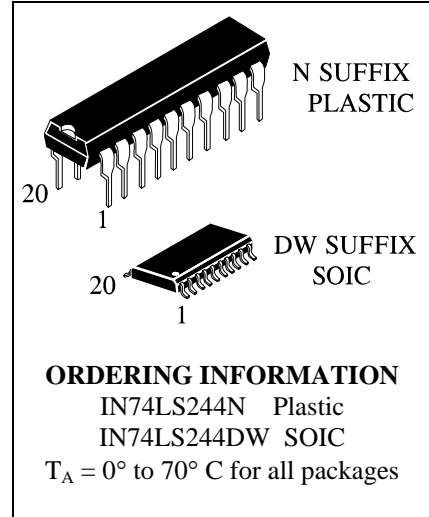
**Octal 3-State Noninverting Buffer/Line Driver/Line Receiver**

These octal buffers and line drivers and designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and busoriented receivers and transmitters.

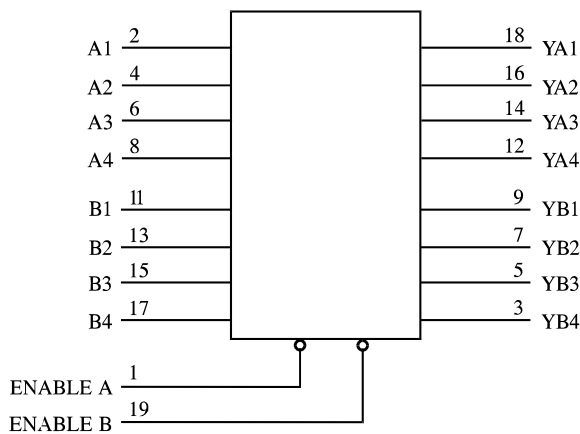
This devise features high fan-out, improved fan-in, and 400 mV noise margin.

It can be used to drive terminated lines down to 133 ohms.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins



**LOGIC DIAGRAM**



PIN 20 = V<sub>CC</sub>  
 PIN 10 = GND

**PIN ASSIGNMENT**

ENABLE A	1 ●	20	V <sub>CC</sub>
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

**FUNCTION TABLE**

Inputs		Outputs YA, YB
Enable A, Enable B	A, B	
L	L	L
L	H	H
H	X	Z

X = don't care  
 Z = high impedance

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	7.0	V
V <sub>IN</sub>	Input Voltage	7.0	V
V <sub>OUT</sub>	Output Voltage	5.5	V
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2.0		V
V <sub>IL</sub>	Low Level Input Voltage		0.8	V
I <sub>OH</sub>	High Level Output Current		-15	mA
I <sub>OL</sub>	Low Level Output Current		24	mA
T <sub>A</sub>	Ambient Temperature Range	0	+70	°C

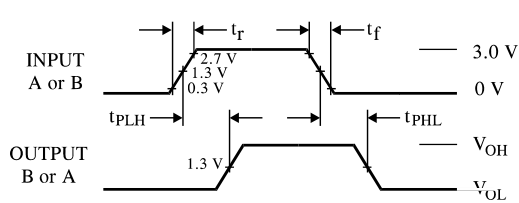
**DC ELECTRICAL CHARACTERISTICS** over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = min, I <sub>IN</sub> = -18 mA		-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = min, I <sub>OH</sub> = -1.0 mA	2.7		V
		V <sub>CC</sub> = min, I <sub>OH</sub> = -3.0 mA	2.4		
		V <sub>CC</sub> = min, I <sub>OH</sub> = -15 mA	2.0		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = min, I <sub>OL</sub> = 12 mA		0.4	V
		V <sub>CC</sub> = min, I <sub>OL</sub> = 24 mA		0.5	
V <sub>T+</sub> - V <sub>T-</sub>	Hysteresis	V <sub>CC</sub> = min	0.2		V
I <sub>OZH</sub>	Output Off Current HIGH	V <sub>CC</sub> = max, V <sub>OUT</sub> = 2.7 V		20	μA
I <sub>OZL</sub>	Output Off Current LOW	V <sub>CC</sub> = max, V <sub>OUT</sub> = 0.4 V		-20	μA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 2.7 V		20	μA
		V <sub>CC</sub> = max, V <sub>IN</sub> = 7.0 V		0.1	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 0.4 V		-0.2	mA
I <sub>O</sub>	Output Short Circuit Current	V <sub>CC</sub> = max, V <sub>O</sub> = 0 V (Note 1)	-40	-225	mA
I <sub>CC</sub>	Supply Current	Outputs High	V <sub>CC</sub> = max Outputs open	27	mA
		Outputs Low		46	
		All outputs disabled		54	

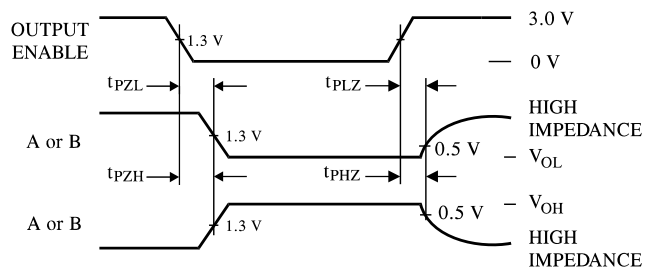
note 1: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

**AC ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $t_r = 15\text{ ns}$ ,  $t_f = 6.0\text{ ns}$ )

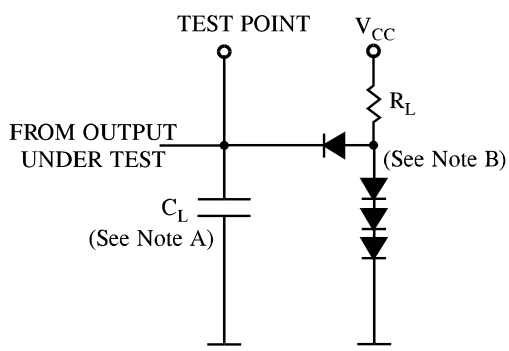
Symbol	Parameter	Test Condition	Min	Max	Unit
$t_{PLH}$	Propagation Delay, Data to Output	$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$		18	ns
$t_{PHL}$	Propagation Delay, Data to Output			18	ns
$t_{PZH}$	Output Enable Time			23	ns
$t_{PZL}$	Output Enable Time			30	ns
$t_{PHZ}$	Output Disable Time	$C_L = 5\text{ pF}$ , $R_L = 667\ \Omega$		18	ns
$t_{PLZ}$	Output Disable Time			25	ns



**Figure 1. Switching Waveforms**  
(See Figure 3)

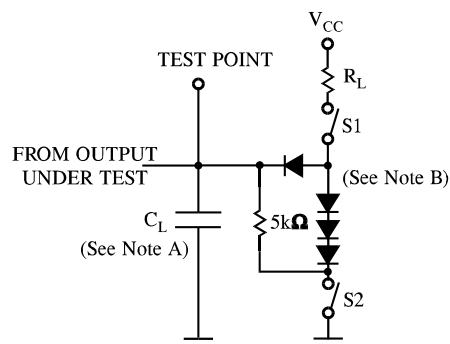


$t_{PZL}$  - S1 closed, S2 opened  
 $t_{PZH}$  - S1 opened, S2 closed  
 $t_{PLZ}$ ,  $t_{PHZ}$  - S1 and S2 closed  
**Figure 2. Switching Waveforms**  
(See Figure 4)



NOTES A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N916 or 1N3064.

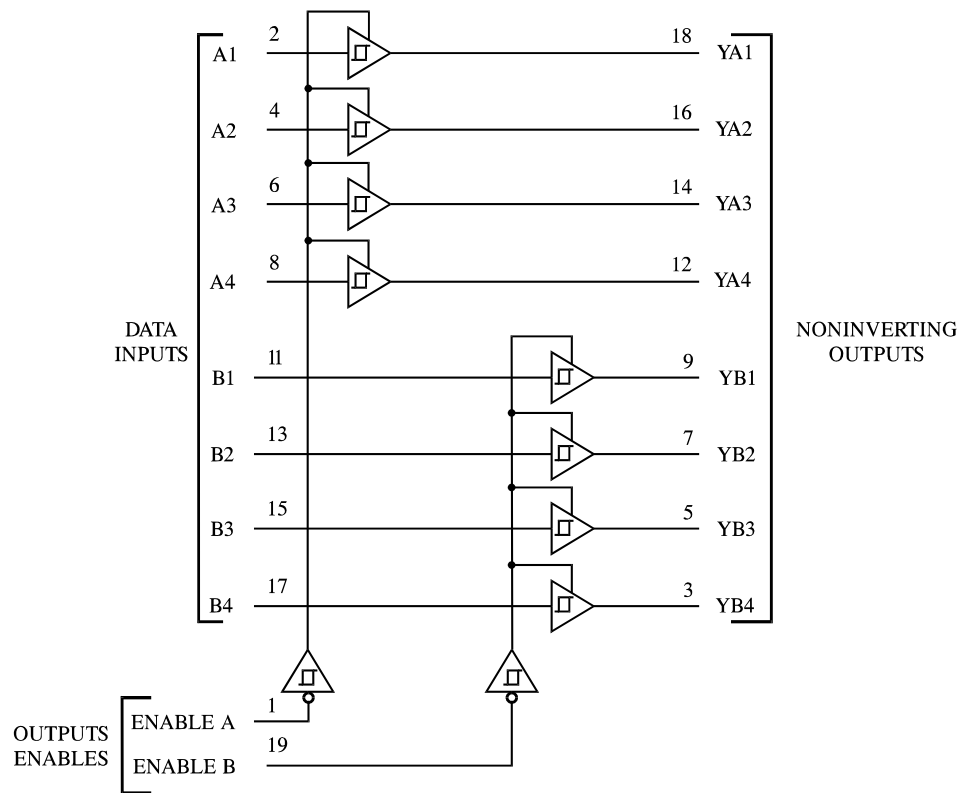
**Figure 3. Test Circuit**



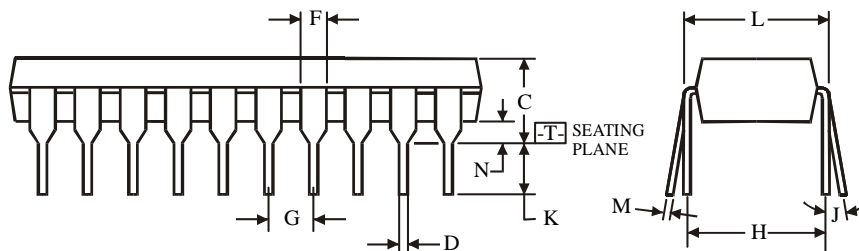
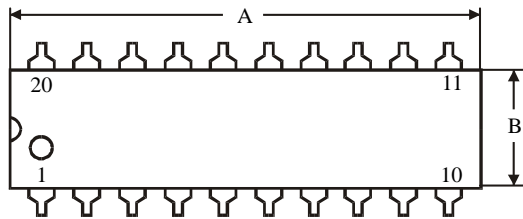
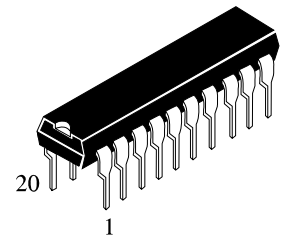
NOTES A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N916 or 1N3064.

**Figure 4. Test Circuit**

EXPANDED LOGIC DIAGRAM



**N SUFFIX PLASTIC DIP  
(MS - 001AD)**



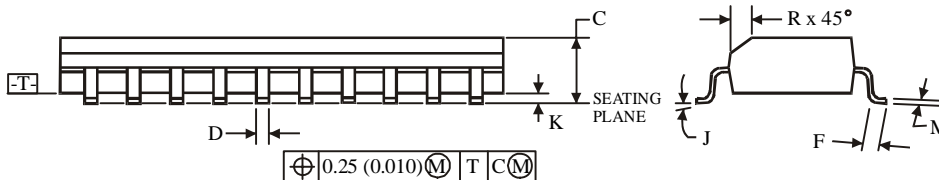
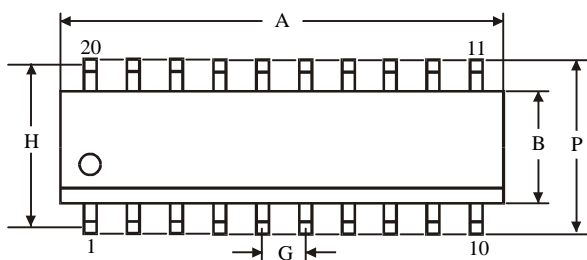
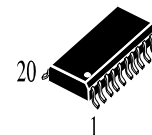
$\oplus 0.25 (0.010) \text{M} \text{T}$

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Dimension, mm		
Symbol	MIN	MAX
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC  
(MS - 013AC)**



$\oplus 0.25 (0.010) \text{M} \text{T} \text{CM}$

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Dimension, mm		
Symbol	MIN	MAX
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75