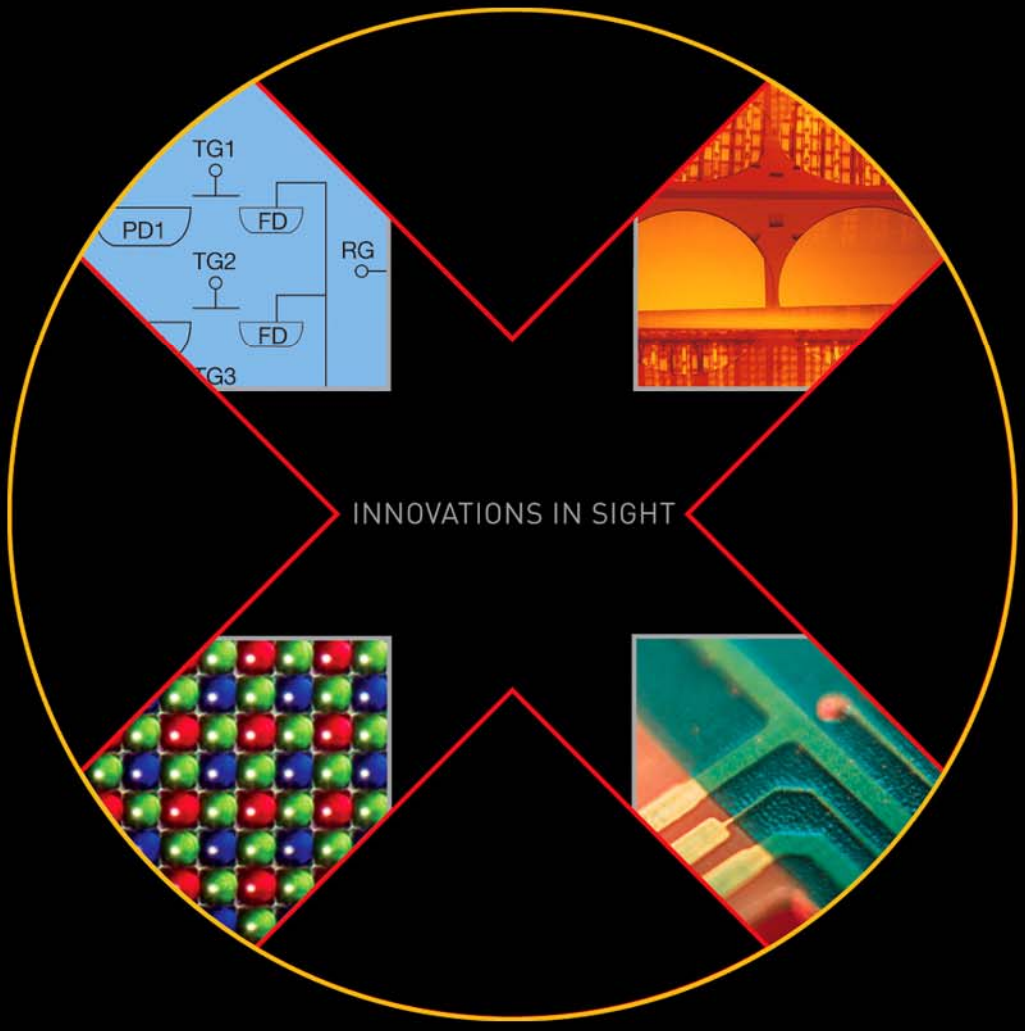
DEVICE PERFORMANCE SPECIFICATION

Revision 7.0 MTD/PS-0542

January 6, 2009



KODAK KLI-4104 IMAGE SENSOR

HIGH-RESOLUTION QUADRI-LINEAR

ARRAY 3 X 4080 CHROMA, 10UM SQUARE PIXELS

AND

ARRAY 1 X 8160 LUMA, 5UM SQUARE PIXELS

Kodak

Image Sensor Solutions

Kodak
Image Sensor Solutions

TABLE OF CONTENTS

TABLE OF FIGURES

Kodak
Image Sensor Solutions

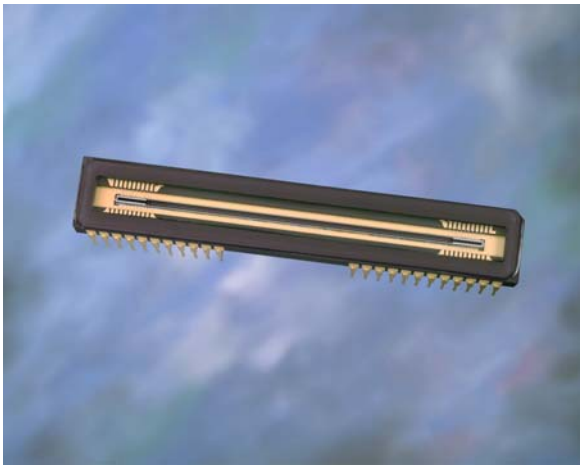
SUMMARY SPECIFICATION

KODAK KLI-4104 IMAGE SENSOR

IMAGE SENSOR QUADRI-LINEAR CCD

DESCRIPTION

The KODAK KLI-4104 Image Sensor is a multi-spectral, linear solid-state image sensor for color scanning applications where fast high resolution is required. The imager consists of three parallel linear photodiode arrays, each with 4080 active photosites for the output of R, G, and B signals. The sensor contains a fourth channel for luminance information. This array has 8160 pixels segmented to transfer out data through one of four luminance outputs. This device offers high sensitivity, high data rates, low noise and negligible lag. Individual electronic exposure control for each of the Chroma and the Luma channel is provided, allowing the KLI-4104 sensor to be used under a variety of illumination conditions.



FEATURES

- Quad-linear array (G, R, B, L)
- High resolution: Luma (monochrome) array with 5um pixels with 8160 count.
- Luma channel has 4 outputs approaching 120MHz data rate
- High resolution: color (RGB) array with 10um pixels with 4080 count.
- Each color channel has 1 output approaching 30MHz data rate
- No Image Lag
- Two-Phase Register Clocking
- On-ship Dark Reference
- Electronic exposure control

APPLICATIONS

- Document scanning
- Industrial machine vision
- High resolution inspection

Parameter	Value
Total Number of Pixels	3x4134 Chroma, 1x8292 Luma
Number of Effective Pixels	3x4128 Chroma, 1x8276 Luma
Number of Active Pixels	3x4080 Chroma, 1x8160 Luma
Pixel Size	10 µm (H) x 10 µm (V) Chroma, 5 µm (H) x 5 µm (V) Luma
Pixel Pitch	10 µm Chroma, 5 µm Luma
Inter-Array Spacing, G to R, R to B B to L	90 µm (9 lines effective) 122.5 µm (12.25 lines effective)
Chip Size	50.5 mm (H) x 1.1 mm (V)
Saturation Signal	121,000 electrons Chroma, 110,000 electrons Luma
Quantum Efficiency	62%(B), 62%(G), 80%(R), 85%(L)
Output Sensitivity	Chroma -14 µV/electron Luma -11 µV/electron
Responsivity (R/G/B/L)	17(B), 20(G), 32(R), 27(L) V/µJ/cm^2
Total Read Noise	120 electrons
Dark Current	Chroma 0.007 pA/pixel Luma 0.0008 pA/pixel
Dark Current Doubling Temperature	9°C
Dynamic Range @ 30 MHz Data Rate	60 dB (chroma) 60 dB (luma)
Photoresponse Non-uniformity	5% Peak-Peak
Charge Transfer Efficiency	0.99999/Transfer
Total Number of Pixels	3x4134 Chroma 1x8292 Luma

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0442	KLI- 4104-AAA-CB-AA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade	KLI-4104-A (Lot Number Serial Number)
4H0443	KLI- 4104-AAA-CB-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Sample	
4H0440	KLI- 4104-AAA-CP-AA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade	
4H0441	KLI- 4104-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0393	KLI- 4104-DAA-CB-AA	Color (RGB), No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade	KLI-4104-A (Lot Number Serial Number)
4H0394	KLI- 4104-DAA-CB-AE	Color (RGB), No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Sample	
4H0294	KLI- 4104-DAA-CP-AA	Color (RGB), No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade	
4H0295	KLI- 4104-DAA-CP-AE	Color (RGB), No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0349	KEK-4H0349-KLI-4104-12-30	Evaluation Board (Complete Kit)	

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Please address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE

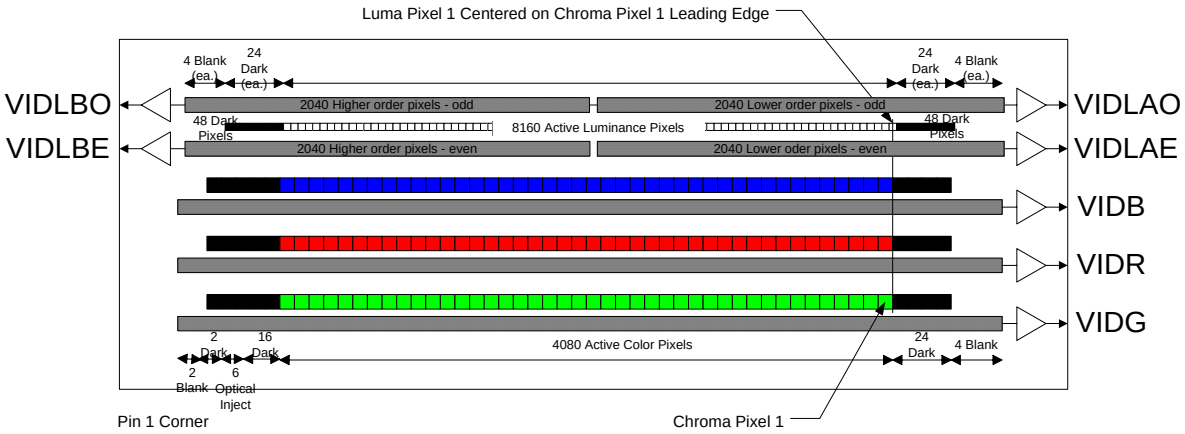


Figure 1: Block Diagram

The KLI-4104 is a high resolution, quadri-linear array designed for high-speed color scanning applications. Each device contains 3 rows of 4080 active photoelements, consisting of high performance 'pinned diodes' for improved sensitivity, lower noise and the elimination of lag. Each row is selectively covered with a red, green or blue integral filter stripe for unparalleled spectral separation. The pixel height and pitch is 10 micron and the center-to-center spacing between color channels is 90 microns, giving an effective nine line delay between adjacent channels during imaging.

Each device also contains 1 row of 8160 active photoelements. This channel has a monochrome response. The pixel height and pitch is 5 micron and the center-to-center spacing between this luminance channel and the blue color channel is 122.5 microns, giving an effective 12 ¼ line delay.

Readout of the pixel data for each color channel is accomplished through the use of a single CCD shift register allowing for a single output per channel with no multiplexing artifacts. Twenty-four light shielded photoelements are supplied at the start of each channel to act as a dark reference. After the 4080 active pixels, the trailing region contains 24 pixels dedicated for test. Only the first 16 pixels in this trailing group are configured to be dark reference pixels. The remaining pixels are used for internal testing. See the block diagram in Figure 1.

Readout of the pixel data for the luminance channel is accomplished through the use of four CCD shift registers in an odd/even and left/right readout configuration. Forty-eight light shielded photoelements are supplied at the beginning of each output channel to act as its dark reference. In other words, twenty-four dark reference pixels are on the leading edge of each luma output, none trailing. See the block diagram in Figure 1.

The devices are manufactured using NMOS, buried channel processing and utilize dual layer polysilicon and dual layer metal technologies.

The die size is 50.50 mm X 1.10 mm and is housed in a custom 46-pin, 0.400" wide, dual in line package. The die center is located between the blue and red channels and the color channels are centered in the long direction of the die. The blue channel center line is displaced +30 µm along the short dimension of the die from the die center, with pin 1 in the lower left corner.

Chroma Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the H1 and H2 gates being held in a 'high' and 'low' state respectively. Next, the TG gates are turned 'on' causing the charge to drain from the photodiode into the TG1 storage region. As TG1 is turned back 'off' charge is transferred through TG2 and into the PHI1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the H1 and H2 phases now resumes for readout of the current line of data while the next line of data is integrated.

Luma Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode and an accumulation region adjacent to the photodiode. This transfer occurs with the bias applied to TG1L. The accumulation storage region is isolated from the CCD shift registers during the integration period by the transfer gate TG2, which is held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the H1Lx and H2Lx gates being held in a 'high' and 'low' state respectively. Next, the TG2 gate is turned 'on' causing the charge to drain from the accumulation region into H1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the H1 and H2 phases now resumes for readout of the current line of data while the next line of data is integrated.

CHARGE TRANSPORT AND SENSING

In either the chroma or luma cases, readout of the signal charge is accomplished by two-phase, complementary clocking of the H1 and H2 gates, (labeled H1Cx/H2Cx or H1Lx/H2Lx). The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (7.25Vp-p min) clock swings for reduced power dissipation at 30MHz thereby, lowering clock noise and simplifying the driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the H2 clocks. Re-settable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by dVFD = dQ/CFD. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, PHIR.

PIN DESCRIPTION AND PHYSICAL ORIENTATION

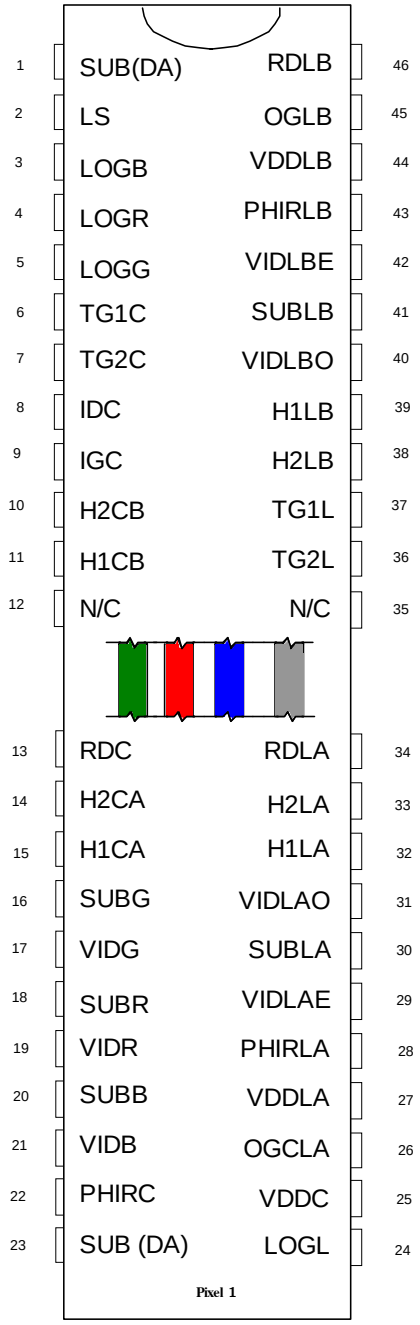


Figure 2: Pinout Diagram

Pin	Name	Description
1	SUB	Substrate / Ground
2	LS	Light Shield / Exposure Drain
3	LOGB	Exposure Control, Blue
4	LOGR	Exposure Control, Red
5	LOGG	Exposure Control, Green
6	TG1C	Transfer Gate 1 Clock, Chroma
7	TG2C	Transfer Gate 2 Clock, Chroma
8	IDC	Test Input, Input Diode, Chroma
9	IGC	Test Input, Input Gate, Chroma
10	H2CB	Phase 2 CCD Clock, Chroma
11	H1CB	Phase 1 CCD Clock, Chroma
12	N/C	No Connection (recommend these pins at ground)
13	RDC	Reset Drain Chroma
14	H2CA	Phase 2 CCD Clock, Chroma
15	H1CA	Phase 1 CCD Clock, Chroma
16	SUBG	Ground Reference, Green
17	VIDG	Output Video, Green
18	SUBR	Ground Reference, Red
19	VIDR	Output Video, Red
20	SUBB	Ground Reference, Blue
21	VIDB	Output Video, Blue
22	PHIRC	Reset Clock, Chroma
23	SUB	Substrate / Ground

Pin	Name	Description
46	RDLB	Reset Drain, Low-, High Pixels, Luma
45	OGLB	Output Gate, High Pixels, Luma
44	VDDLB	Amplifier Supply, Low- High Pixels, Luma
43	PHIRLB	Reset Clock, Luma
42	VIDLBE	Output Video, Luma High Pixels, Even Channel
41	SUBLB	Ground Reference, Low- High Pixels, Luma
40	VIDLBO	Output Video, Luma High Pixels, Odd Channel
39	H1LB	Phase 1 CCD Clock, Luma
38	H2LB	Phase 2 CCD Clock, Luma
37	TG1L	Transfer Gate 1 Bias, Luma
36	TG2L	Transfer Gate 2 Clock, Luma
35	N/C	No Connection (recommend these pins at ground)
34	RDLA	Reset Drain, Low-, High Pixels, Luma
33	H2LA	Phase 2 CCD Clock, Luma
32	H1LA	Phase 1 CCD Clock, Luma
31	VIDLA0	Output Video, Luma Low Pixels, Odd Channel
30	SUBLA	Ground Reference, Low- High Pixels, Luma
29	VISLAE	Output Video, Luma Low Pixels, Even Channel
28	PHIRLA	Reset Clock, Luma
27	VDDLA	Amplifier Supply, Low- High Pixels, Luma
26	OGCLA	Output Gate, Chroma and Low Pixels Luma
25	VDDC	Amplifier Supply, Chroma
24	LOGL	Exposure Control, Luma

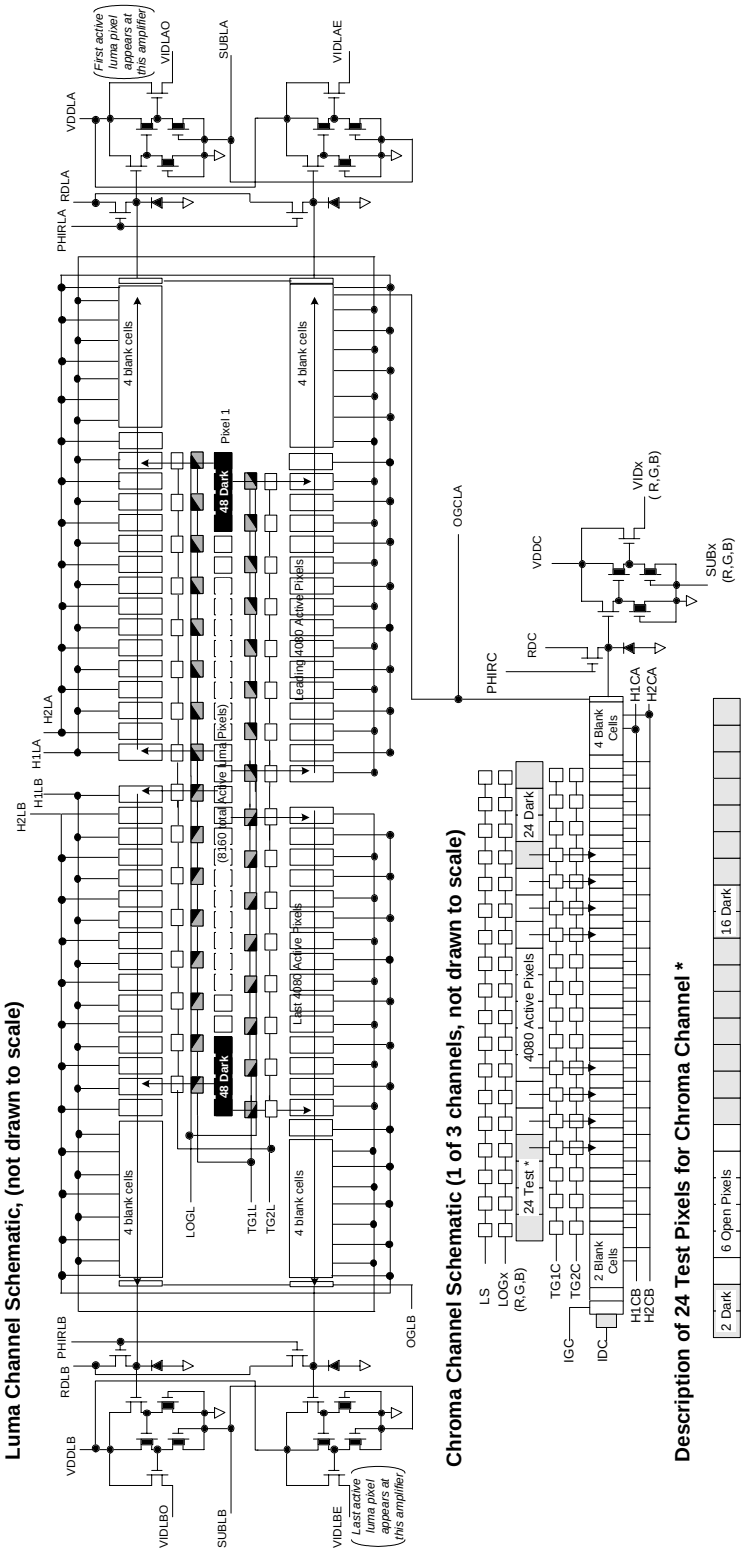


Figure 3: Device Schematic

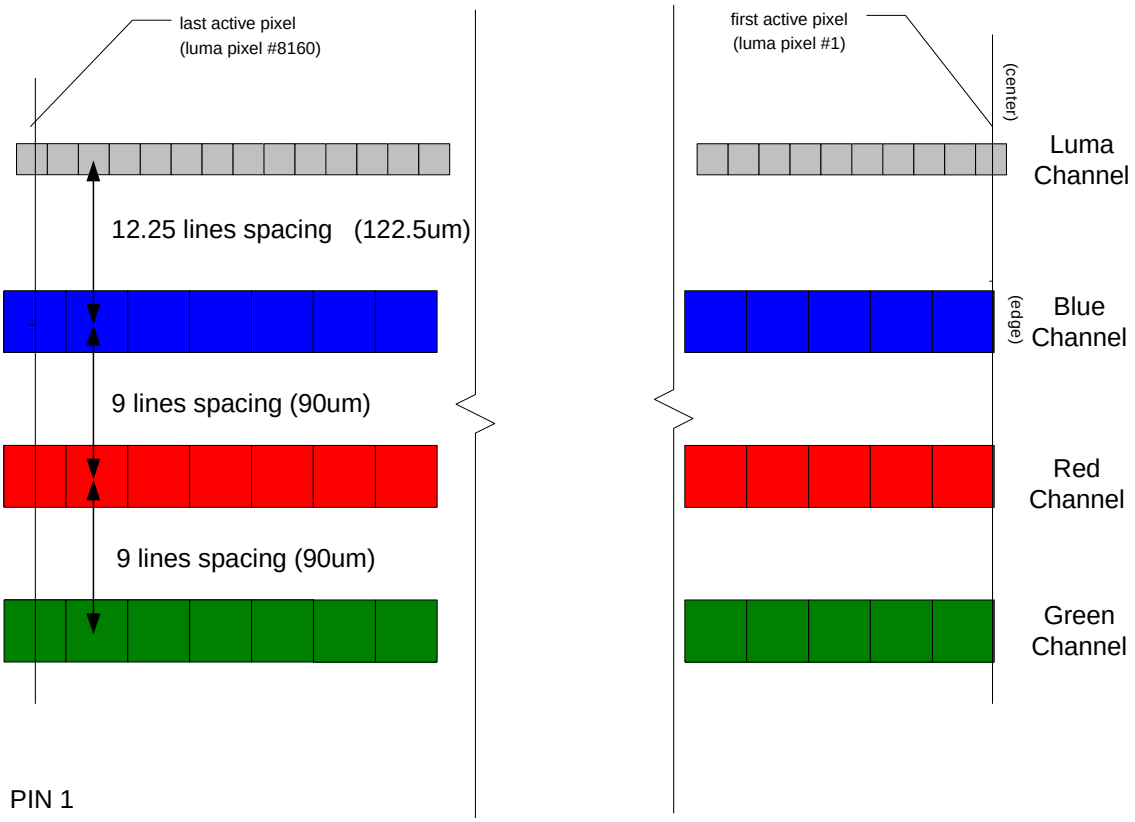


Figure 4: Channel Alignment Diagram

	Pixel Clock Cycle	VIDR	VIDG	VIDB	VIDLAO	VIDLAE	VIDLBO	VIDBLE
Leading Blanks (4)	1	Blank(1)	Blank(1)	Blank(1)	Blank(1)	Blank(1)	Blank(1)	Blank(1)
	2	Blank(2)	Blank(2)	Blank(2)	Blank(2)	Blank(2)	Blank(2)	Blank(2)
	3	Blank(3)	Blank(3)	Blank(3)	Blank(3)	Blank(3)	Blank(3)	Blank(3)
	4	Blank(4)	Blank(4)	Blank(4)	Blank(4)	Blank(4)	Blank(4)	Blank(4)
Leading DARK pixels (24)	5	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)
	6	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)
	7	Dark(3)	Dark(3)	Dark(3)	Dark(3)	Dark(3)	Dark(3)	Dark(3)
	8	Dark(4)	Dark(4)	Dark(4)	Dark(4)	Dark(4)	Dark(4)	Dark(4)
	9	Dark(5)	Dark(5)	Dark(5)	Dark(5)	Dark(5)	Dark(5)	Dark(5)
	.							
	.							
	.							
	26	Dark(22)	Dark(22)	Dark(22)	Dark(22)	Dark(22)	Dark(22)	Dark(22)
	27	Dark(23)	Dark(23)	Dark(23)	Dark(23)	Dark(23)	Dark(23)	Dark(23)
	28	Dark(24)	Dark(24)	Dark(24)	Dark(24)	Dark(24)	Dark(24)	Dark(24)
ACTIVE pixels	29	Active(1)	Active(1)	Active(1)	Active(1)	Active(2)	Active(8159)	Active(8160)
	30	Active(2)	Active(2)	Active(2)	Active(3)	Active(4)	Active(8157)	Active(8158)
	31	Active(3)	Active(3)	Active(3)	Active(5)	Active(6)	Active(8155)	Active(8156)
	32	Active(4)	Active(4)	Active(4)	Active(7)	Active(8)	Active(8153)	Active(8154)
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	2066	Active(2038)	Active(2038)	Active(2038)	Active(4075)	Active(4076)	Active(4085)	Active(4086)
	2067	Active(2039)	Active(2039)	Active(2039)	Active(4077)	Active(4078)	Active(4083)	Active(4084)
	2068	Active(2040)	Active(2040)	Active(2040)	Active(4079)	Active(4080)	Active(4081)	Active(4082)
	Clock hold during luma transfer transition to minimize noise feedthru							
	2069	Active(2041)	Active(2041)	Active(2041)	Active(1)	Active(2)	Active(8159)	Active(8160)
	2070	Active(2042)	Active(2042)	Active(2042)	Active(3)	Active(4)	Active(8157)	Active(8158)
	2080	Active(2043)	Active(2043)	Active(2043)	Active(5)	Active(6)	Active(8155)	Active(8156)
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	4105	Active(4077)	Active(4077)	Active(4077)	Active(4073)	Active(4074)	Active(4087)	Active(4088)
	4106	Active(4078)	Active(4078)	Active(4078)	Active(4075)	Active(4076)	Active(4085)	Active(4086)
	4107	Active(4079)	Active(4079)	Active(4079)	Active(4077)	Active(4078)	Active(4083)	Active(4084)
	4108	Active(4080)	Active(4080)	Active(4080)	Active(4079)	Active(4080)	Active(4081)	Active(4082)
TEST group Lagging DARK pixels (24)	4109	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)
	4110	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	4123	Dark(15)	Dark(15)	Dark(15)	Dark(15)	Dark(15)	Dark(15)	Dark(15)
	4124	Dark(16)	Dark(16)	Dark(16)	Dark(16)	Dark(16)	Dark(16)	Dark(16)
	4125	Open(1)	Open(1)	Open(1)	Dark(17)	Dark(17)	Dark(17)	Dark(17)
	4126	Open(2)	Open(2)	Open(2)	Dark(18)	Dark(18)	Dark(18)	Dark(18)
	4127	Open(3)	Open(3)	Open(3)	Dark(19)	Dark(19)	Dark(19)	Dark(19)
	4128	Open(4)	Open(4)	Open(4)	Dark(20)	Dark(20)	Dark(20)	Dark(20)
	4129	Open(5)	Open(5)	Open(5)	Dark(21)	Dark(21)	Dark(21)	Dark(21)
	4130	Open(6)	Open(6)	Open(6)	Dark(22)	Dark(22)	Dark(22)	Dark(22)
	4131	Dark(17)	Dark(17)	Dark(17)	Dark(23)	Dark(23)	Dark(23)	Dark(23)
	4132	Dark(18)	Dark(18)	Dark(18)	Dark(24)	Dark(24)	Dark(24)	Dark(24)
Blanks (2) chroma	4133	Blank(1)	Blank(1)	Blank(1)	OVERCLOCK FOR SYMMETRY			
	4134	Blank(2)	Blank(2)	Blank(2)				

NOTE: 2 lines of luma channels per every chroma channel

Figure 5: Pixel Clock Video Output Table

IMAGING PERFORMANCE

Imaging Performance Operational Conditions

Specifications given under nominally specified operating conditions for the given mode of operation @ 25°C, fCLK = 1 MHz, AR cover glass, color filters where applicable, no exposure control (line time = integration time), and an active load as shown in Figure 13, unless otherwise specified. See notes on next page for further descriptions.

Imaging Performance Specifications - Chroma Channels

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Output Voltage, Chroma	Vsat	1.5	1.7		Vp-p	1, 8, 9, 17	die[21]
Output Sensitivity, Chroma	DeltaVo/deltaNe		14		µV/e-	8, 9	design[22]
Saturation Signal Charge, Chroma	Ne, sat		121K		electrons	1, 8, 9	design[22]
Responsitivity Blue @ 460nm Green @ 550nm Red @ 650 nm	R		 17 20 32		V/microJ/cm2	2, 8, 9 ± 10 % ± 10 % ± 10 %	design[22]
Dynamic Range, Chroma	DR		60		dB	3	design[22]
Dark Signal Non-Uniformity, Chroma	DSNU		2	16	mV		die[21]
DC Gain, Amplifier, Chroma	A_{DC}		0.74				design[22]
Dark Current, Chroma @ 40°C	Idark		0.007	2	PA/pixel	14, 17	die[21]
Charge Transfer Efficiency, Chroma @ 30MHz Data Rate Charge Transfer Efficiency, Chroma @ 2MHz Data Rate	CTE	 0.999995	0.999992 0.999997			 4, 19	design[22] die[21]
Lag, Chroma @ 30MHx Data Rate Lag, Chroma @ 2MHx Data Rate	L		1 0.005		%	15	design[22] die[21]
DC Output, Offset, Chroma	Vo, dc		8.6			8, 9	design[22]
Photoresponse Non-Uniformity, Chroma Low Frequency	PRNU, Low		4	15	% p-p	5, 19	die[21]
Photoresponse Non-Uniformity, Chroma Medium Frequency	PRNU, Medium		4	15	% p-p	6, 19	die[21]
Photoresponse Non-Uniformity, Chroma High Frequency	PRNU, High		4	15	% p-p	7, 19	die[21]
Smear Smear, Chroma @ 450nm Smear, Chroma @ 500nm Smear, Chroma @ 550nm Smear, Chroma @ 600nm Smear, Chroma @ 650nm	Smear		 0.03 0.05 0.1 0.2 0.3		%		design[22]
Response Non-Linearity	RNL		3		%	16	design[22]
Darkfield Defect, Chroma Brightpoint	Dark Def			0	Allowed	11, 17	die[21]
Brightfield Defect, Chroma Dark or Bright	Bfld Def			3	Allowed	10, 12, 19	die[21]
Exposure Control Defects, Chroma Channels	Exp Def			64	Allowed	10, 13, 20 Figure 10	die[21]

Imaging Performance Specifications - Luma Channels

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Output Voltage, Luma	Vsat	1.0	1.3		Vp-p	1, 8, 9, 17	die[21]
Output Sensitivity, Luma	DeltaVo/deltaNe		11.5		µV/e-	8, 9	design[22]
Saturation Signal Charge, Luma	Ne, sat		110K		electrons	8, 9	design[22]
Responsivity, Luma (550nm)	R		6.5		V/microJ/cm2	2, 8, 9 (± 10 %)	die[21]
Dynamic Range, Luma	DR		60		dB	3	design[22]
Dark Signal Non-Uniformity, Luma	DSNU		2	16	mV	17	die[21]
DC Gain, Amplifier, Luma	A_{DC}		0.74				design[22]
Dark Current, Luma @ 40°C	Idark		0.0008	0.02	pA/pixel	14, 17	die[21]
Charge Transfer Efficiency, Luma @ 30MHz Data Rate Charge Transfer Efficiency, Luma @ 2MHz Data Rate	CTE	0.999995	0.999997 0.999997			4, 19	design[22] die[21]
Lag, Luma @ 30MHx Data Rate per Luma Channel Lag, Luma @ 2MHx Data Rate per Luma Channel	L		1 0.3		%	15	die[21]
DC Output, Offset, Luma	Vo, dc		8.6		Volts	8, 9	design[22]
Photoresponse Non-Uniformity, Luma Low Frequency	PRNU, Low		4	10	% p-p	5, 19	die[21]
Photoresponse Non-Uniformity, Luma Medium Frequency	PRNU, Medium		4	10	% p-p	6, 19	die[21]
Photoresponse Non-Uniformity, Luma High Frequency	PRNU, High		4	10	% p-p	7, 19	die[21]
Smear @ 550nm	Smear		0.12		%		design[22]
Response Non-Linearity	RNL		3.4		%	16	design[22]
Darkfield Defect, Luma Brightpoint	Dark Def			0	Allowed	11, 17	die[21]
Brightfield Defect, Luma Dark or Bright	Bfld Def			6	Allowed	17, 18, 19	die[21]
Exposure Control Defects, Luma Channels	Exp Def			128	Allowed	13, 20 Figure 10	die[21]

Notes:

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded beyond specification
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm. Color filter arrays become transparent after 710 nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF. See chart of typical responsivity later in this document.
3. As measured at 30 MHz data rate. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between PHI1 and PHI2 phases must be maintained to minimize clock noise.
4. Measured per transfer. For a chroma line: (0.99999) * 8268 = 0.92065. For a luma line: (0.99999) * 2092 = 0.97930.
5. Low frequency response is measured across the entire array with a 1000 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
6. Medium frequency response is measured across the entire array with a 50 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
7. High frequency response non-uniformity represents individual pixel defects evaluated under a flat field illumination. An individual pixel value may deviate above or below the average response for the entire array. Zero individual defects allowed per this specification.
8. Increasing the current load (nominally 4.7 mA) to improve signal bandwidth will decrease these parameters.
9. If resistive loads are used to set current, the amplifier gain will be reduced, thereby reducing the output sensitivity and net responsivity.
10. Defective pixels will be separated by at least one non-defective pixel within and across the color channels.
11. Pixels whose response is greater than the average response by the specified threshold, (16mV). See line 1 in Figure 5.
12. Pixels whose response is greater or less than the average response by the specified threshold, (±15%). See lines 2 and 3 in Figure 5.
13. Pixels whose response deviates from the average pixel response by the specified threshold, (4.5mV for chroma, 5.5mV for luma), when operating in exposure control mode with an integration time that is 50% of the line time. See lines 4 and 5 in Figure 10. If dark pattern correction is used with exposure control, the dark pattern acquisition should be completed with exposure control actuated. Dark current tends to suppress the magnitude of these defects as observed in typical applications, hence line rate changes may affect perceived defect magnitude. Measured at 1MHz data rate.
14. Dark current doubles approximately every +9°C.
15. Residual charge in the first field after transfer is used to determine lag measurement.
16. Nominal value was measured at an output of 1.5V signal level at 30MHz. Expect linearity to be better than 10% over the entire range.
17. As measured at 1MHz data rate.
18. Pixels whose response is greater or less than the average response by the specified threshold, (±10%). See lines 2 and 3 in Figure 5.
19. As measured at 1MHz data rate and with an average output level of 70% VSat.
20. As measured at 1MHz data rate and with an average output level of 100mV. With the exposure control active - the timing is adjusted so exposure time = 50% * integration time.
21. A parameter that is measured on every sensor during production testing.
22. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

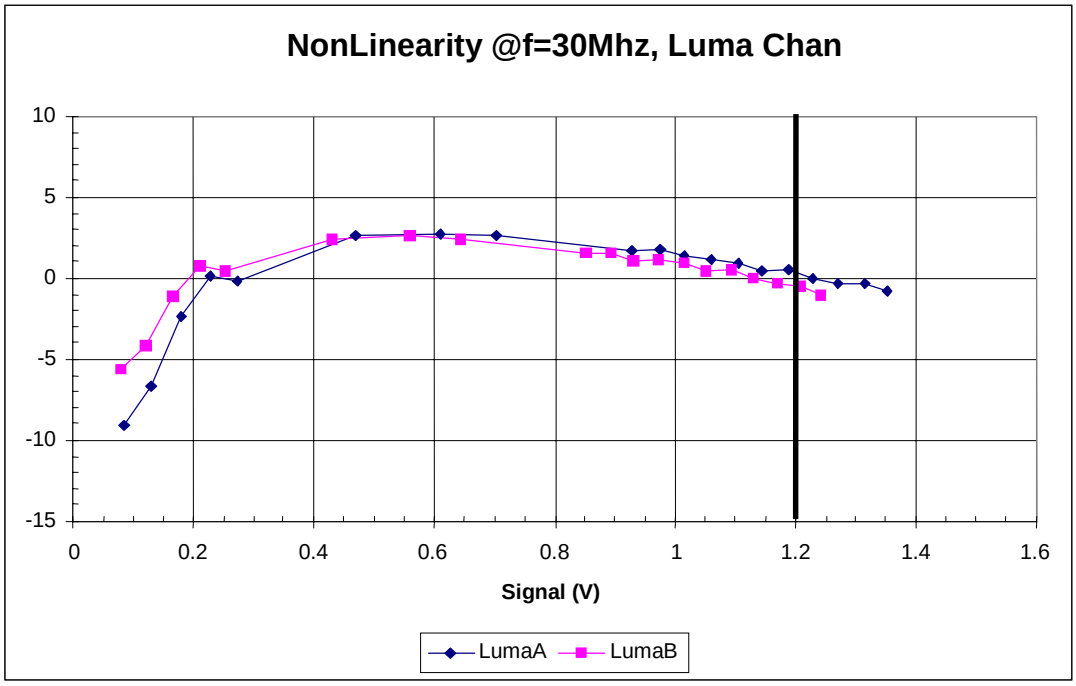


Figure 6: Typical Response Non-Linearity (%), Luma

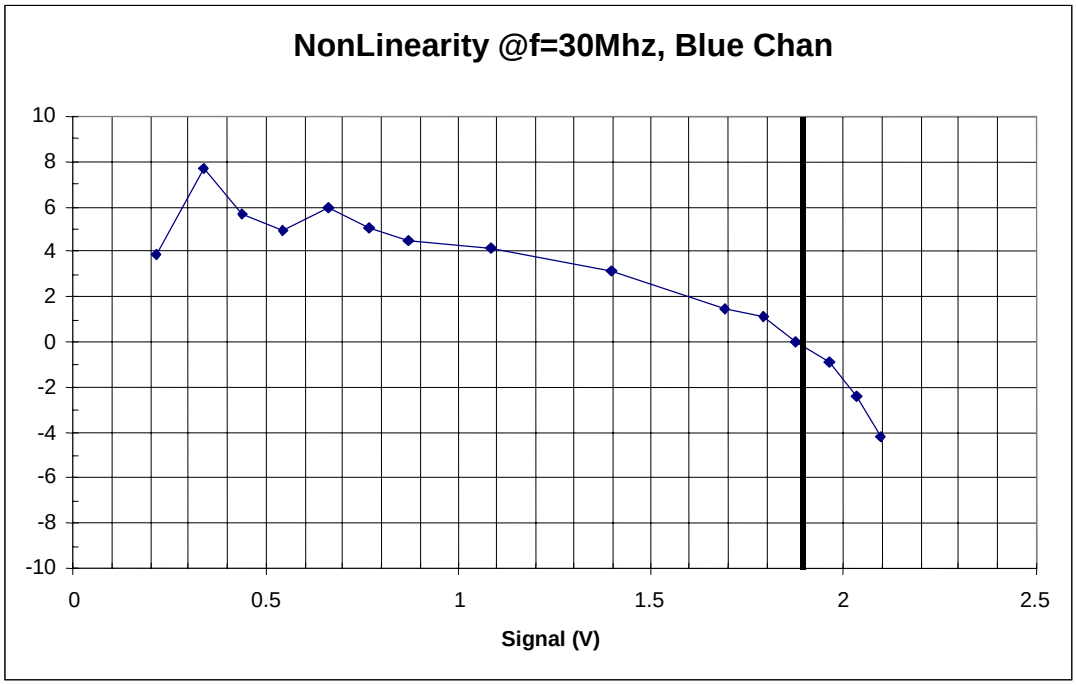


Figure 7: Typical Response Non-Linearity (%), Blue

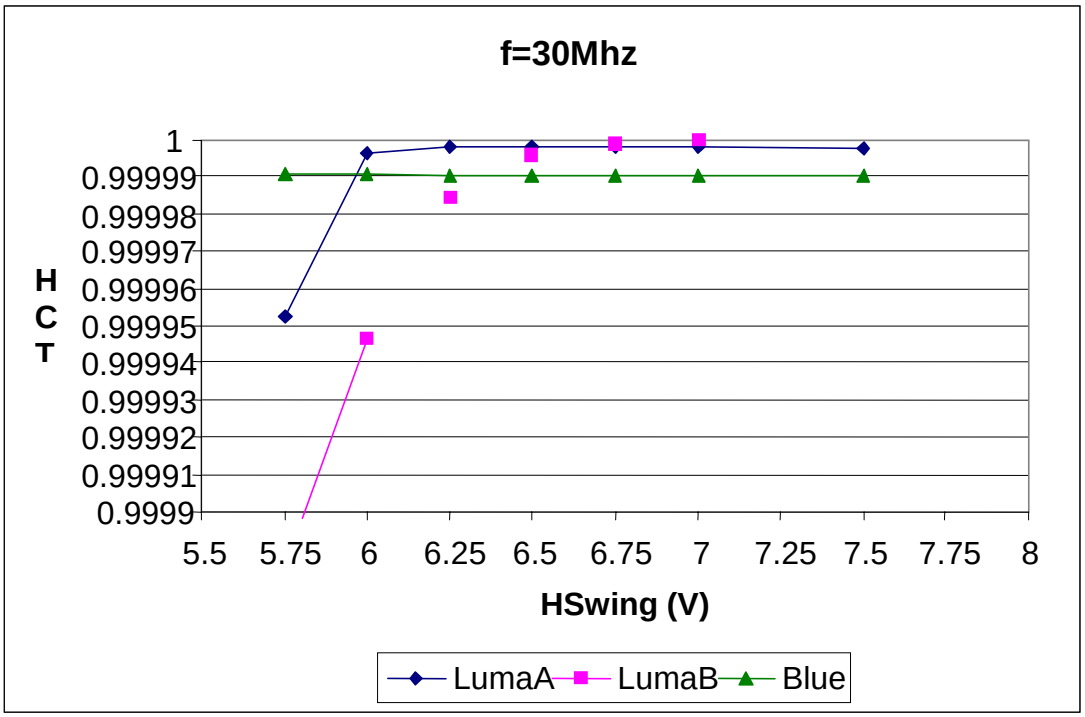


Figure 8: Typical CTE Performance vs. H Clock Levels

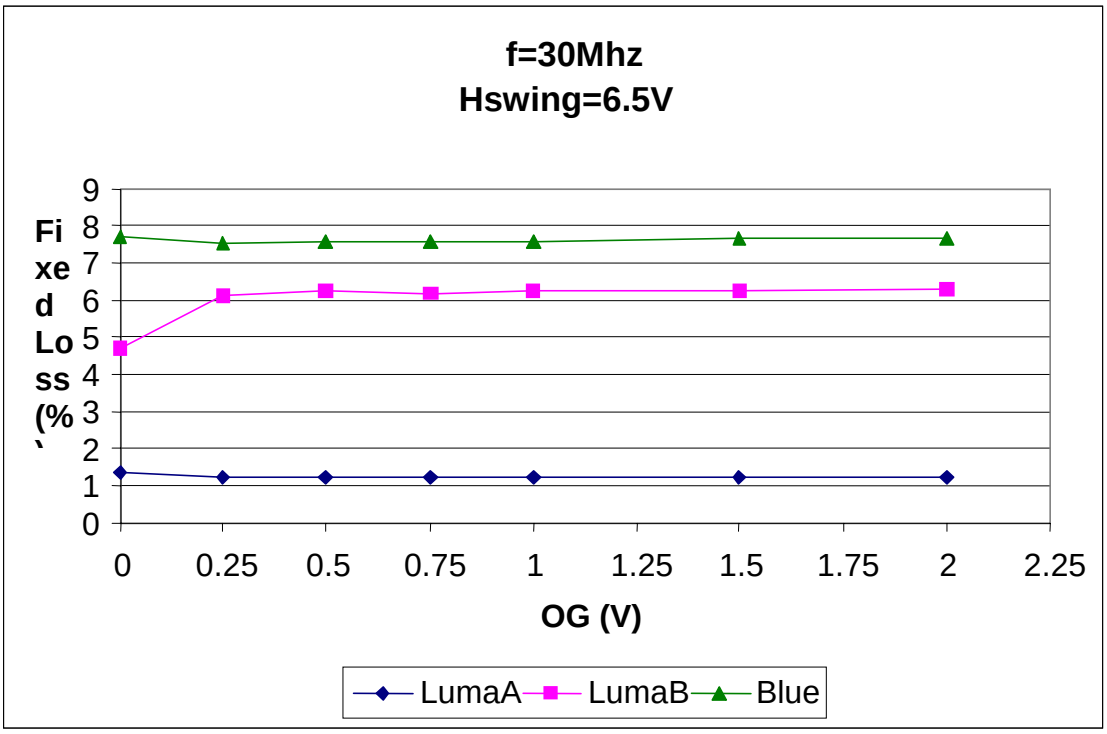


Figure 9: Typical Fixed Charge Loss vs. OG at 30 MHz.

DEFECT DEFINITIONS

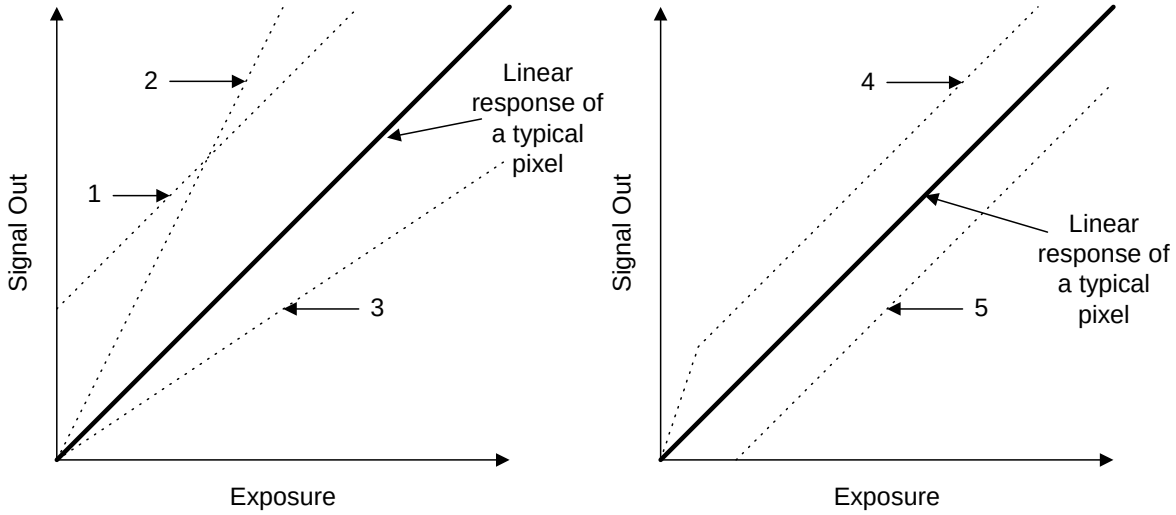


Figure 10: Defect Pixel Classification

Notes:

1 Dark Offset Error

2, 3 Brightfield Defects; bright (2), or dark (3)

4, 5 Exposure control mode defects, fast (4), or slow (5) pixels.

Color Filter Response And Description

1. A filter set has been implemented for a series of quad-linear image sensors optimized for high sensitivity color scanning. Values for the various nominal wavelength positions are shown below with corresponding tolerances for responsivity and wavelength as indicated for Color Image Sensors. See Figure 11 for clarification of parameters.
2. Independent of filter type, a degree of variation in the spectral response for the KLI-series quad-linear image sensors can be expected from the natural manufacturing tolerances of the process. This variation is due to the combined variations in filter properties (net density and filter peak wavelength position) and the device properties (sensitivity and film thickness variations).
3. Values for gauging filter performance are determined from Figure 11. The center (or peak) transmission wavelength is specified as 0, and the 50% points are given as 1 and 2, corresponding to the near and far wavelength sides of the filter pass band.
4. For the red filter, only the near wavelength value is presented. The red filter, as well as the blue and green filters, exhibits a high level of transmission beyond the 700nm (i.e., the filters become transparent). The far wavelength edge is assumed controlled by the system IR cut filter characteristics.

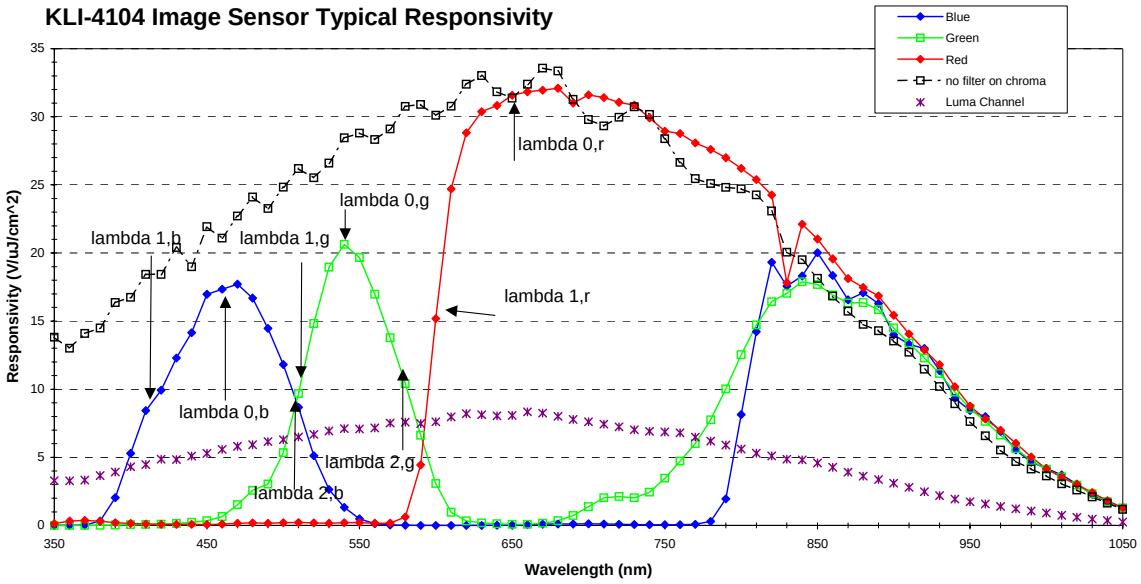


Figure 11: Typical Responsivity

Filter Variation Parameters For Color Image Sensors

Filter Channel	Parameter	Wavelength (nm) (typical)	Responsivity Tolerance 3 sigma	Wavelength Tolerance (nm) (typical)
Green	λ 0,g	540	± 12%	± 8
	λ 1,g	512	-	± 8
	λ 2,g	580	-	± 8
Blue	λ 0,b	462	± 12%	± 8
	λ 1,b	415	-	± 8
	λ 2,b	508	-	± 8
Red	λ 0,r	650	± 12%	-
	λ 1,r	602	-	± 8

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Gate Pin Voltages	VGate	0	16	V	1, 2
Pin-to-Pin Voltage	VPin-Pin		16	V	1, 3
Diode Pin Voltages	VDiode	-0.5	16	V	1, 4
Output Bias Current	IDD	-2	-8	mA	5
Output Load Capacitance	CVID,Load		10	pF	7
CCD Clocking Frequency	fclk		30	MHz	6

Notes:

1. Referenced to substrate voltage.
2. Includes pins: H1CA, H2CA, H2CA, H2CB, H1LA, H1LB, H2LA, H2LB, TG1C, TG2C, TG1L, TG2L, PHIRC, PHIRLA, PHIRLB, OGCLA, OGLB, IGC, LOGR, and LOGG.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDR, VIDG, VIDB, VIDLAO, VIDLAE, VIDLBO, VIDLBE, SUB(DA), SUBR, SUBG, SUBB, SUBLA, SUBLB, RDC, RDLA, RDLB, VDDC, VDDLA, VDDLB, LS and IDC.
5. Care must be taken not to short output pins to ground during operation as this may cause permanent damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the maximum clocking frequency. VIDR, VIDG, VIDB, VIDLAO, VIDLAE, VIDLBO, and VIDLBE load current values may need to be adjusted as well.
7. Exceeding the upper limit on output load capacitance will greatly reduce the output frequency response. Thus, direct probing of the output pins with conventional oscilloscope probes is not recommended.
8. The absolute maximum ratings indicate the limits of this device beyond which damage may occur. The Operating ratings indicate the conditions where the design should operate the device. Operating at or near these ratings do not guarantee specific performance limits. Guaranteed specifications and test conditions are contained in the Image Specifications section.

DEVICE INPUT ESD PROTECTION CIRCUIT (SCHEMATIC)

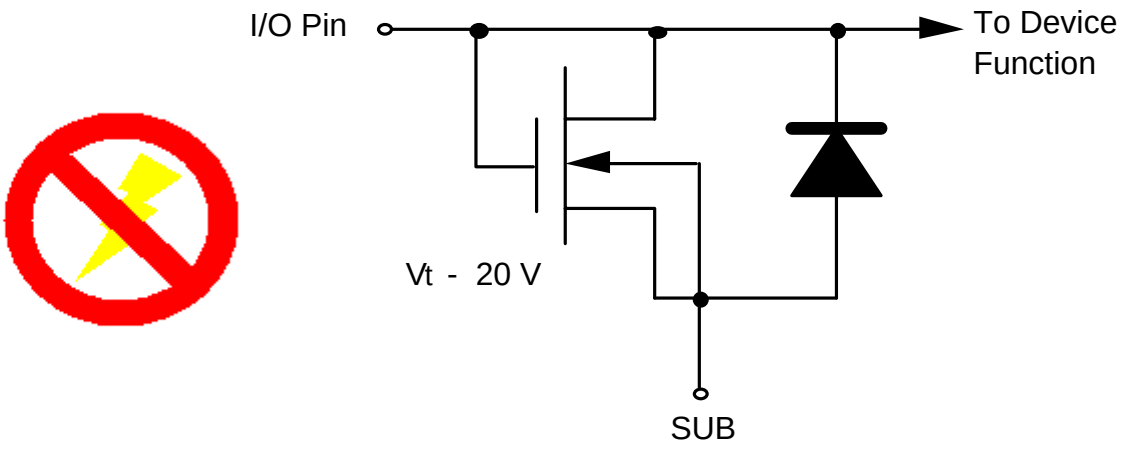


Figure 12: Device Input Protection Circuit

CAUTION: To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures!

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	V_{SUBR}, V_{SUBG} V_{SUBB} V_{SUBLA} V_{SUBLB} $V_{SUB(DA)}$		0		V	
Accumulation Phase Bias, Luma	V_{TG1L}		0	0.5	V	2, 3
Reset Drain Bias	V_{RDC} V_{RDLA}, V_{RDLAB},	10.5	11	11.5	V	2
Output Buffer Supply	V_{VDD} V_{VDD} V_{VDD} V_{VDD}	14.5	15	15.5	V	2
Output Bias Current/Channel	I_{IDDC} I_{IDDLA} I_{IDDLB}	-2	-4.7	-8	mA	1, 2
Output Gate Bias	V_{OGCLA}, V_{OGLB}	0.5	0.7	0.9	V	2, 3
Light Shield / Drain Bias	V_{LS}	12	15	15.5	V	2
Test Pin - Input Gate	V_{IGC}		0		V	2, 3
Test Pin - Input Diode	V_{IDC}	12	15	15.5	V	2

Notes:

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. Circuit below is just one solution.
2. Referenced to substrate voltage.
3. Do not exceed absolute maximum levels for diode pins voltage.

Typical Output Bias/Buffer Circuit

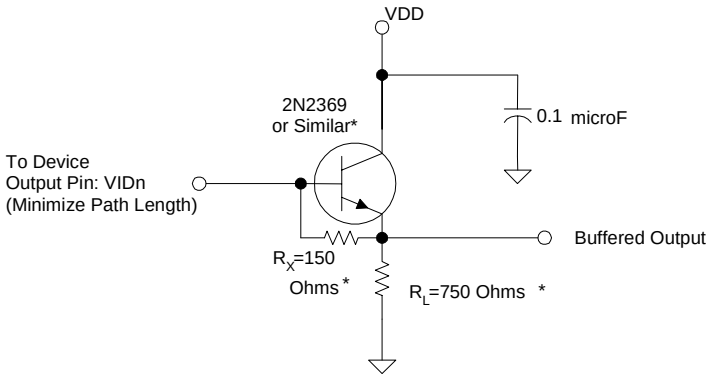


Figure 13: Typical Output Bias/Buffer Circuit

*Rx serves as the load bias for the on-chip amplifiers. Choose the values of Rx and RL to optimize for specific operating frequency. Rx should not be less than 75 Ohms.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	30MHz Operation	1MHz Operation	Maximum	Units	Notes
CCD Element Duration	1e = 1/fCLK	0.033	1		µs	3, 1e count
Line/Integration Period	1L = tint, Chroma	138.4	4156		µs	3, 4, 4156 counts
Line/Integration Period	1L = tint, Luma	68.9	2087		µs	3, 4, 2087 counts
PD-CCD Transfer Period	tpd, Chroma	0.533	16		µs	3, 5, 16e counts
PD-CCD Transfer Period	tpd, Luma	0.566	17		µs	3, 5, 17e counts
Transfer Gate 1 Clear	ttg1	0.033	1		µs	3, 1e count
Transfer Gate 2 Clear	ttg2	0.033	1		µs	3, 1e count
Charge Drain Duration as % of Line Time	tdr, Chroma			90	%	2
Charge Drain Duration as % of Line Time	tdr, Luma			90	%	2
Clamp to H2 Delay	tcd	5			ns	1
Sample to Reset Edge Delay	tsd	5			ns	1
LOG Rise Time	$t_{logrise}$	0.066	2		µs	3, 2e count
LOG Fall Time	$t_{logfall}$	0.066	2		µs	3, 2e count

Notes:

1. Recommended delays for Correlated Double Sampling (CDS) of output.
2. Maximum value stated ensures proper linearity performance. Integration times shorter than 10% of the line time increase device non-linearity.
3. Where noted as a multiple of CCD element durations, scale the appropriate times listed if the clock element time changes.
4. This value represents the shortest line period. Integration time can be shorter than a line period with the use of electronic exposure control or by extending the line period with horizontal overclocking.
5. If the application uses values less than those listed here expect degradation in lag and/or exposure control performance, where appropriate.

ELECTRICAL CHARACTERISTICS AC

CLOCK LEVEL CONDITIONS FOR OPERATION

Description	Symbol	Minimum	1MHz Operation	30MHz Operation	Maximum	Units	Notes
CCD Readout Clocks High	$VH1x_H$,$VH2x_H$	6.25	6.5	7.25	9.0	V	3, 7
CCD Readout Clocks Low	$VH1x_L$,$VH2x_L$	-0.1	0.0	0.0	0.1	V	1, 3
Transfer Clocks High - Chroma	$VTGxC_H$	6.25	6.5	7.25	9.0	V	4, 7
Transfer Clocks High- Luma	$VTG2L_H$	7.00	7.5	8.00	10.0	V	7
Transfer Clocks Low	$VTGx_L$	-0.1	0.0	0.0	0.1	V	1, 4
Reset Clock High (Normal Mode)	$VPHIRx_H$	6.25	6.5	7.25	9.0	V	5, 7
Reset Clock Low	$VPHIRx_L$	-0.1	0.0	0.0	0.1	V	1, 5
Exposure Clocks High	$VLOGx_H$	6.25	6.5	7.25	9.0	V	2, 6, 7
Exposure Clocks Low	$VLOGx_L$	-0.1	0.0	0.0	0.1	V	1, 2, 6

Notes:

1. Care should be taken to insure that low rail overshoot does not exceed -0.5 VDC. Exceeding this value may result in non-photogenerated charged being injected into the video signal.
2. Connect pin to ground potential for applications where exposure control is not required.
3. Where "x" can be "CA", "CB", "LA", or "LB".
4. Where "x" can be "1" or "2".
5. Where "x" can be "C", "LA", or "LB".
6. Where "x" can be "R", "G", or "B".
7. For high level clocks at 30MHz operation, use the values found in the "30MHz Operation" column. This value represents the recommended setting for operation. Operating ranges for the high level clocks should be held to a variation range of +/- 0.25. Clock levels below this range will result in loss of charge transfer efficiency and other performance degradations.

Clock Voltage Detail Characteristics[1]

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
TG1C High-level variation	V1HH	-	0.50	1	V	High-level coupling
TG2x High-level variation	V2HL	-	0.28	1	V	High-level coupling
TG2x Low-level variation	V2LH	-	0.46	1	V	Low-level coupling
TG1C Low-level variation	V1LL	-	0.14	1	V	Low-level coupling
H1x High-level variation	H1HH	-	0.30	1	V	
H1x High-level variation	H1HL	-	0.07	1	V	
H1 Low-level variation	H1LH	-	0.16	1	V	
H1x Low-level variation	H1LL	-	0.25	1	V	
H2x High-level variation	H2HH	-	0.40	1	V	
H2x High-level variation	H2HL	-	0.06	1	V	
H2x Low-level variation	H2LH	-	0.10	1	V	
H2x Low-level variation	H2LL	-	0.27	1	V	
H1x – H2x Cross-over	H1CR1	40	50	60	%	Rising side of H1
H1x – H2x Cross-over	H1CR2	40	50	60	%	Falling side of H1
PHIRx High-level variation	RGHH	-	0.19	1	V	
PHIRx High-level variation	RGHL	-	0.20	1	V	
PHIRx Low-level variation	RGLH	-	0.11	1	V	
PHIRx Low-level variation	RGLL	-	0.30	1	V	
TG1C Rise Time	tV1r	-	0.26	1	us	2
TG2x Rise Time	tV2r	-	0.55	1	us	2
TG1C Fall Time	tV1f	-	0.43	1	us	2
TG2x Fall Time	tV2f	-	0.31	1	us	2
H1 Rise Time	tH1r	-	9.0	10	ns	2
H2 Rise Time	tH2r	-	6.9	10	ns	2
H1 Fall Time	tH1f	-	5.8	10	ns	2
H2 Fall Time	tH2f	-	5.4	10	ns	2
PHIRx Rise Time	tRGr	-	2.0	4	ns	2
PHIRx Fall Time	tRGf	-	2.2	4	ns	2
Reset Pulse Width	tRGw	-	5.0	-	ns	

Notes:

1. H1, H2 clock frequency: 30MHz. The maximum and minimum values in this table are supplied for reference. Testing against the device performance specifications is performed using the nominal values.
2. Longer times will degrade noise performance.

CLOCK LINE CAPACITANCE

Chroma

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Phase 1 Clock Capacitance	C_{H1CA} C_{H1CB}		330		pF	1
Phase 2 Clock Capacitance	C_{H2CA} C_{H2CB}		270		pF	1
Transfer Gate 1 Capacitance	C_{TG1C}		185		pF	
Transfer Gate 2 Capacitance	C_{TG2C}		320		pF	
Exposure Gate Capacitance	C_{LOGR} C_{LOGG} C_{LOGB}		33		pF	
Reset Gate Capacitance	C_{PHIRC}		10		pF	

Luma

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Phase 1 Clock Capacitance	C_{H1LA} C_{H1LB}		400		pF	
Phase 2 Clock Capacitance	C_{H2LA} C_{H2LB}		300		pF	
Transfer Gate 2 Capacitance	C_{TG2L}		230		pF	
Exposure Gate Capacitance	C_{LOGL}		75		pF	
Reset Gate Capacitance	C_{PHIRLA} C_{PHIRLB}		6		pF	

Notes:

1. The value listed is the effective value, or equal to ½ the total load capacitance per CCD phase. Since the CCDs are driven from both ends of the sensor, the total load capacitance per horizontal drive function is approximately twice the value listed. These values were calculated from design targets. These values do not take into account the device package.

TIMING

EDGE ALIGNMENT

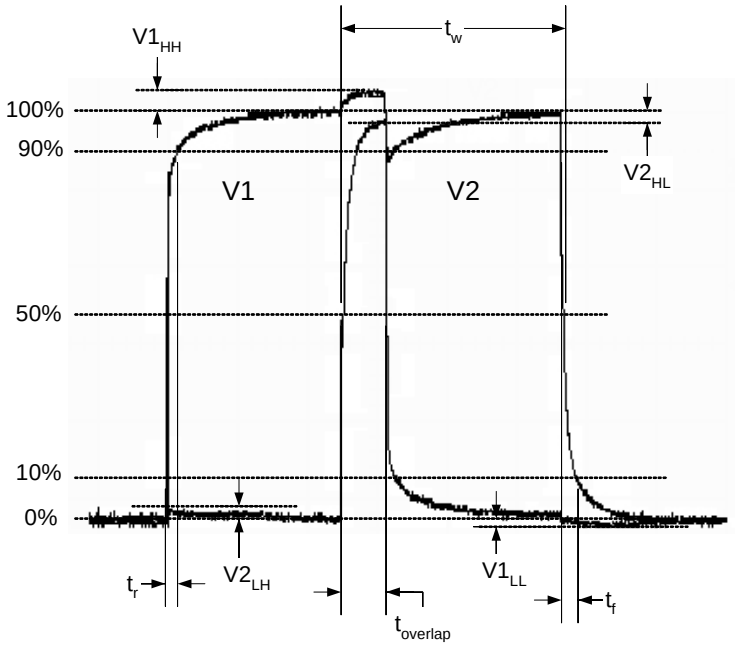


Figure 14: Transfer Timing Edge Alignment

PIXEL TIMING

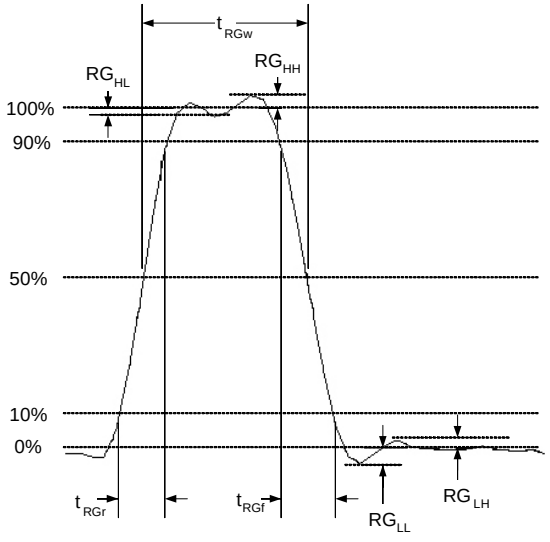


Figure 15: Pixel Timing Detail

PIXEL TIMING EDGE ALIGNMENT

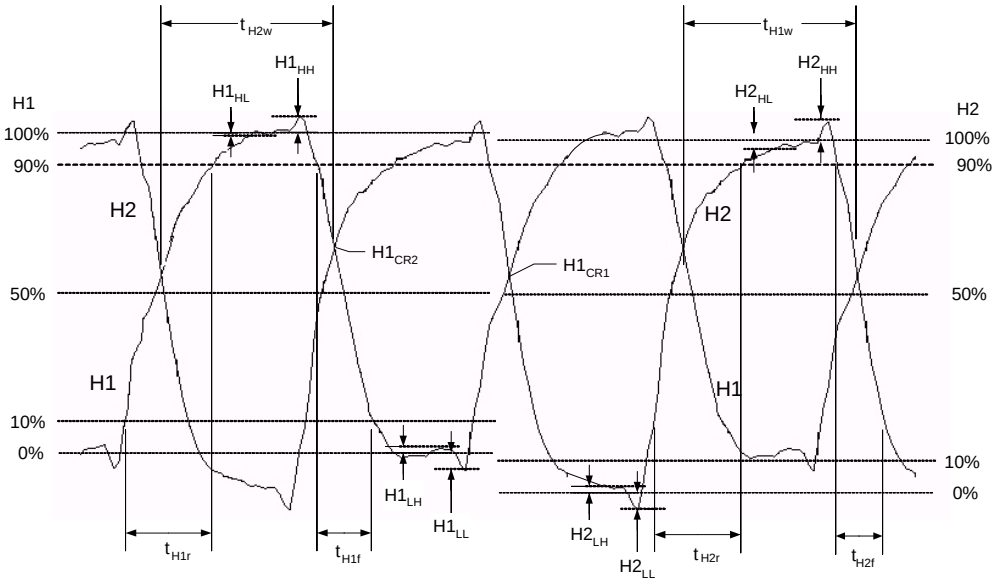
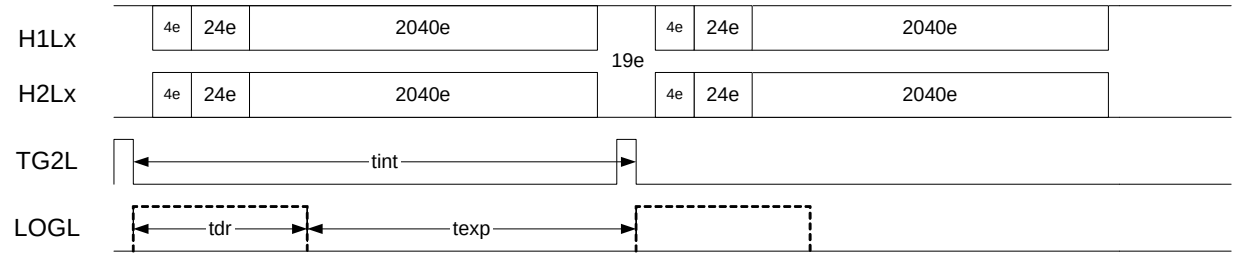


Figure 16: H1 and H2 Edge Alignment

LINE TIMING

Line Timing, Luma



Line Timing, Chroma

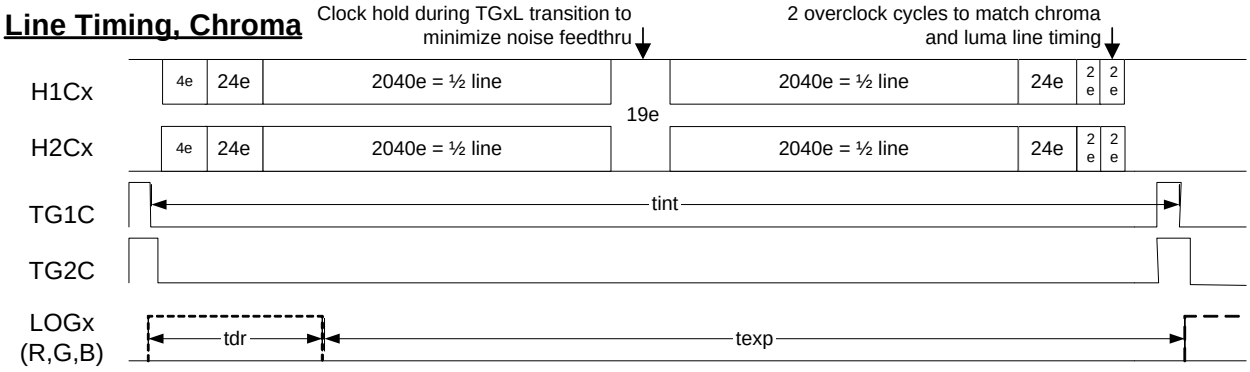
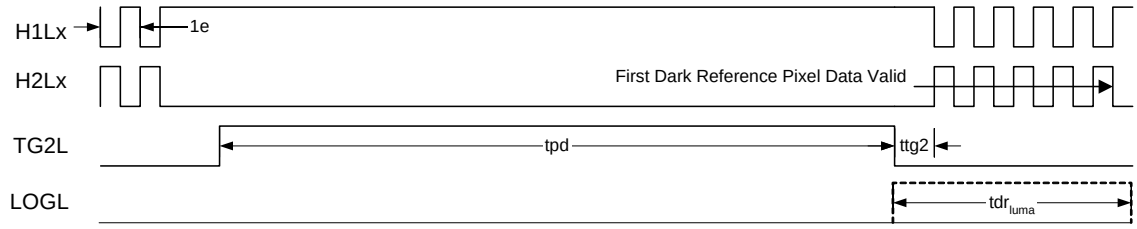


Figure 17: Line Timing Diagram

Luma Accumulation Gate-to-CCD Transfer Timing



Chroma Photodiode-to-CCD Transfer Timing

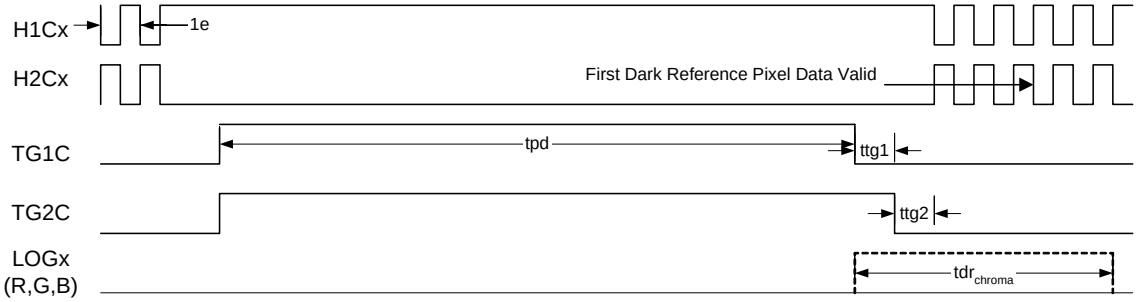
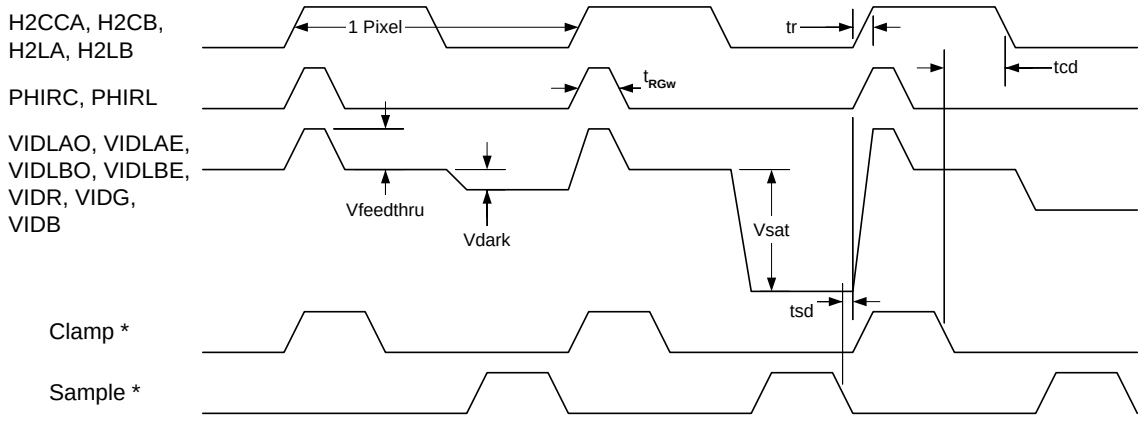


Figure 18: Transfer Timing Diagram

Output Timing



* Required for Optional Off-Chip, Analog, Correlated Double Sampling (CDS) Signal Processing

Figure 19: Output Timing Diagram

STORAGE AND HANDLING

STORAGE CONDITITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-25	80	°C	1
Humidity	RH	5	90	%	2
Operating Temperature	T_{OP}	0	70	°C	3
Guaranteed Temperature of Performance	T_{SP}	25	40	°C	4

Notes:

1. T=25°C. Excessive humidity will degrade MTTF.
2. Long-term storage toward the maximum temperature may accelerate color filter degradation.
3. Noise performance will degrade at higher temperatures.
4. See section for Imaging Performance Specifications.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices"

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370°C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.
3. For circuit board repair, or de-soldering an image sensor, do not use solder suction equipment. In any instance, care should be given to minimize and eliminate electrostatic discharge.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY

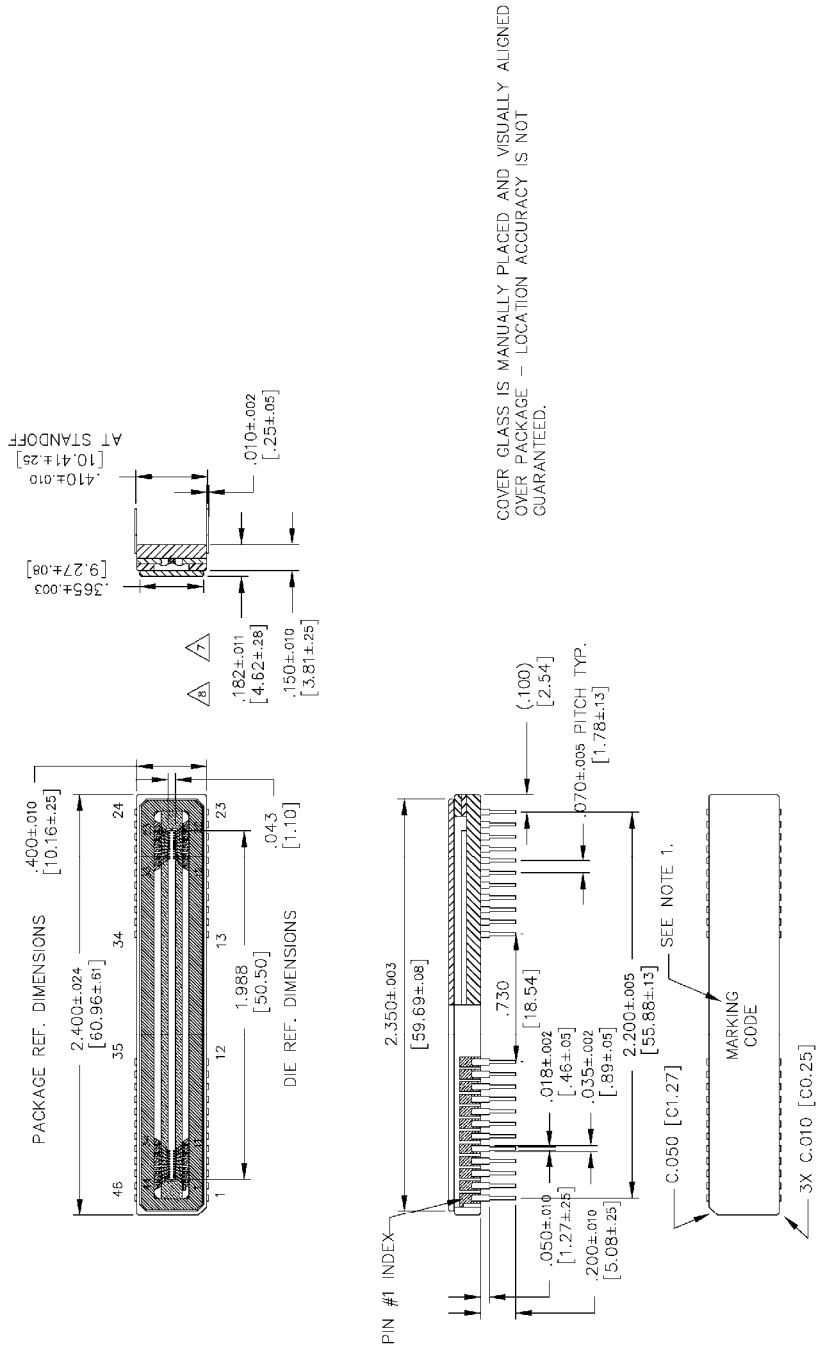


Figure 20: Completed Assembly (1 of 1)

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	• Initial formal release
2.0	• Updated specification format. Clarification of test conditions adding Notes 19-22 for Imaging Performance
3.0	• ECO 628. Updated exposure control features for the chroma only. Luma channel does not have exposure control.
4.0	• Performance values finalized per production characterization. • Correction to general part description on page 6.
5.0	• Page 3 charge capacity values updated based on characterization data . • Page 4 pinout table corrected for labeling of VIDLBE (pin 42) and VIDLBO (pin 40). Page 5 schematic clarified for readability. Page 21 timing labels changed to reflect TG1C and TG2x level variations. Levels and values did not change. Removal of package drawing. Updated exposure control features to include the luma channel. Finally, page 28, (%) description added to linearity chart to clarify units. • Sensitivity test added to Image Specification table. • Page 4 LOGL (pin 24) added to table and diagram. • Page 6 description of die center added to last paragraph. • Page 11 20mV max for chroma and 17mV max for luma added to exposure defect described in note 13. • Page 20 correction to signal names TG1C, TG2x in table. • Page 23 5ns nominal reset pulse width added to table. • Page 25 Figure 14 updated to use same name as Figure 10 for reset pulse width, tRGw
6.0	• Update of test conditions and specification format
7.0	• Page 13 - Clarified test conditions as defined by test capabilities

This page intentionally left blank.

This page intentionally left blank.