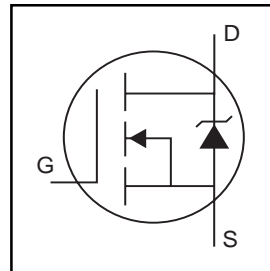


IRLR/U3103

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Ultra Low On-Resistance
- Surface Mount (IRLR3103)
- Straight Lead (IRLU3103)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

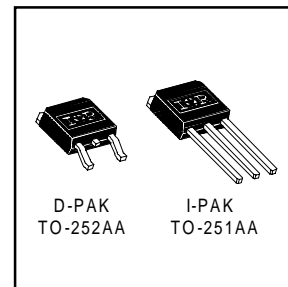


$V_{DSS} = 30V$
$R_{DS(on)} = 0.019\Omega$
$I_D = 55A\text{⑤}$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



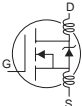
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	55⑤	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	39⑤	
I_{DM}	Pulsed Drain Current ①⑦	220	
$P_D @ T_C = 25^\circ C$	Power Dissipation	107	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②⑦	240	mJ
I_{AR}	Avalanche Current①⑦	34	A
E_{AR}	Repetitive Avalanche Energy①⑦	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

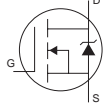
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.037	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.019	Ω	V _{GS} = 10V, I _D = 33A ④
		—	—	0.024		V _{GS} = 4.5V, I _D = 25A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	23	—	—	S	V _{DS} = 25V, I _D = 34A ⑦
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 30V, V _{GS} = 0V
		—	—	250		V _{DS} = 18V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
Q _g	Total Gate Charge	—	—	50	nC	I _D = 34A
Q _{gs}	Gate-to-Source Charge	—	—	14		V _{DS} = 24V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	28		V _{GS} = 4.5V, See Fig. 6 and 13 ④ ⑦
t _{d(on)}	Turn-On Delay Time	—	9.0	—		V _{DD} = 15V
t _r	Rise Time	—	210	—	ns	I _D = 34A
t _{d(off)}	Turn-Off Delay Time	—	20	—		R _G = 3.4Ω, V _{GS} = 4.5V
t _f	Fall Time	—	54	—		R _D = 0.43Ω, See Fig. 10 ④ ⑦
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑥
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	1600	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	640	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	320	—		f = 1.0MHz, See Fig. 5 ⑦

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	55 ⑤	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ① ⑦	—	—	220		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 28A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	81	120	ns	T _J = 25°C, I _F = 34A
Q _{rr}	Reverse Recovery Charge	—	210	310	nC	di/dt = 100A/μs ④ ⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 15V, starting T_J = 25°C, L = 300μH, R_G = 25Ω, I_{AS} = 34A. (See Figure 12)
- ③ I_{SD} ≤ 34A, di/dt ≤ 140A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%
- ⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current = 20A
- ⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact
- ⑦ Uses IRL3103 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

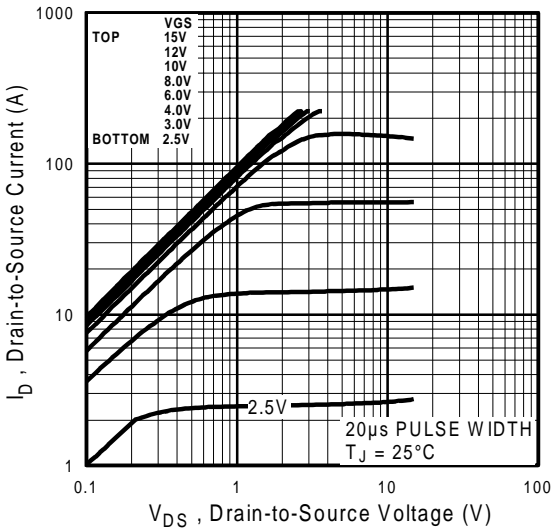


Fig 1. Typical Output Characteristics

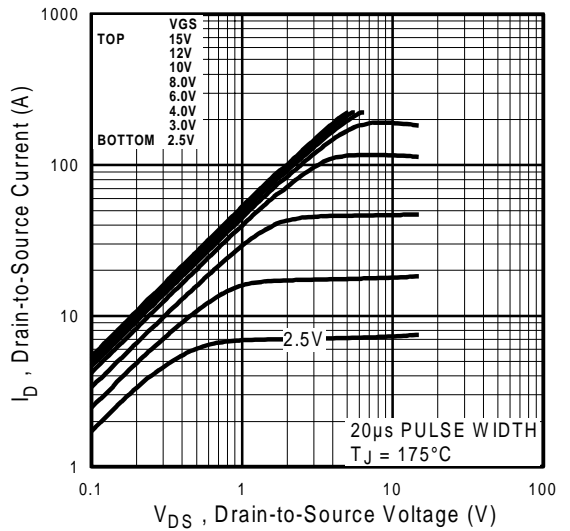


Fig 2. Typical Output Characteristics

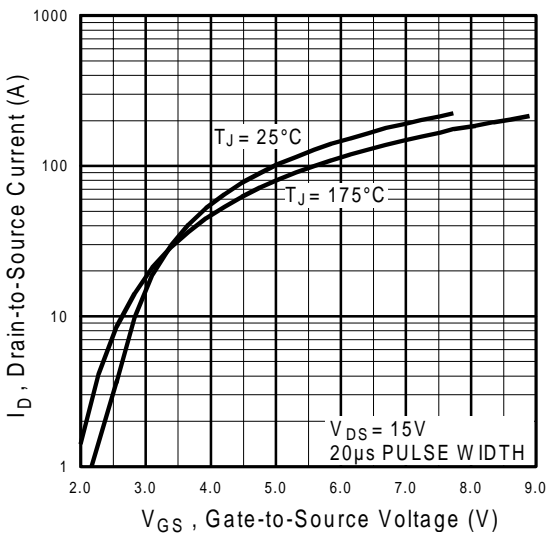


Fig 3. Typical Transfer Characteristics

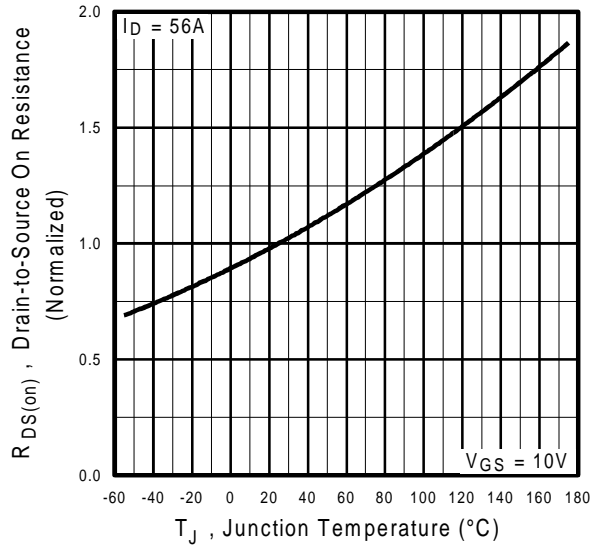


Fig 4. Normalized On-Resistance Vs. Temperature

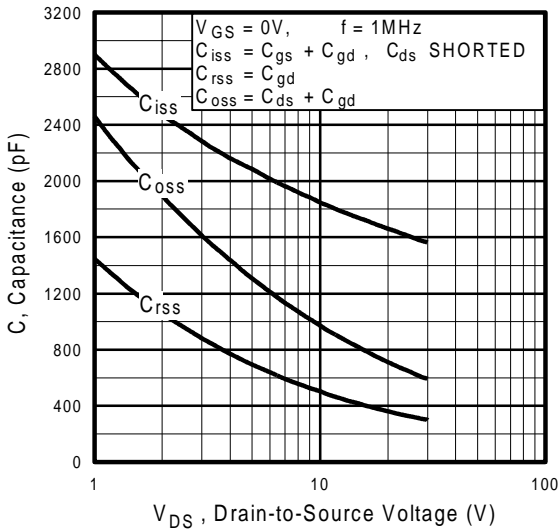


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

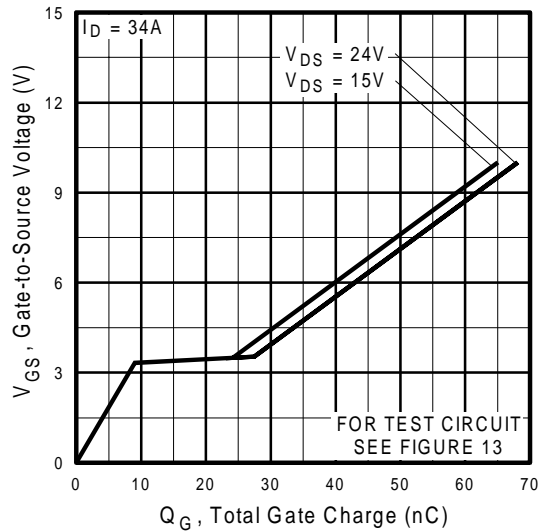


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

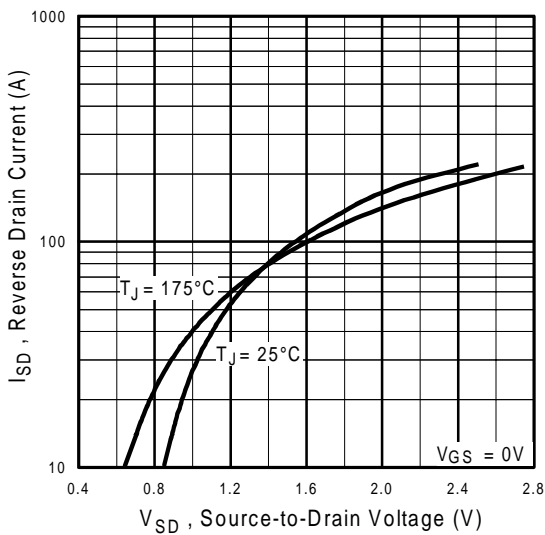


Fig 7. Typical Source-Drain Diode Forward Voltage

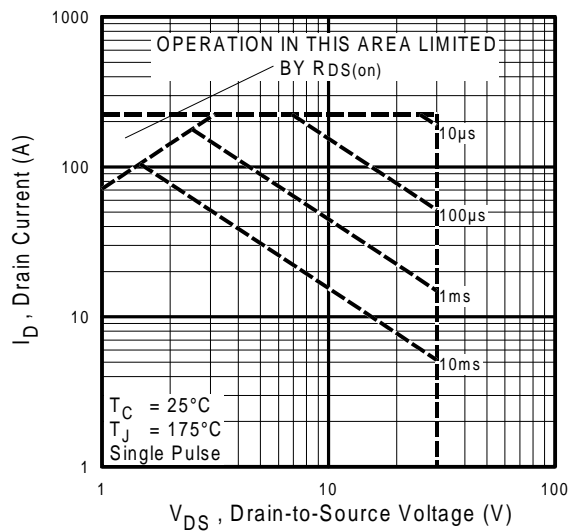


Fig 8. Maximum Safe Operating Area

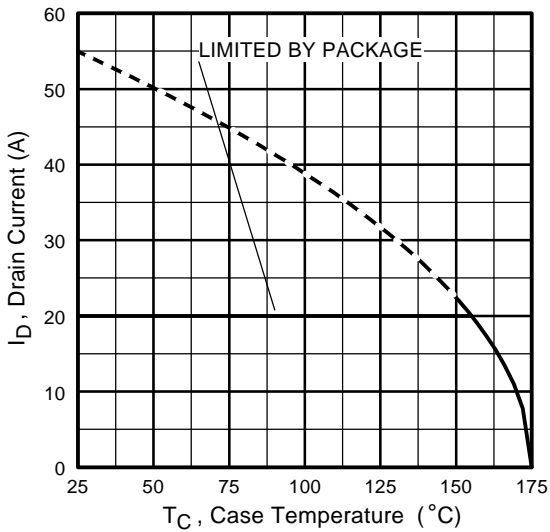


Fig 9. Maximum Drain Current Vs. Case Temperature

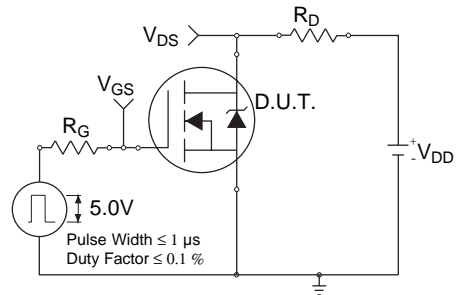


Fig 10a. Switching Time Test Circuit

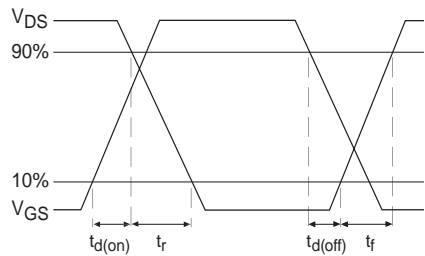


Fig 10b. Switching Time Waveforms

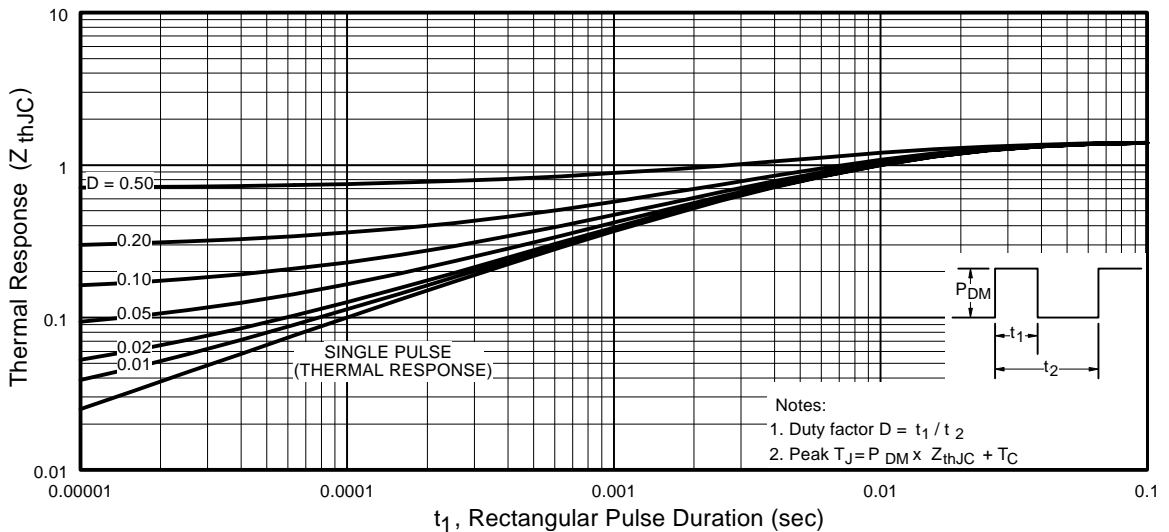


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

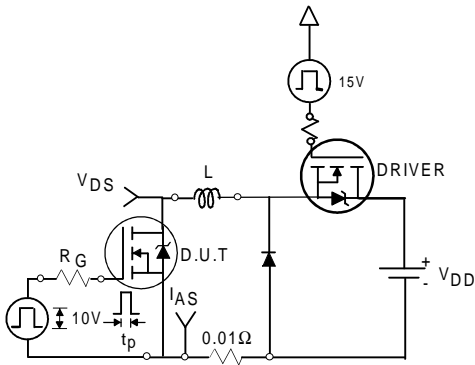


Fig 12a. Unclamped Inductive Test Circuit

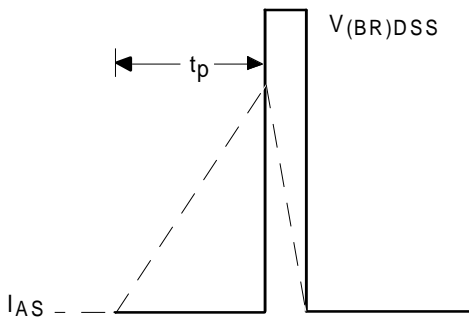


Fig 12b. Unclamped Inductive Waveforms

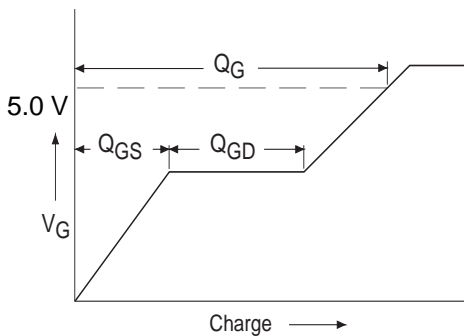


Fig 13a. Basic Gate Charge Waveform

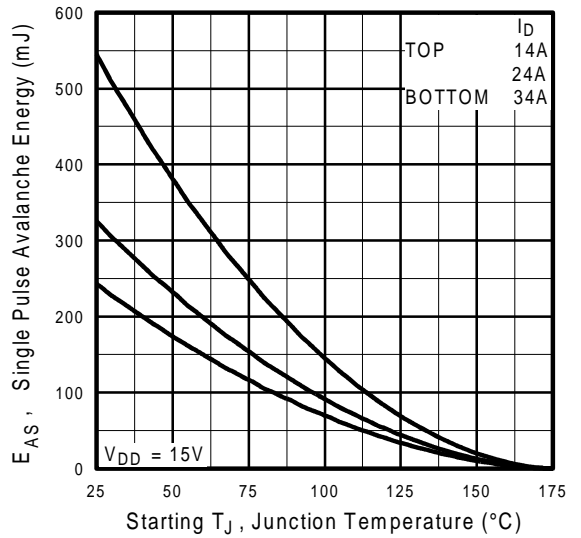


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

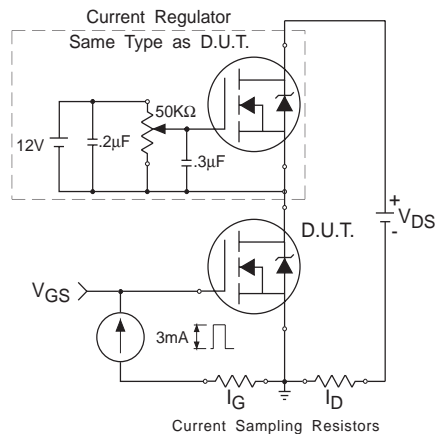
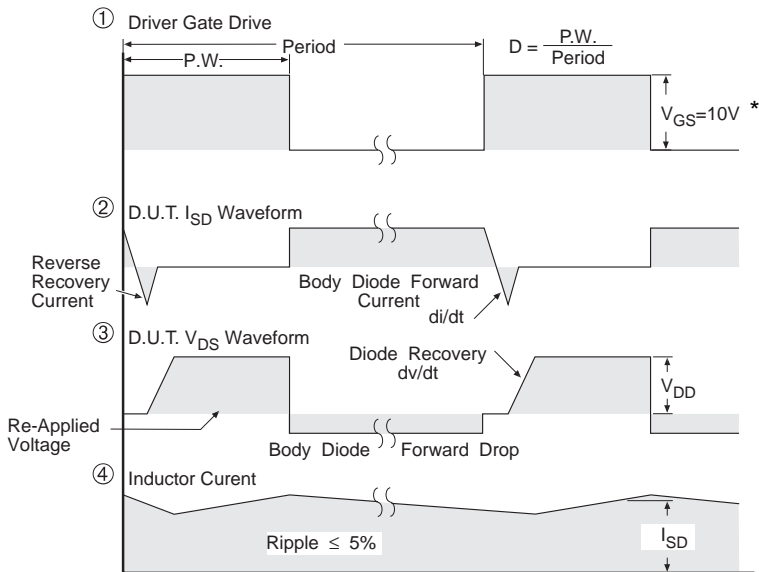
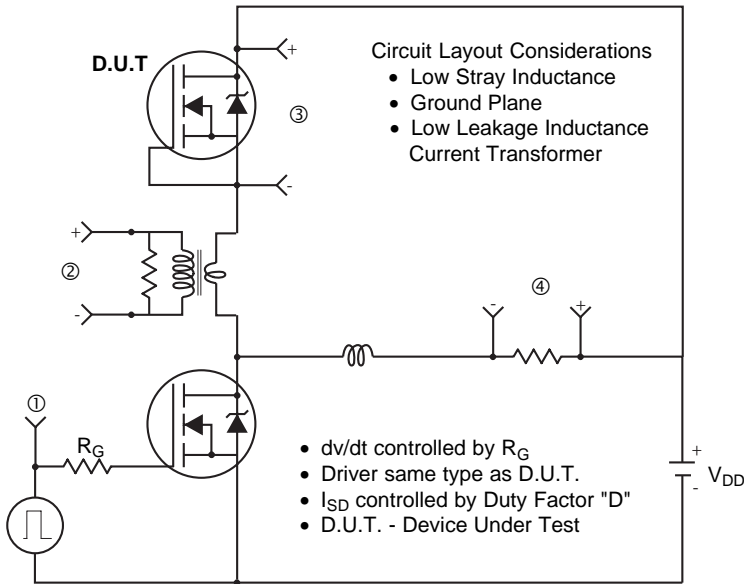


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



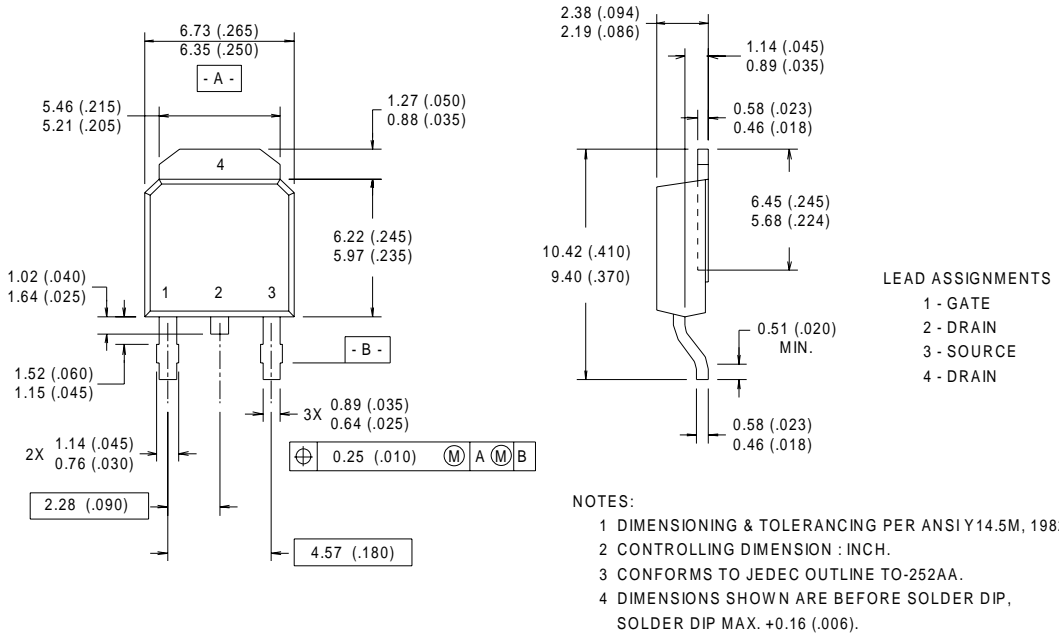
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-252AA Outline

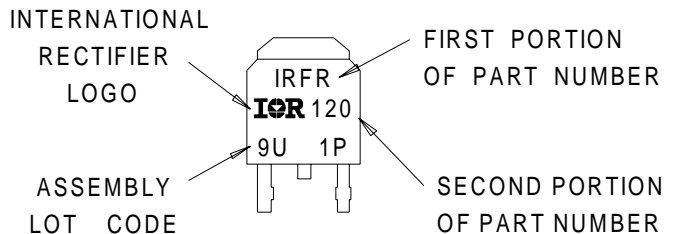
Dimensions are shown in millimeters (inches)



Part Marking Information

TO-252AA (D-PARK)

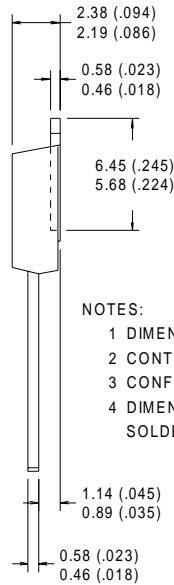
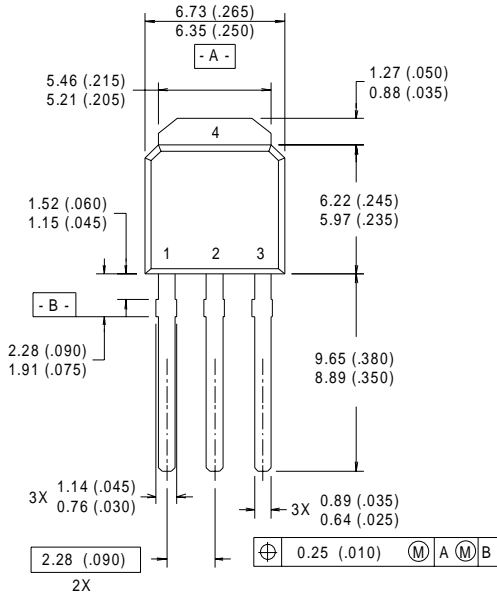
EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



Package Outline

TO-251AA Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

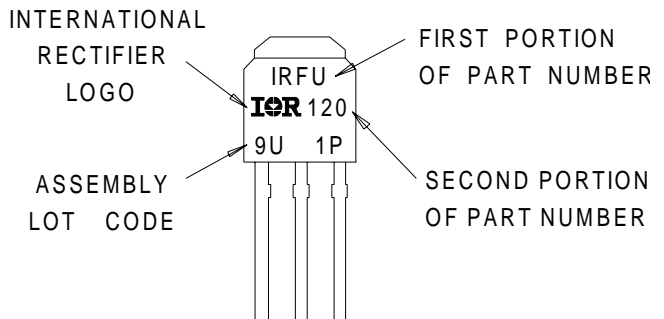
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
- 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

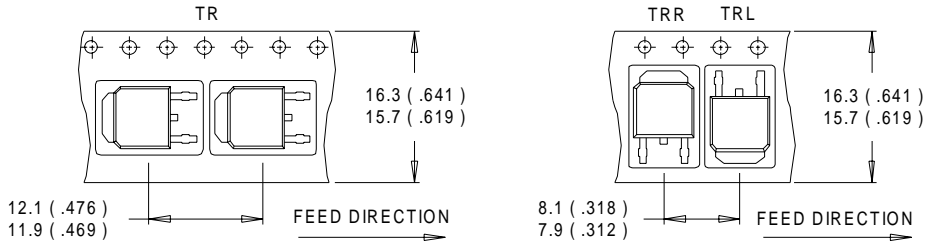
TO-251AA (I-PARK)

EXAMPLE : THIS IS AN IRFU120
 WITH ASSEMBLY
 LOT CODE 9U1P

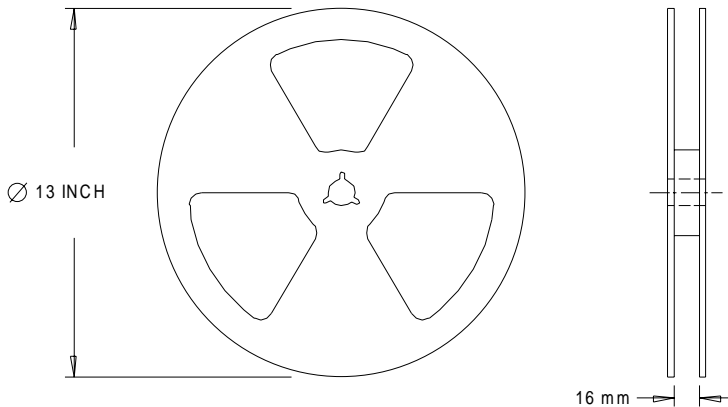


Tape & Reel Information

TO-252AA



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

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IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

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<http://www.irf.com/> Data and specifications subject to change without notice. 11/98

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>