PFS704-729EG
HiperPFS™ Family

High Power PFC Controller with Integrated High-Voltage MOSFET

Key Benefits
- Single chip solution for boost power factor correction (PFC)
  - EN61000-3-2 Class C and D compliant
- High light load efficiency at 10% and 20% load
  - >95% efficiency from 10% load to full load
  - <130 mW no-load consumption at 230 VAC with output in regulation
  - <50 mW no-load consumption at 230 VAC in remote off state
- Frequency adjusted over line voltage, and line cycle
  - Spread-spectrum across >60 kHz window to simplify EMI filtering requirements
  - Lower boost inductance
- Provides up to 1 kW peak output power
  - >1 kW peak power delivery in power limit voltage regulation mode
- High integration allows smaller form factor, higher power density designs
  - Incorporates control, gate driver, and high-voltage power MOSFET
  - Internal current sense reduces component count and system losses
- Protection features include: UV, OV, OTP, brown-in/out, cycle-by-cycle current limit, and power limiting for overload protection
- Halogen free and RoHS compliant

Applications
- PC
- Printer
- LCD TV
- Video game consoles
- High power adaptors
- High power LED lighting
- Industrial and appliance
- Generic PFC converters

Output Power Table

Product	Maximum Continuous Output Power Rating at 90 VAC	Peak Output Power Rating at 90 VAC
PFS704EG	110 W	120 W
PFS706EG	140 W	150 W
PFS708EG	190 W	205 W
PFS710EG	240 W	260 W
PFS712EG	300 W	320 W
PFS714EG	350 W	385 W
PFS716EG	388 W	425 W
Product	**Maximum Continuous Output Power Rating at 180 VAC**	**Peak Output Power Rating at 180 VAC**
PFS723EG	255 W	280 W
PFS724EG	315 W	350 W
PFS725EG	435 W	480 W
PFS726EG	540 W	600 W
PFS727EG	675 W	750 W
PFS728EG	810 W	900 W
PFS729EG	900 W	1000 W

Table 1. Output Power Table (see Notes on page 9)

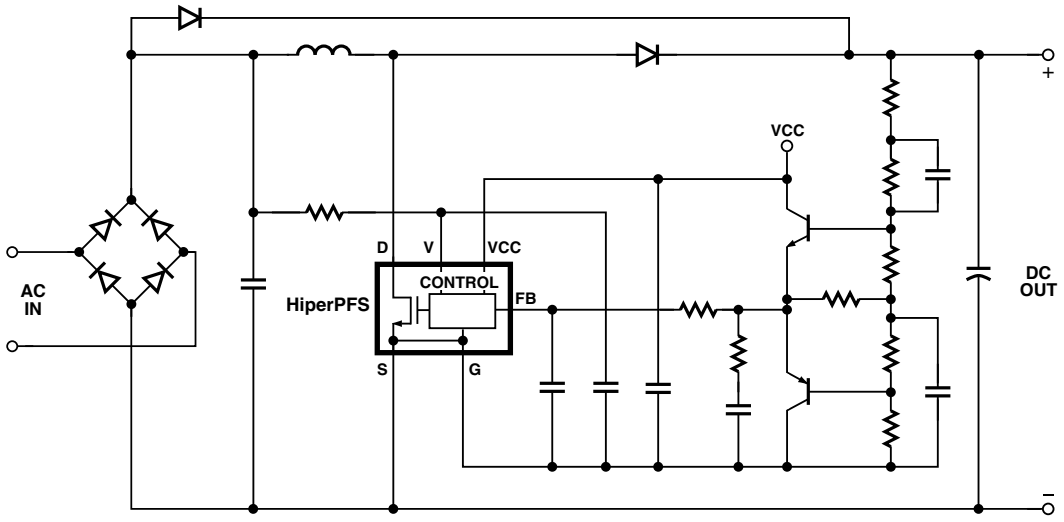


Figure 1. Typical Application Schematic.

Section List

Description

The HiperPFS device family members incorporate a continuous conduction mode (CCM) boost PFC controller, gate driver, and high voltage power MOSFET in a single, low-profile eSIP™ power package that is able to provide near unity input power factor. The HiperPFS devices eliminate the PFC converter's need for external current sense resistors, the power loss associated with those components, and leverages an innovative control technique that adjusts the switching frequency over output load, input line voltage, and even input line cycle. This control technique is designed to maximize efficiency over the entire load range of the converter, particularly at light loads. Additionally, this control technique significantly minimizes the EMI filtering requirements due to its wide-bandwidth spread spectrum effect. HiperPFS includes Power Integrations' standard set of comprehensive protection features, such as integrated soft-start, UV, OV, brown-in/out, and hysteretic thermal shutdown. HiperPFS also provides cycle-by-cycle current limit for the power MOSFET, power limiting of the output for over-load protection, and pin-to-pin short-circuit protection.

HiperPFS's innovative variable-frequency continuous conduction mode of operation (VF-CCM) minimizes switching losses by maintaining a low average switching frequency, while also varying the switching frequency in order to suppress EMI, the traditional challenge with continuous-conduction-mode solutions. Systems using HiperPFS typically reduce the total X and Y capacitance requirements of the converter, the inductance of both the boost choke and EMI noise suppression chokes, reducing overall system size and cost. Additionally, compared with designs that use discrete MOSFETs and controllers, HiperPFS devices dramatically reduce component count and board footprint while simplifying system design and enhancing reliability. The innovative variable-frequency, continuous conduction mode controller enables the HiperPFS to realize all of the benefits of continuous-conduction mode operation while leveraging low-cost, small, simple EMI filters.

Many regions mandate high power factor for many electronic products with high power requirements. These rules are combined with numerous application-specific standards that require high power supply efficiency across the entire load range, from full load to as low as 10% load. High efficiency at light load is a challenge for traditional PFC approaches in which fixed MOSFET switching frequencies cause fixed switching losses on each cycle, even at light loads. HiperPFS simplifies compliance with new and emerging energy-efficiency standards over a broad market space in applications such as PCs, LCD TVs, notebooks, appliances, pumps, motors, fans, printers, and LED lighting.

HiperPFS advanced power packaging technology and high efficiency simplifies the complexity of mounting the package and thermal management, while providing very high power capabilities in a single compact package; these devices are suitable for PFC applications from 75 W to 1 kW

Product Highlights

Protected Power Factor Correction Solution

- Incorporates high-voltage power MOSFET, controller, and gate driver
- EN61000-3-2 Class D compliance
- Integrated protection features reduce external component count
  - Accurate built-in brown-in/out protection
  - Accurate built-in undervoltage (UV) protection
  - Accurate built-in overvoltage (OV) protection
  - Hysteretic thermal shutdown (OTP)
  - Internal power limiting function for overload protection
  - Cycle-by-cycle power switch current limit
- No external current sense required
  - Provides "lossless" internal sensing via sense-FET
  - Reduces component count and system losses
  - Minimizes high current gate drive loop area
- Minimizes output overshoot and stresses during start-up
  - Integrated power limit and frequency soft start
- Improve dynamic response
  - Input line feed-forward gain adjustment for constant loop gain across entire input voltage range
- Eliminates up to 40 discrete components for higher reliability and lower cost

Intelligent Solution for High Efficiency and Low EMI

- Continuous conduction mode PFC uses novel constant volt/amp-second control engine
  - High efficiency across load using a UF boost diode
  - Low cost EMI filter
- Universal input device (PFS704 – PFS716) utilize frequency sliding technique for light load efficiency improvements
  - >95% efficiency from 10% load to full load at low line input voltage
  - >96% efficiency from 10% load to full load at high line input voltage
- High line input device (PFS723 – PFS729) maintain higher average switching frequency to minimize boost inductance and core size
  - >94% efficiency from 10% load to full load
- Variable switching frequency to simplify EMI filter design
  - Varies over line input voltage to maximize efficiency and minimize EMI filter requirements
  - Varies with input line cycle voltage by >60 kHz to maximize spread spectrum effect

Advanced Package for High Power Applications

- Up to 1 kW peak output power capability in a highly compact package
- Simple clip mounting to heat sink
  - Can be directly connected to heat sink with insulation pad
  - Provides thermal impedance equivalent to a TO-220
- Staggered pin arrangement for simple routing of board traces and high voltage creepage requirements
- Single package solution for PFC converter reduces assembly costs and layout size

Pin Functional Description

VOLTAGE MONITOR (V) Pin:
The V pin is tied to the rectified AC rail through an external resistor. Internal circuitry detects the peak of the input line voltage which resembles a full-wave rectified waveform. The rectified high-voltage bus is connected directly to the V pin voltage through a large resistor (4 MΩ for PFS70x and PFS71x; 9 MΩ for PFS72x) to minimize power dissipation and standby power consumption. A small ceramic capacitor (0.1 μF for PFS70x and PFS71x; 0.047 μF for PFS72x) is required from the VOLTAGE MONITOR pin to SIGNAL GROUND pin to bypass any switching noise present on the rectified bus. This pin also features both brown-in and brown-out protection.

FEEDBACK (FB) Pin:
The FEEDBACK pin is high input-impedance reference terminal that connects to a feedback resistor network. This pin will also feature fast overvoltage and undervoltage detection circuitry that will disengage the internal power MOSFET in the event of a system fault. A 10 nF capacitor is required between the FEEDBACK to SIGNAL GROUND pins; this capacitor must be placed very close to the device on the PCB to bypass any switching noise. This pin is also used for loop compensation.

BIAS POWER (VCC) Pin:
This is a 10-12 VDC bias supply used to power the IC. The bias voltage must be externally clamped to prevent the VCC pin from exceeding 13.4 VDC.

SIGNAL GROUND (G) Pin:
Discrete components used in the feedback circuit, including loop compensation, decoupling capacitors for the supply (VCC) and line-sense (V) must be referenced to the G pin. **The SIGNAL GROUND pin must not be tied to the SOURCE pin**.

SOURCE (S) Pin:
This pin is the source connection of the power switch.

DRAIN (D) Pin:
This is the tab and drain connection of the internal power switch.

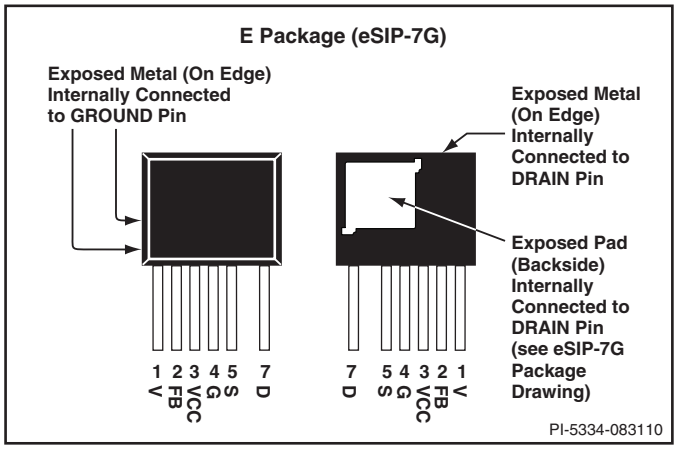


Figure 2. Pin Configuration.

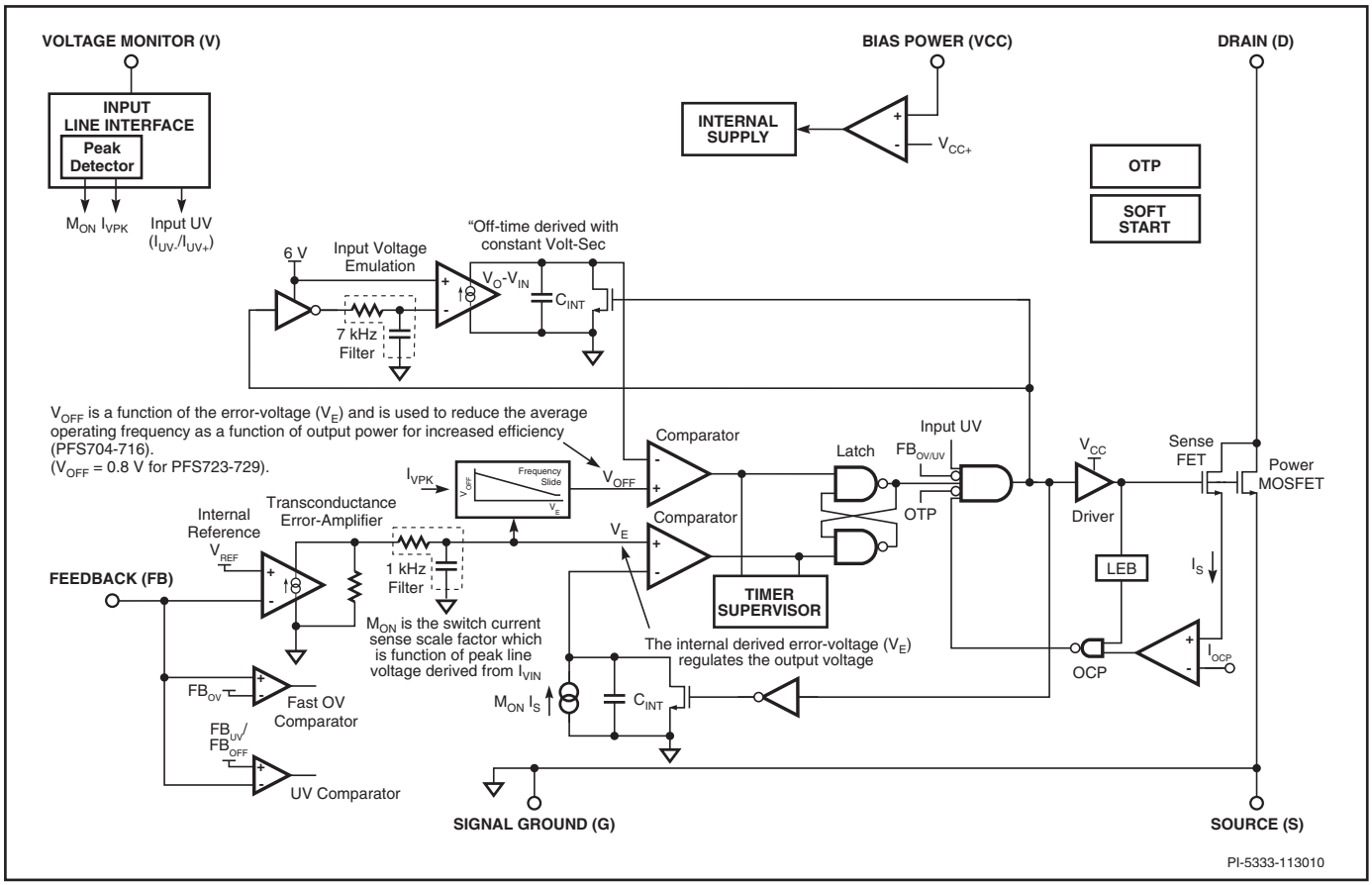


Figure 3. Functional Block Diagram.

Functional Description

The HiperPFS is a variable switching frequency boost PFC solution. More specifically, it employs a constant amp-second on-time and constant volt-second off-time control algorithm. This algorithm is used to regulate the output voltage and shape the input current to comply with regulatory harmonic current limits (high power factor). Integrating the switch current and controlling it to have a constant amp-sec product over the on-time of the switch allows the average input current to follow the input voltage. Integrating the difference between the output and input voltage maintains a constant volt-second balance dictated by the electro-magnetic properties of the boost inductor and thus regulates the output voltage and power.

More specifically, the control technique sets constant volt-seconds for the off-time (t_{OFF}). The off-time is controlled such that:

$$(V_O - V_{IN}) \times t_{OFF} = K_1 \qquad (1)$$

Since the volt-seconds during the on-time must equal the volt-seconds during the off-time, to maintain flux equilibrium in the PFC choke, the on-time (t_{ON}) is controlled such that:

$$V_{IN} \times t_{ON} = K_1 \qquad (2)$$

The controller also sets a constant value of charge during each on-cycle of the power MOSFET. The charge per cycle is varied gradually over many switching cycles in response to load changes so it can be regarded as substantially constant for a half line cycle. With this constant charge (or amp-second) control, the following relationship is therefore also true:

$$I_{IN} \times t_{ON} = K_2 \qquad (3)$$

Substituting t_{ON} from (2) into (3) gives:

$$I_{IN} = V_{IN} \times \frac{K_2}{K_1} \qquad (4)$$

The relationship of (4) demonstrates that by controlling a constant amp-second on-time and constant volt-second off-time, the input current I_{IN} is proportional to the input voltage V_{IN}, therefore providing the fundamental requirement of power factor correction.

This control produces a continuous mode power switch current waveform that varies both in frequency and peak current value across a line half-cycle to produce an input current proportional to the input voltage.

Control Engine

The controller features a low bandwidth error-amplifier which connects its non-inverting terminal to an internal voltage reference of 6 V. The inverting terminal of the error-amplifier is available on the external FEEDBACK pin which connects to the external feedback resistor divider, transient load speed-up and compensation networks to regulate the output voltage.

The internal sense-FET switch current is integrated and scaled by the input voltage peak detector current sense gain (M_{ON}) and compared with the error-amplifier signal (V_E) to determine the cycle on-time. Internally the difference between the input and output voltage is derived and the resultant is scaled, integrated, and compared to a voltage reference (V_{OFF}) to determine the cycle off-time. Careful selection of the internal scaling factors produce input current waveforms with very low distortion and high power factor.

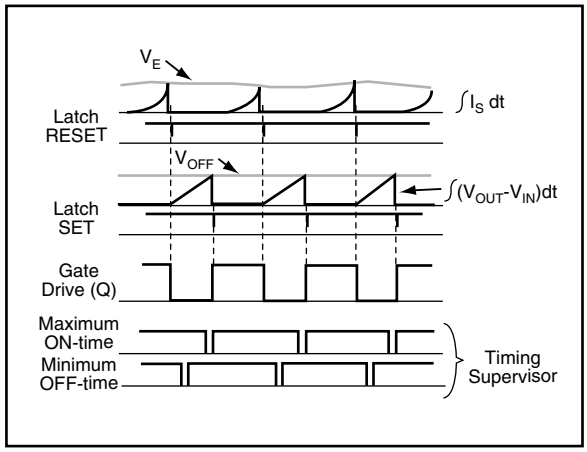


Figure 4. Idealized Converter Waveforms.

The input voltage is internally synthesized using the switch duty cycle and a 7 kHz low pass filter. This synthesized input voltage representation is subtracted from a fixed reference voltage (6 V) to derive a current source proportional to (V_O-V_{IN}). Please refer to Figure 3.

Line Feed-Forward Scaling Factor (M_{ON})

The VOLTAGE MONITOR (V) pin current is used internally to derive the peak of the input line voltage which is used to scale the gain of the current sense signal through the M_{ON} variable. This contribution is required to reduce the dynamic range of the control feedback signal as well maintain a constant loop gain over the operating input line range. This line-sense feed-forward gain adjustment is proportional to the square of the peak rectified AC line voltage and is adjusted as a function of V pin current. The line-sense feed-forward gain is also important in providing a switch power limit over the input line range. Besides modifying brown- in/out thresholds, the V pin resistor also affects power limit of the device

This characteristic is optimized to maintain a relatively constant internal error-voltage level at full load from an input line of 100 to 230 VAC input (PFS704-716).

Beyond the specified peak power rating of the device, the internal power limit feature will regulate the output voltage below the set regulation threshold as a function of output overload beyond the peak power rating. Figure 5 illustrates the typical regulation characteristic as function of load.

Soft-Start with Pin-to-Pin Short-Circuit Protection

Since the FEEDBACK pin is the interface for output voltage regulation (resistor voltage divider to output voltage) as well as loop compensation (series RC), the typical application circuit of the HiperPFS requires an external transistor network to overcome the inherently slow feedback loop response. Specifically, an

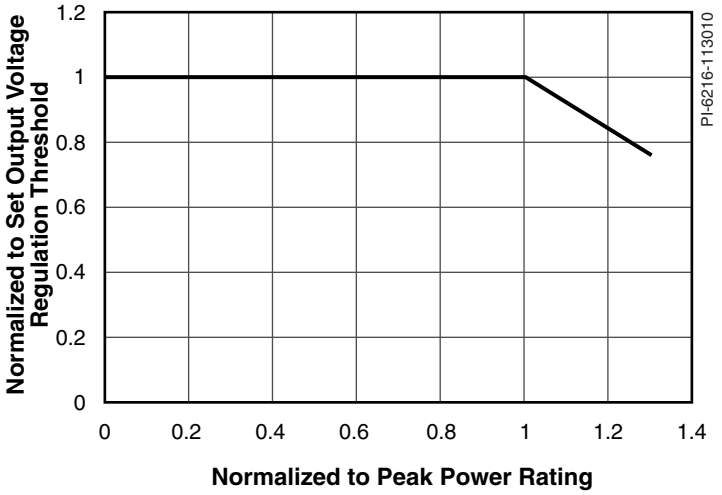


Figure 5. Typical Normalized Output Voltage Characteristics as Function of Normalized Peak Load Rating

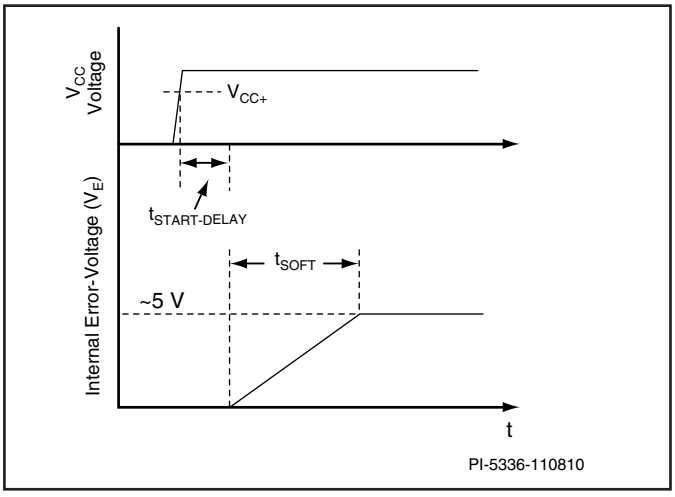


Figure 6. Power Limit Soft-Start Function.

NPN and PNP transistor are tied between the output voltage divider resistors to limit the maximum overshoot and undershoot during a load transient response. To reduce switch and output diode current stress at start-up, the HiperPFS slews the internal error-voltage from zero to its steady-state value at start-up. Figure 6 illustrates the relative relationship between the application of V_{CC} and power limit soft-start function through the internal error-voltage.

The error-voltage has a controlled slew rate of 0.25 V/ms at start-up, corresponding to the t_{SOFT} time duration for a full scale error voltage of 5 V.

The beginning of soft-start is gated by the V_{CC+}, I_{UV+} and FEEDBACK pin voltage thresholds in the sequence described below. Once the applied V_{CC} is above the V_{CC+} threshold, the sensed V pin current is above I_{UV+} and the feedback pin voltage is above FB_{OFF}, the IC applies a ~6 mA current sink through the VOLTAGE MONITOR pin and checks that the FEEDBACK pin voltage is still above the FB_{OFF} threshold. This checks to ensure that the FEEDBACK and V pins are not shorted together. In the event that the FEEDBACK pin voltage is below the FB_{OFF}

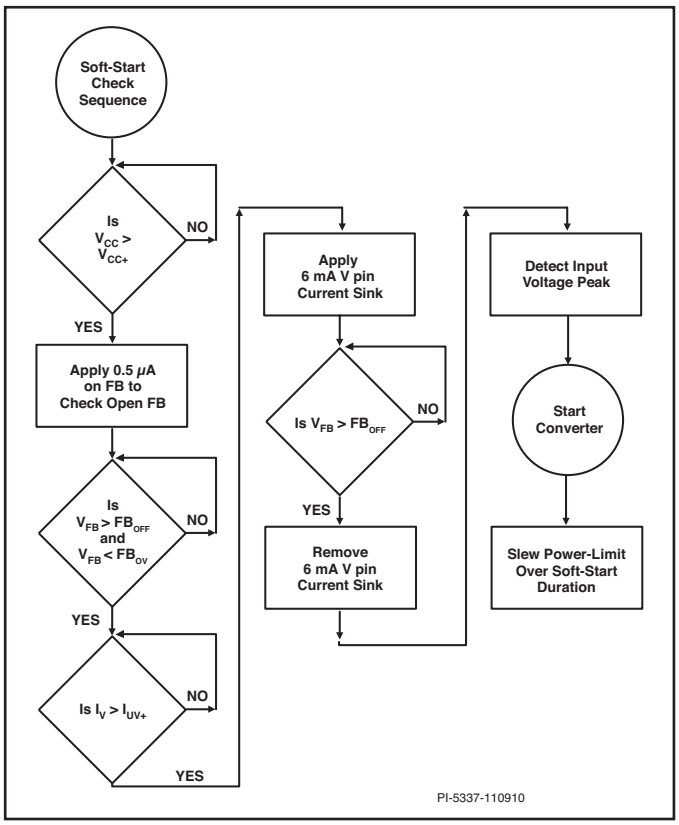


Figure 7. Start-Up Sequence.

threshold the V pin holds the 6 mA current sink indefinitely until the FEEDBACK pin is above the FB_{OFF}. If the FEEDBACK pin voltage is above FB_{OFF}, the IC releases the current source and resumes with normal soft-start and operation. Figure 7 illustrates this sequence.

Timing Supervisor and Operating Frequency Range

Since the controller is expected to operate with a variable switching frequency over the line frequency half-cycle, typically spanning a range of 24 – 95 kHz, the controller also features a timing supervisor function which monitors and limits the maximum switch on-time and off-time as well as ensures a minimum cycle off-time. The timer supervisor limits the normal operating frequency range for loads in excess of 10% of the device peak power rating.

Figure 8a shows the typical half-line frequency profile of the device switching frequency as a function of input voltage at peak load conditions. Figure 8b shows for a given line condition the effect of EcoSmart to the switching frequency as a function of load (PFS704-716). The switching frequency is not a function of boost choke inductance.

EcoSmart

The PFS704-716 controllers includes an EcoSmart mode wherein the internal error signal (V_E) is used to detect the converter output power. Since the internal error-signal is directly proportional to the output power, this signal level is used to set the average switching frequency as a function of output power. The off-time integrator control reference (V_{OFF}) is

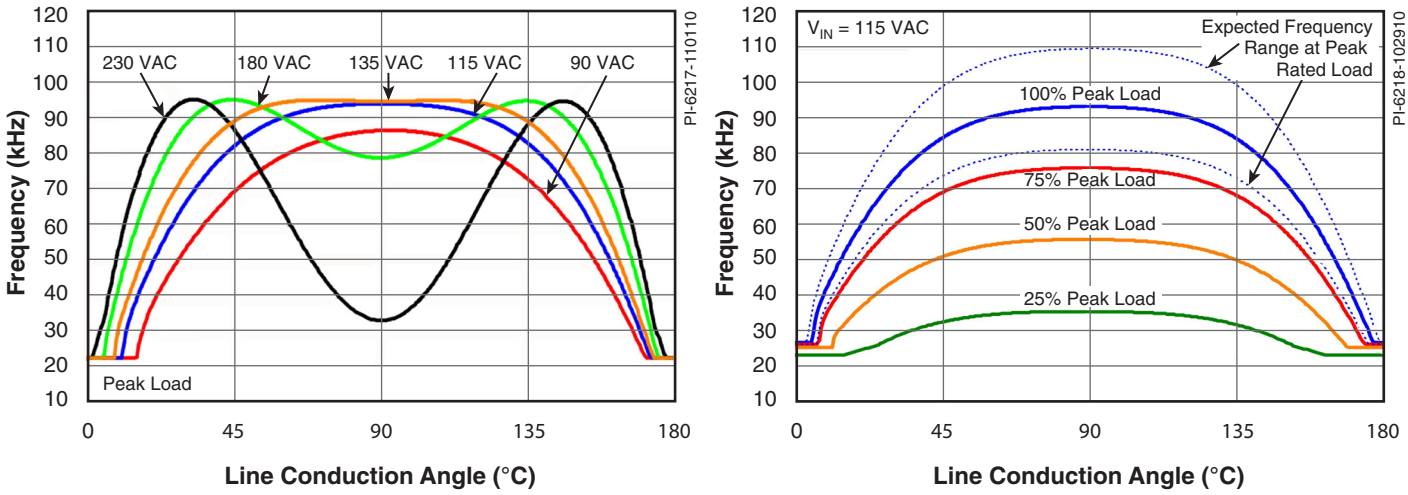


Figure 8. (a) Frequency Variation Over Line Half-Cycle as a Function of Input Voltage (b) Frequency Variation Over Line Half-Cycle as a Function of Load.

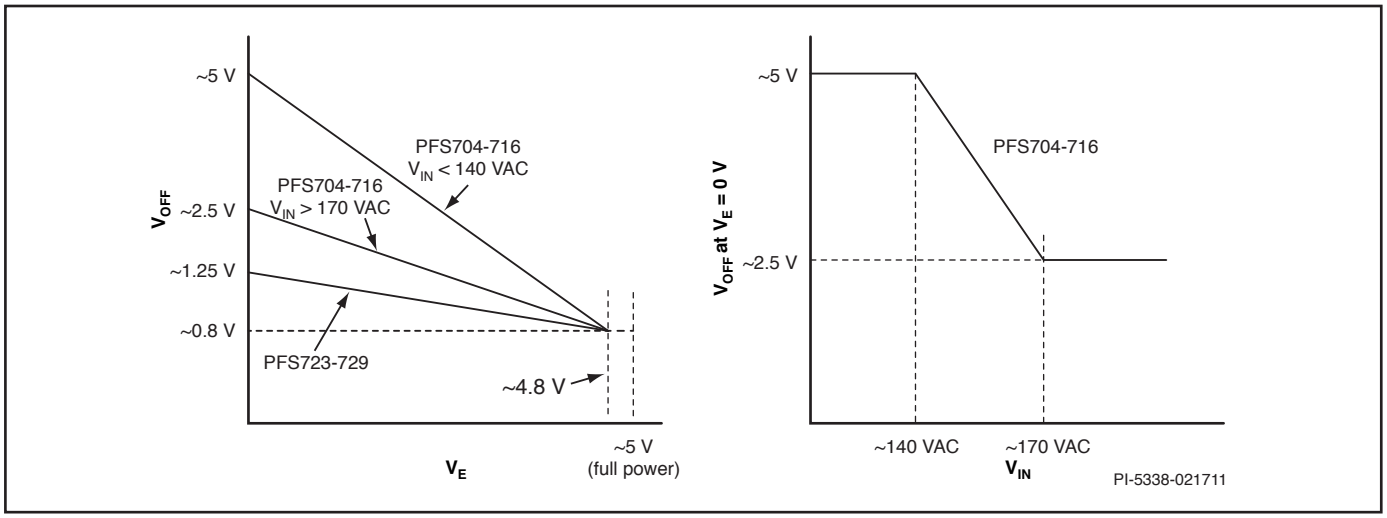


Figure 9. V_{OFF} vs. V_E and V_{OFF} vs. Input Voltage.

controlled with respect to the internal error-voltage level (output power) to allow the converter to maintain output voltage regulation and relatively flat conversion efficiency between 10% to 100% of rated load which is essential to meet many efficiency directives.

The degree of frequency slide is also controlled as a function of peak input line voltage, at high input line the maximum off-time voltage reference at zero error-voltage will be approximately 1/2 of the maximum value at low input line conditions.

The lower V_{OFF} slope reduces the average frequency swing for high input line operation.

Protection Modes

VOLTAGE MONITOR (V) Pin Shutdown

The VOLTAGE MONITOR pin features a shutdown protection mode which can be used with the VOLTAGE MONITOR pin resistor or external circuitry to cover system faults. During start-up (1 V < V_{FB} < 5.8 V) in the event the current through the VOLTAGE MONITOR pin exceeds the $I_{V(OFF)}$ threshold for a duration exceeding approximately (1 µs), the IC disables the internal MOSFET for the entire duration that the V pin current is above $I_{V(OFF)}$. In normal operation, if the current through the V pin exceeds the $I_{V(OFF)}$ threshold for a duration exceeding $t_{V(OFF)}$, the IC will reinitiate the start-up sequence.

Brown-In Protection (I_{UV+})

The VOLTAGE MONITOR pin features an input line undervoltage detection to limit the minimum start-up voltage detected through the V pin. This detection threshold will inhibit the device from starting at very low input AC voltage.

Brown-Out Protection (I_{UV-})

The V pin features a brown-out protection mode wherein the HiperPFS will turn-off when the V pin current is below the Line UV-threshold for a period exceeding the $t_{REFRESH}$ time period. In the event a single half-line cycle is missing (normal operating line frequency is 47 to 63 Hz) the brown-out protection will not be activated. The HiperPFS shutdown in effect gradually reduces the internal error-voltage to zero volts at rate of 1 V/ms

to decay the power MOSFET on-time to zero. At peak power (V_E ~5 V) the shutdown time will be approximately 5 ms. The internal error-voltage is held at 0 V for as long as the input peak voltage is below the brown-in (I_{UV+}) threshold. The internal error-voltage controlled slew to 0 V gradually reduces the switch on-time to zero to deplete energy stored in the boost choke as well as input EMI filter for power-down. Once the error-voltage reaches zero volts the controller is effectively in an off-state (gated by 5 ms timer) and will restart once all the conditions of soft-start are satisfied.

The brown-out threshold is reduced to I_{UV-SS} during start-up until the FEEDBACK pin exceeds approximately 5.8 V. Temporarily reducing the brown-out threshold prevents false turn-off at high power start-up when the voltage drop across the input bridge rectifier and filter stage may cause the rectified input to sag below the brown-out threshold.

Fast Output Voltage Overvoltage Protection (FB_{OV})
The FEEDBACK pin features a means to detect an output overvoltage condition through the FEEDBACK pin and disables the power MOSFET until the sensed output voltage falls below the FB_{OV} threshold. A deglitch filter (~2 μs) is used to prevent the controller from falsely triggering this mode. An FB_{OV} event in excess of the 2 μs delay will terminate the switch cycle immediately. This detection circuit also includes some hysteresis.

Output Voltage Undervoltage Protection (FB_{UV})
The FEEDBACK pin features an undervoltage detection to detect an output overload or a broken feedback loop. If the IC detects the falling edge on the FEEDBACK pin that has fallen below FB_{UV} threshold, it will turn-off the internal power MOSFET and reinitiate the start-up sequence. Similar to the FB_{OV} detection, this mode has a deglitch filter of approximately 100 μs.

VCC Undervoltage Protection (UVLO)
The BIAS POWER (VCC) pin has an undervoltage lock-out protection which inhibits the IC from starting unless the applied V_{CC} voltage is above the V_{CC+} threshold. The IC initiates a soft-start once the VCC pin voltage exceeds the V_{CC+} threshold. After start-up the IC will continue to operate until the VCC pin voltage has fallen below V_{CC-} level. The absolute maximum voltage of the VCC pin is 13.4 V which must be externally limited to prevent damage to the IC.

Over-Current Protection
The device includes a cycle-by-cycle over-current-protection (OCP) mode which protects the device in the event of a catastrophic fault. The OCP mode in the PFS704-716 is input line dependent as shown in Figure 10. The intention of OCP in this device is strictly protection of the internal power MOSFET and is not intended to protect the converter from output short-circuit or overload fault conditions.

The PFS704-716 controller latches the high line OCP for a 1/2 line cycle and updates the OCP status after the expiration of a 5 ms block-out timer. This feature has particular benefit for hard-start after an AC line cycle drop where the peak detector may falsely detect a low input line condition even though the input is at high input line.

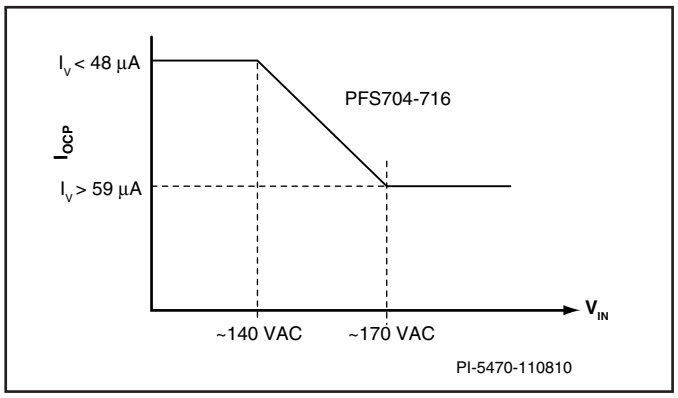


Figure 10. Line Dependant OCP.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time must be set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction.

Safe Operating Range (SOA) Mode
Since the cycle-by-cycle OCP mechanism described above does not prevent the possibility of inductor current "stair-casing", an SOA mode is required. Rapid build up of the device current can occur in event of inductor saturation or when the input and output voltages are equal (non or very short inductor reset time).

The SOA mode is triggered whenever the device reaches current limit (I_{OCP}) and the on-time is less than t_{SOA}.

The SOA mode forces an off-time equal to t_{OCP} and pulls the internal error-voltage (V_E) down to approximately 1/2 of its set value.

Open FEEDBACK Pin Protection
The FEEDBACK pin also features a static current of I_{FB} that is continuously sourced out of the pin to protect against a fault related to an open FEEDBACK pin. The internal current source introduces a static offset to the output regulation which must be accounted for in selecting the output feedback regulation components.

Hysteretic Thermal Shutdown
The thermal shutdown circuitry senses the controller die temperature. The threshold is set at 118 °C typical with a 50 °C hysteresis. When the die temperature rises above this threshold (118 °C +8/-7 °C), the power MOSFET switching is disabled and remains disabled until the die temperature falls by ~50 °C, at which point the device will reinitiate a soft-start and start-up sequence.

Output Power Table[1]

Product	Maximum Continuous Output Power Rating at 90 VAC[2]		Peak Output Power Rating at 90 VAC[5]	Product	Maximum Continuous Output Power Rating at 180 VAC[4]	Peak Output Power Rating at 180 VAC[5]
	Minimum[3]	Maximum				
PFS704EG	85 W	110 W	120 W	**PFS723EG**	255 W	280 W
PFS706EG	105 W	140 W	150 W	**PFS724EG**	315 W	350 W
PFS708EG	140 W	190 W	205 W	**PFS725EG**	435 W	480 W
PFS710EG	180 W	240 W	260 W	**PFS726EG**	540 W	600 W
PFS712EG	225 W	300 W	320 W	**PFS727EG**	675 W	750 W
PFS714EG	265 W	350 W	385 W	**PFS728EG**	810 W	900 W
PFS716EG	295 W	388 W	425 W	**PFS729EG**	900 W	1000 W

Table 2. Output Power Table.

Notes:
1. See Key Application considerations.
2. Maximum practical continuous power at 90 VAC in an open-frame design with adequate heat sinking, measured at 50 °C ambient.
3. Recommended lower range of maximum continuous power for **best light load efficiency**; HiperPFS will operate and perform below this level.
4. Maximum practical continuous power at 180 VAC in an open-frame design with adequate heat sinking, measured at 50 °C ambient.
5. Internal output power limit.

Application Example

A High Efficiency, 347 W, 380 VDC Universal Input PFC

The circuit shown in Figure 11 is designed using a PFS714EG device from the HiperPFS family of integrated PFC controllers. This design is rated for a continuous output power of 347 W and provides a regulated output voltage of 380 VDC nominal maintaining a high input power factor and overall efficiency from light load to full load.

Fuse F1 provides protection to the circuit and isolates it from the AC supply in case of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C3, C4, C5, C6 and C19 together with inductors L1, L2, L3 and L4 form the EMI filter reducing the common mode and differential mode noise. Resistors R1, R3 and CAPZero, IC U2 are required to discharge the EMI filter capacitors once the circuit is disconnected. CAPZero eliminates static losses in R1 and R2 by only connecting these components across the input when AC is removed.

The boost converter stage consists of inductor L5, diode rectifier D2 and the HiperPFS IC U1. This converter stage works as a boost converter and controls the input current of the power supply while simultaneously regulating the output DC voltage. Diode D1 prevents a resonant build up of output voltage at start-up by bypassing inductor L5 while simultaneously charging output capacitor C15. Thermistor RT1 limits the inrush input current of the circuit at start-up and prevents saturation of L5. In most high-performance designs, a relay will be used to bypass the thermistor after start-up to improve power supply efficiency. Therefore efficiency measurement, that represents the high performance configuration, the thermistors should be shorted. Capacitors C14 and C21 are used for reducing the loop length and area of the output circuit to reduce EMI and overshoot of voltage across the drain and source of the MOSFET inside U1 at each switching instant.

The PFS714EG IC requires a regulated supply of 12 V for operation and must not exceed 13.4 V. Resistors R6, R16, R17, Zener diode VR1, and transistor Q3 form a shunt regulator that prevents the supply voltage to IC U1 from exceeding 12 V. Capacitors C8, C18 and C20 filter the supply voltage and provide decoupling to ensure reliable operation of IC U1. Diode D5 prevents destruction of U1 if the auxiliary input is inadvertently connected reverse polarity.

The rectified AC input voltage of the power supply is sensed by IC U1 using resistors R4, R5 and R19. The capacitor C12 filters any noise on this signal.

Divider network comprising of resistors R9, R10, R11, R12, R13, and R14 are used to scale the output voltage and provide feedback to IC U1. The circuit comprising of diode D4, transistor Q1, Q2 and the resistors R12 and R13 form a non-linear feedback circuit which improves the load transient response by improving the response time of the PFC circuit.

Resistor R7, R8, R15, and capacitors C13 and C17 are required for shaping the loop response of the feedback network. The combination of resistor R8 and capacitor C13 provide a low frequency zero and the resistor R15 and capacitor C13 form a low frequency pole.

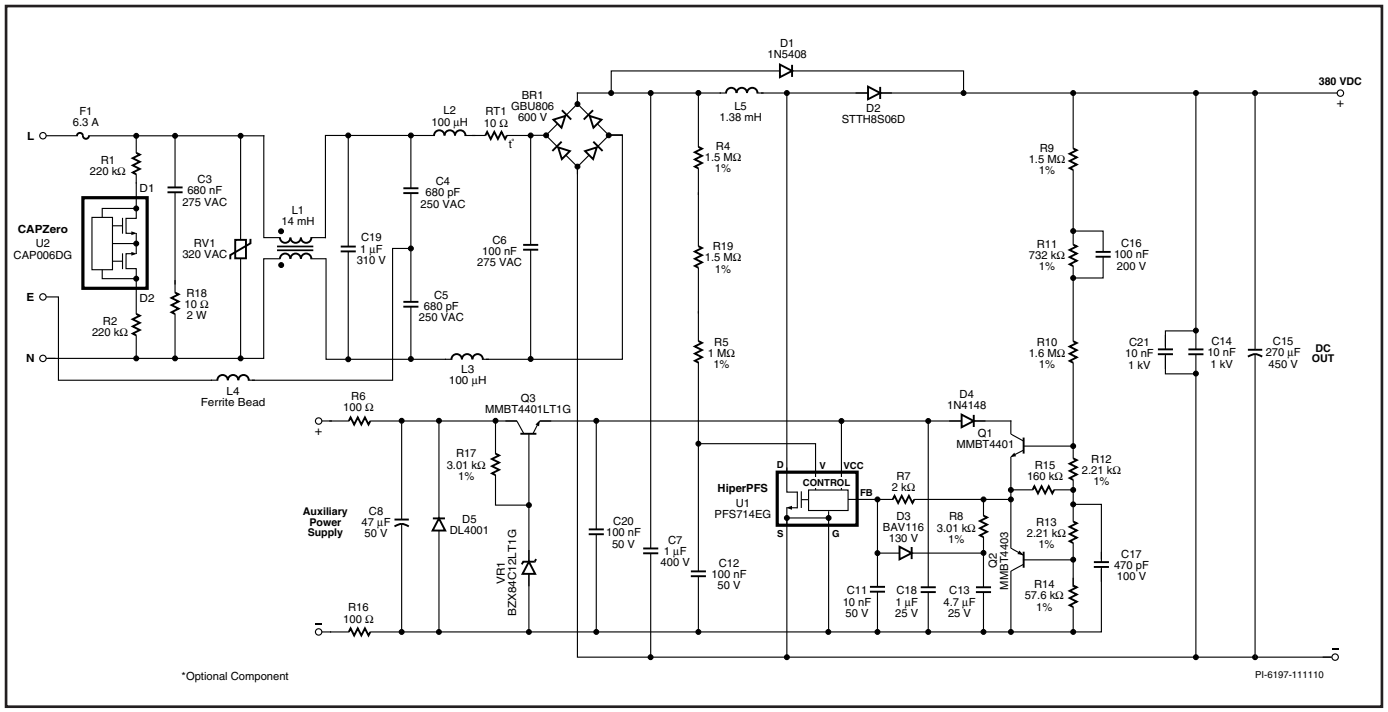


Figure 11. 347 W PFC using PFS714EG.

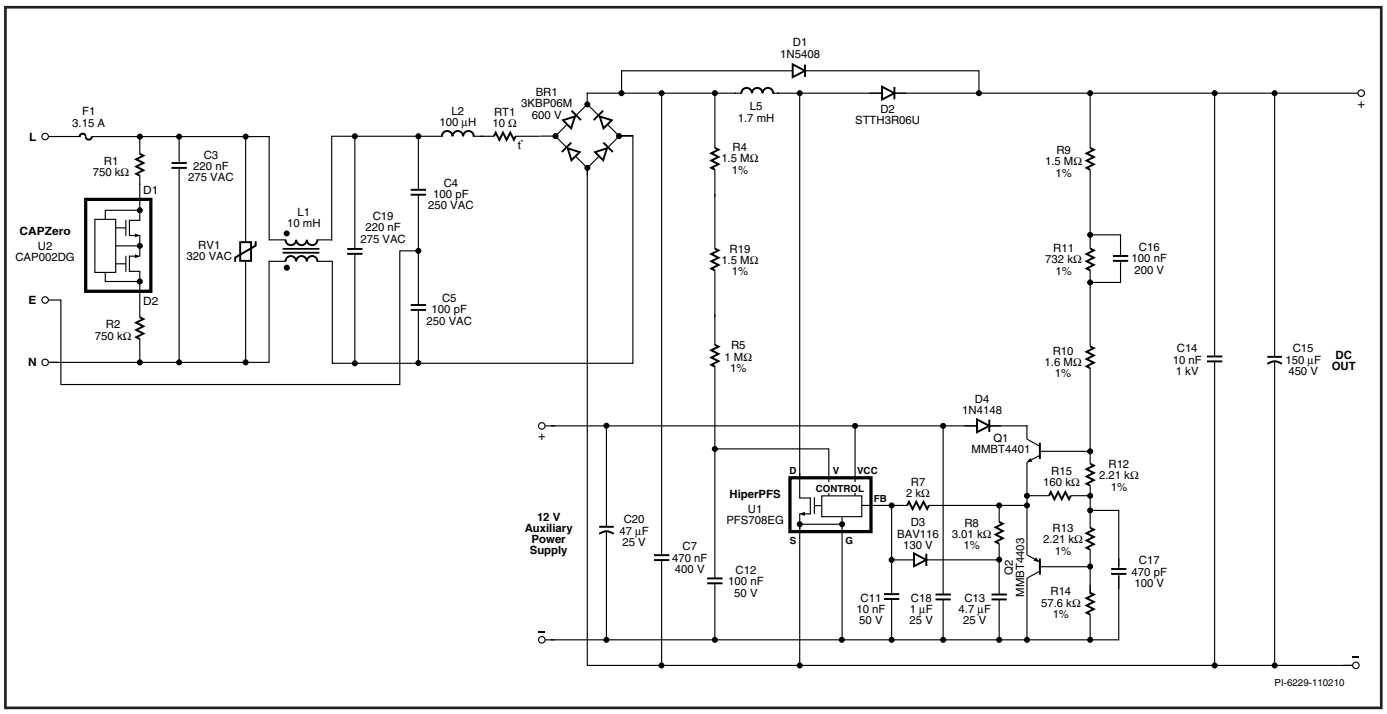


Figure 12. 180 W PFC using PFS708EG.

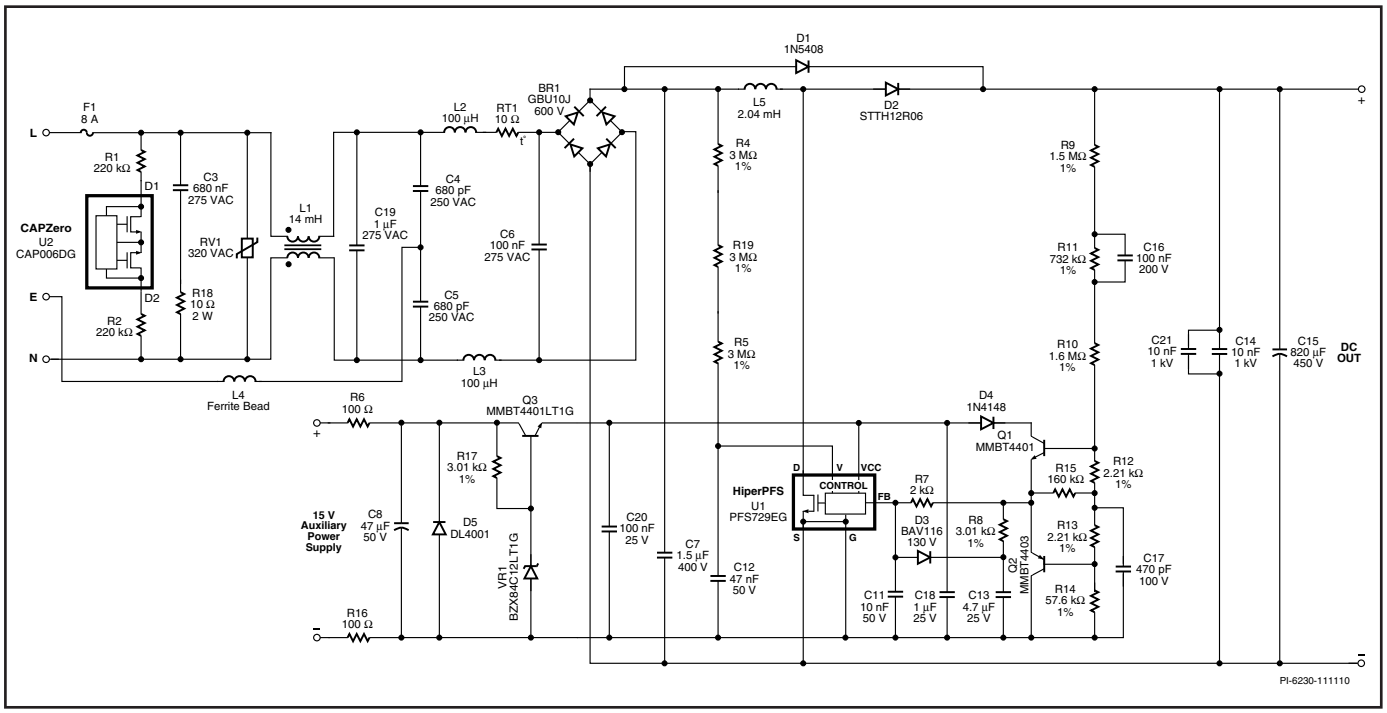


Figure 13. 900 W PFC using PFS729EG.

Design, Assembly, and Layout Considerations

Power Table

The data sheet power table as shown in Table 2 represents the maximum practical continuous output power based on the following conditions:

For the universal input devices (PFS704-716):

1. An input voltage range of 90 VAC to 264 VAC
2. Overall efficiency of at least 93% at the lowest operating voltage
3. Use of ultrafast recovery diode or high performance diode for PFC output.
4. Sufficient heat sinking to keep device temperature ≤100 ºC
5. 380 V to 385 V nominal output

For the 230 V only devices (PFS723-729):

1. An input voltage range of 180 VAC to 264 VAC
2. Overall efficiency of at least 96% at the lowest operating voltage
3. Use of ultrafast recovery diode or high performance diode for PFC output.
4. Sufficient heat sinking to keep device temperature ≤100 ºC
5. 380 V to 385 V nominal output

Operation beyond the limits stated above will require derating.

Use of a nominal output voltage higher than 390 V is not recommended for HiperPFS based designs. Operation at voltages higher than 390 V can result in higher than expected drain-source voltage during line and load transients.

HiperPFS Selection

Selection of the optimum HiperPFS part depends on required maximum output power, PFC efficiency and overall system efficiency (when used with a second stage DC-DC converter), heat sinking constraints, system requirements and cost goals. The HiperPFS part used in a design can be easily replaced with the next higher or lower part in the power table to optimize performance, improve efficiency or for applications where there are thermal design constraints. Minor adjustments to the inductance value and EMI filter components may be necessary in some designs when the next higher or the next lower HiperPFS part is used in an existing design for performance optimization.

Every HiperPFS family part has an optimal load level where it offers the most value. Operating frequency of a part will change depending on load level. Change of frequency will result in change in peak to peak current ripple in the inductance used. Change in current ripple will affect input PF and total harmonic distortion of input current.

Input Fuse and Protection Circuit

The input fuse should be rated for a continuous current above the input current at which the PFC turns-off due to input under voltage. This voltage is referred to as the brown-out voltage.

The fuse should also have sufficient I^2t rating in order to avoid nuisance failures during start-up. At start a large current is drawn from the input as the output capacitor charges to the peak of the applied voltage. The charging current is only limited by any inrush limiting thermistors, impedance of the EMI filter inductors and the forward resistance of the input rectifier diodes.

A MOV will typically be required to protect the PFC from line surges. Selection of the MOV rating will depend on the energy level (EN1000-4-5 Class level) to which the PFC is required to withstand.

Input EMI Filter

The variable switching frequency of the HiperPFS effectively modulates the switching frequency and reduces conducted EMI peaks associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for the average detection mode used in EMI measurements.

The PFC is a switching converter and will need an EMI filter at the input in order to meet the requirements of most safety agency standards for conducted and radiated EMI. Typically a common mode filter with X capacitors connected across the line will provide the required attenuation of high frequency components of input current to an acceptable level. The leakage reactance of the common mode filter inductor and the X capacitors form a low pass filter. In some designs, additional differential filter inductors may have to be used to supplement the differential inductance of the common mode choke.

A filter capacitor with low ESR and high ripple current capability should be connected at the output of the input bridge rectifier. This capacitor reduces the generation of the switching frequency components of the input current ripple and simplifies EMI filter design. Typically, 0.33 μF per 100 W should be used for universal input designs and 0.15 μF per 100 W of output power should be used for 230 VAC only designs.

It is often possible to use a higher value of capacitance after the bridge rectifier and reduce the X capacitance in the EMI filter.

Regulatory requirements require use of a discharge resistor to be connected across the input (X) capacitance on the AC side of the bridge rectifier. This is to ensure that residual charge is dissipated after the input voltage is removed when the capacitance is higher than 0.1 μF. Use of CAPZero integrated circuits from Power Integrations, helps eliminate the steady state losses associated with the use of discharge resistors connected permanently across the X capacitors.

Inductor Design

It is recommended that the inductor be designed with the maximum operating flux density less than 0.3 T and a peak flux density less than 0.42 T at maximum current limit when a ferrite core is used. If a core made from Sendust or MPP is used, the flux density should not exceed 1 T. A powder core inductor will have a significant drop in inductance when the flux density approaches 1 T.

For high-line only designs, the value of K_P (the ratio of peak to ripple current) of the drain current at the peak of the input voltage waveform should be kept below 0.5 for ferrite core and

0.675 for powder core designs respectively. For universal input designs, K_P should be kept below 0.25 for ferrite core and 0.625 for powder core respectively. For high performance designs, use of Litz wire is recommended to reduce copper loss due to skin effect and proximity effect. For toroidal inductors the numbers of layers should be less than 3 and for bobbin wound inductors, inter layer insulation should be used to minimize inter layer capacitance.

Output Diode

For a 385 V nominal PFC output voltage, use of a diode with 600 V or higher PIV rating is recommended. CCM operation with hard switching demands that diodes with low reverse recovery time and reverse recovery charge should be used. The variable frequency CCM operation of HiperPFS reduces diode switching losses as compared to fixed frequency solutions and enables use of easily available high frequency diodes such as the Turbo-2 series from STMicroelectronics. Diodes with soft recovery characteristics that result in a reduced EMI are available from a number of manufacturers. For highly demanding applications such as 80 PLUS Gold power supplies, use of Silicon Carbide diodes may be considered. These uses will typically provide further full load improvement in efficiency.

The diodes will be required to have a forward continuous current rating of at least 1.2 A to 1.5 A for every 100 W of output power.

Output Capacitor

For a 385 V nominal PFC, use of a electrolytic capacitor with 450 V or higher continuous rating is recommended. The capacitance required is dependent on the acceptable level of output ripple and any hold up time requirements. The equations below provide an easy way to determine the required capacitance in order to meet the hold up time requirement and also to meet the output ripple requirements. The higher of the two values would be required to be used:

Capacitance required for meeting the hold up requirement is calculated using the equation:

$$C_O = \frac{2 \times P_{OUT} \times t_{HOLD\_UP}}{V_{OUT}^2 - V_{OUT(MIN)}^2}$$

C_O	PFC output capacitance in F.
P_O	PFC output power in watts.
$t_{HOLD-UP}$	Hold-up time specification for the power supply in seconds.
V_{OUT}	Lowest nominal output voltage of the PFC in volts.
$V_{OUT(MIN)}$	Lowest permissible output voltage of the PFC at the end of hold-up time in volts.

Capacitance required for meeting the low frequency ripple specification is calculated using the equation:

$$C_O = \frac{I_{O(MAX)}}{2 \times \pi \times f_L \times \Delta V_O \times \eta_{PFC}}$$

f_L	Input frequency in Hz
ΔV_O	Peak-peak output voltage ripple in volts
η_{PFC}	PFC operating efficiency
$I_{O(MAX)}$	Maximum output current in amps

Capacitance calculated using the above method should be appropriately increased to account for ageing and tolerances.

Power Supply for the IC

A 12 V regulated supply should be used for the HiperPFS. If the V_{CC} exceeds 13.4 V, the HiperPFS may be damaged. In most applications a simple series pass linear regulator made using an NPN transistor and Zener diode is adequate since the HiperPFS only requires approximately 3.4 mA maximum for its operation.

It is recommended that a 1 μF or higher, low ESR ceramic capacitor be used to decouple the V_{CC} supply. This capacitor should be placed directly at the IC on the circuit board.

Line-Sense Network

The line-sense network connected to the V pin provides input voltage information to the HiperPFS. The value of this resistance sets the brown-in and brown-out threshold for the part. A value of 4 MΩ is recommended for use with the universal input parts and a value of 9 MΩ is recommended for the 230 VAC only parts. Only 1% tolerance resistors are recommended. This resistance value may be modified to adjust the brown-in threshold if required however change of this value will affect the maximum power delivered by the part.

A decoupling capacitor of 0.1 μF is required to be connected from the VOLTAGE MONITOR pin to the GROUND pin of the HiperPFS for the universal input parts and a decoupling capacitor of 0.047 μF is required for the 230 VAC only parts. This capacitor should be placed directly at the part on the circuit board.

Feedback Network

A resistor divider network that provides 6 V at the feedback pin at the rated output voltage should be used. The compensation elements are included with the feedback divider network since the HiperPFS does not have a separate pin for compensation. The HiperPFS based PFC has two loops in its feedback. It has an inner current loop and a low bandwidth outer voltage loop which ensures high input power factor. The compensation RC circuit included with the feedback network reduces the response time of the HiperPFS to fast changes in output voltage resulting from transient loads. The feedback circuit recommended for use with the HiperPFS includes a pair of transistors that are biased in a way that the transistors are in cutoff during normal operation. When a rapid change occurs in the output voltage, these transistors conduct momentarily to correct the feedback pin voltage rapidly thereby helping the HiperPFS to respond to the changes in output voltage without the delay associated with a low bandwidth feedback loop.

The recommended circuit and the associated component values are shown in Figure 14.

Resistors, R1 to R5 comprise of the main output voltage divider network. The sum of resistors R1, R2 and R3 is the upper divider resistor and the lower feedback resistor is comprised of the sum of resistors R4 and R5. Capacitor C1 is a soft-finish capacitor that reduces output voltage overshoot at start-up. Resistor R8 and capacitor C3 form a low pass filter to filter any switching noise from coupling into the FEEDBACK pin. Resistor

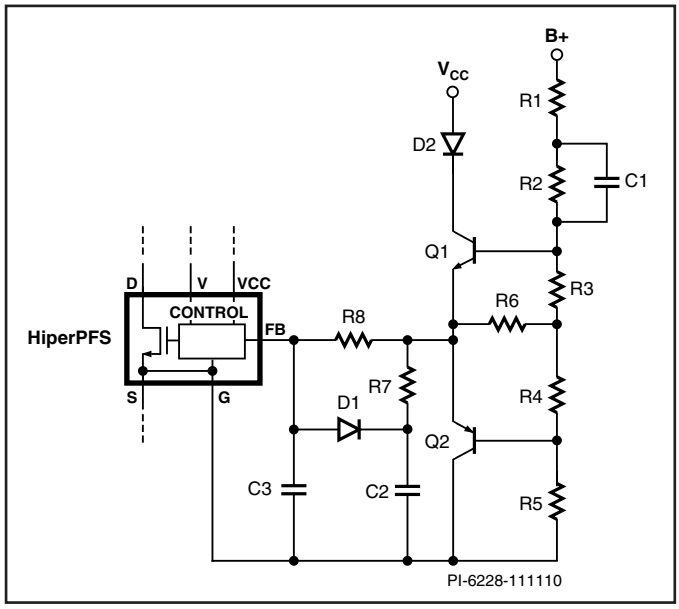


Figure 14. Recommended Feedback Circuit.

R7 and capacitor C2 is the loop compensation network which introduces a low frequency zero required to tailor the loop response to ensure low cross-over frequency and sufficient phase margin. Resistor R6 isolates the fast portion (resistor voltage divider network comprising of resistors R1 to R5) and the slow feedback loop compensator circuit (resistor R7 and capacitor C2). Transistors Q1 and Q2, biased with resistors R3 and R4 respectively, detect output voltage transient conditions and provide the FEEDBACK pin with "fast" information to increase the loop response of the system. Diode D1 is included to cover a single point fault condition wherein capacitor C2 is shorted. In the event C2 is short-circuited, the FEEDBACK pin is forced below the FB_{OFF} threshold through diode D1 and subsequently turns the HiperPFS off. Only a standard recovery diode should be used for D1. Use of ultrafast or fast recovery diode is not recommended including small signal diodes (e.g. 1N4148) which are typically also fast recovery.

The recommended values for the components used are as follows:
R5 = 57.6 kΩ
R3, R4 = 2.2 kΩ
R2 = 732 kΩ
C1 = 0.1 μF, 100 V X7R/NPO
R6 = 160 kΩ
R7 = 3 kΩ
R8 = 2 kΩ
C2 = 4.7 μF
C3 = 10 nF (For layouts that result in excessive noise on the feedback signal, a 20 nF capacitor may be used).
D1 = BAV116 W or 1N4007 (A general purpose standard recovery diode should only be used).
Q1, Q2 = Small signal transistors equivalent to 2N4401 and 2N4403.

When the above component values are used, the value of resistor R1 can be calculated using the equation below:

$$R_1 = \frac{V_O - 79}{100 \times 10^{-6}}$$

Since the total voltage across resistor R1 is approximately 301 V, resistor R1 may have to be divided into two or more resistors to distribute the voltage stress below the voltage ratings of the resistor used.

The value of resistor R7 will have to be adjusted in some designs and as a guideline the value from the following calculation can be used:

$$R_7 = R_Z = \frac{P_O}{4 \times V_O^2 \times C_O}(k\Omega)$$

P_O Maximum continuous output power in watts
V_O Nominal PFC output voltage in volts
C_O PFC output capacitance in farads

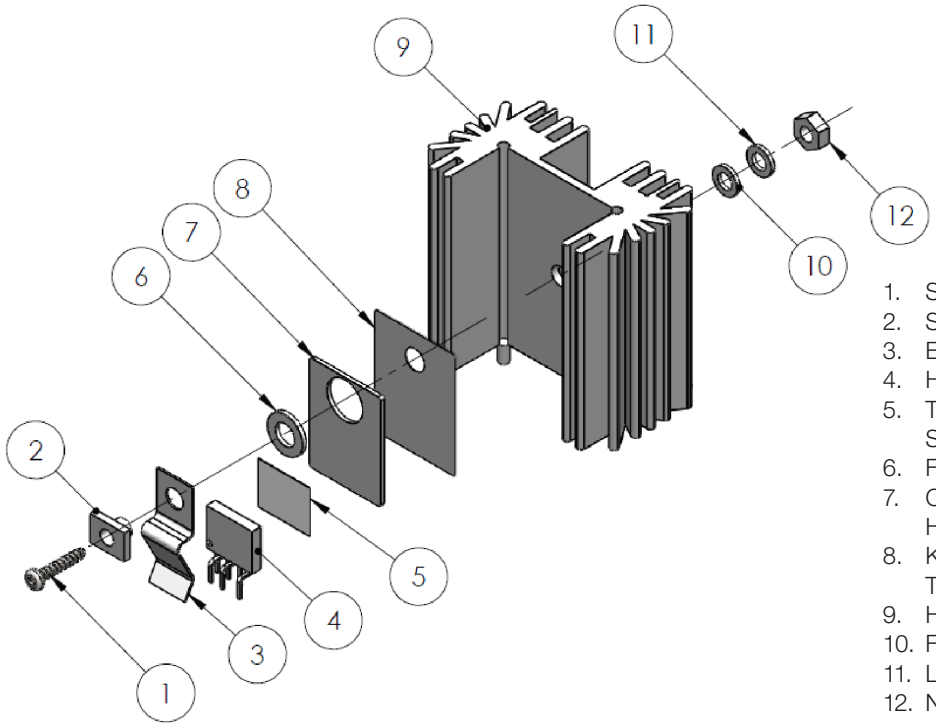
Improvement in low frequency phase margin can be achieved by increasing the value of the capacitor C2 however increase in value of capacitor C2 will result in some increase in overshoot at the output of the PFC during transient loading and should be verified.

Diode D2 connected in series with the collector of the NPN transistor Q1 is to prevent loading of the feedback circuit when the V_{CC} is absent. Presence of this diode ensures that there is no start-up delay when the V_{CC} is applied to the HiperPFS, the feedback circuit, and transistor.

Heat Sinking and Thermal Design
The exposed pad on the HiperPFS eSIP package is internally connected to the drain of the MOSFET. Due to the significant amount of power dissipated in the part, the HiperPFS should be mounted on a rectangular heat spreader made of thermally conductive material such as Aluminum or Copper. Figure 15 shows an example of the recommended assembly for the HiperPFS. In this assembly shown, a 0.76 mm thick aluminum heat spreader is used. A thermally conductive sil pad should be used to separate the heat spreader from the heat sink. A thin film of thermally conductive silicone grease should be applied to the rear surface of the HiperPFS to ensure low thermal resistance contact between the package of the HiperPFS and the heat spreader.

For universal input applications up to 150 W and 230 VAC only applications up to 300 W, the heat spreader is not essential. Use of heat spreader in these applications will help reduce temperature of the part and heat spreaders can be used if necessary. Figure 17 shows an example of the recommended assembly for lower power designs that do not need a heat spreader.

The HiperPFS is electrically connected to the heat spreader and the heat sink is required to be connected to the source in order to reduce EMI. The voltage between the heat spreader and heat sink can easily exceed 400 V during transient conditions. Attention should be placed on creepage and clearance based on applicable safety specification.



1. SCREW
2. SHOULDER WASHER
3. EDGE CLIP
4. HiperPFS
5. THERMALLY CONDUCTIVE SILICONE GREASE
6. FIBER WASHER
7. CUSTOM ALUMINUM HEATSPREADER
8. KAPTON SILPAD INSULATOR TO-247
9. HEAT SINK
10. FLAT WASHER
11. LOCK WASHER
12. NUT

Figure 15. Heat Sink Assembly Example – High Power Designs.

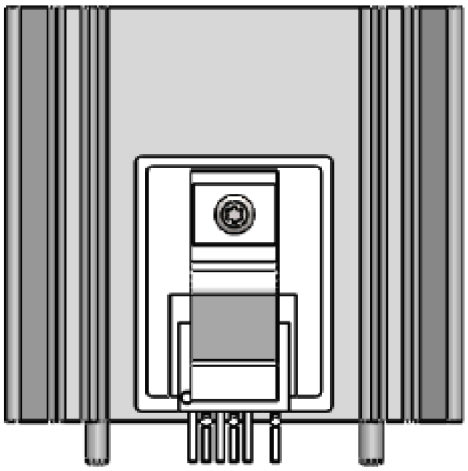


Figure 16. Heat Sink Assembly – High Power Designs.

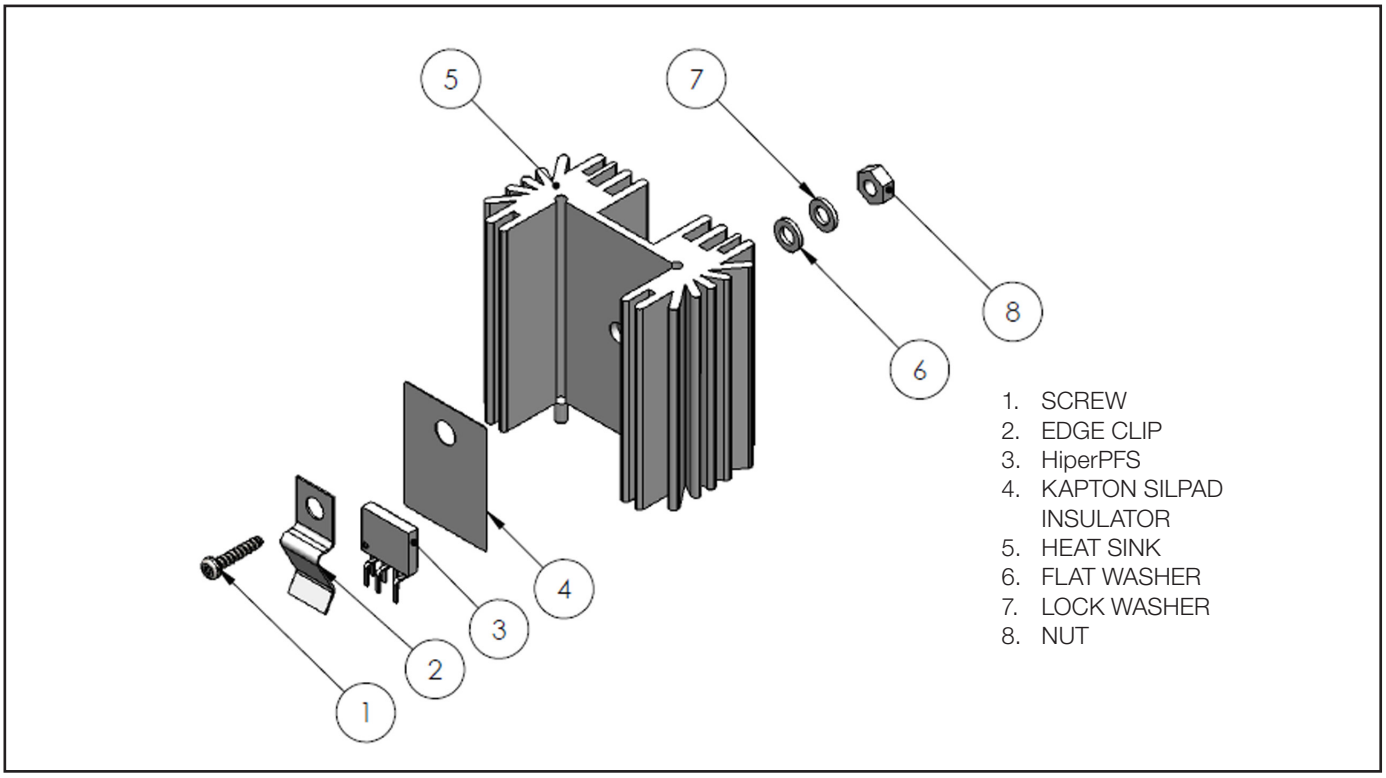


Figure 17. Heat Sink Assembly Example – Low Power Designs.

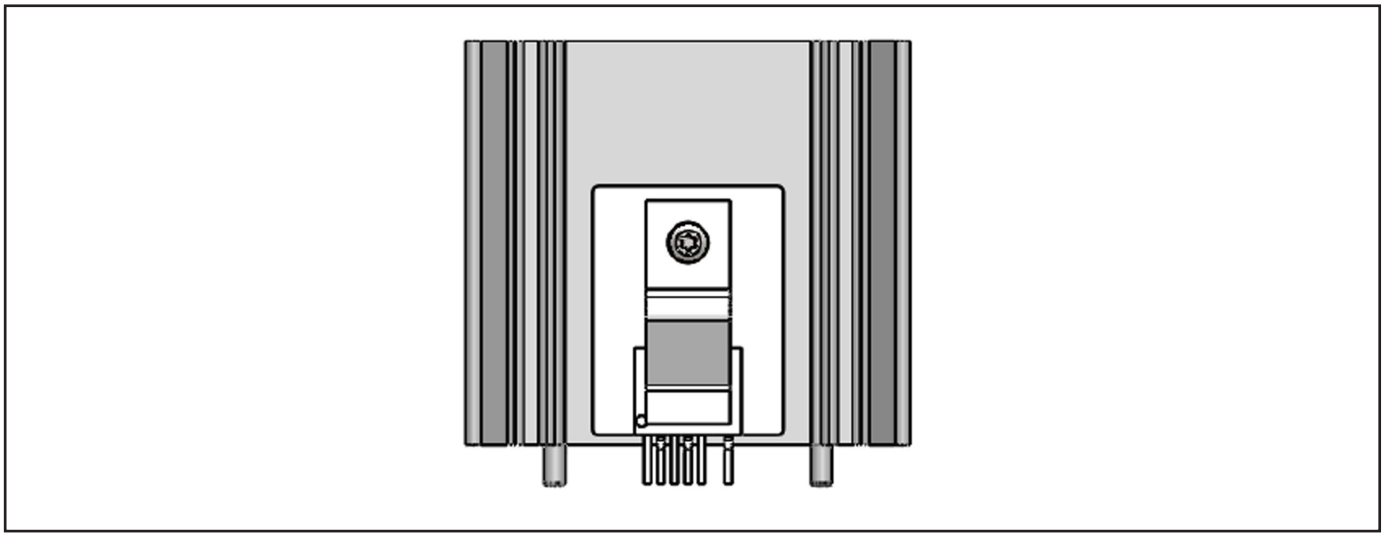


Figure 18. Heat Sink Assembly – Low Power Designs.

PCB Design Guidelines and Design Example

The line-sense network and the feedback circuit use large resistance values in order to minimize power dissipation in the feedback network and the line-sense network. Care should be taken to place the feedback circuit and the line-sense network components away from the high voltage and high current nodes to minimize any interference. Any noise injected in the feedback network or the line-sense network will typically manifest as degradation of power factor. Excessive noise injection can lead to waveform instability or dissymmetry.

The EMI filter components should be clustered together to improve filter effectiveness. The placement of the EMI filter components on the circuit board should be such that the input circuit is located away from the drain node of the HiperPFS, the output diode of the PFC or the PFC inductor.

A filter or decoupling capacitor should be placed at the output of the bridge rectifier. This capacitor together with the X capacitance in the EMI filter and the differential inductance of the EMI filter section and the source impedance, works as a filter to reduce the switching frequency current ripple in the input current. This capacitor also helps to minimize the loop area of the switching frequency current loop thereby reducing EMI.

The connection between the HiperPFS drain node, output diode drain terminal and the PFC inductor should be kept as small as possible.

A low loss ceramic dielectric capacitor should be connected between the cathode of the PFC output diode and the source terminal of the HiperPFS. This ensures that the loop area of the loop carrying high frequency currents at the transition of switch-off of the MOSFET small and helps to reduce radiated EMI due to high frequency pulsating nature of the diode current traversing through the loop.

During placement of components on the board, it is best to place the VOLTAGE MONITOR pin, FEEDBACK pin and VCC pin decoupling capacitors close to the HiperPFS before the other components are placed and routed. Power supply return trace from the GROUND pin should be separate from the trace connecting the feedback circuit components to the GROUND pin.

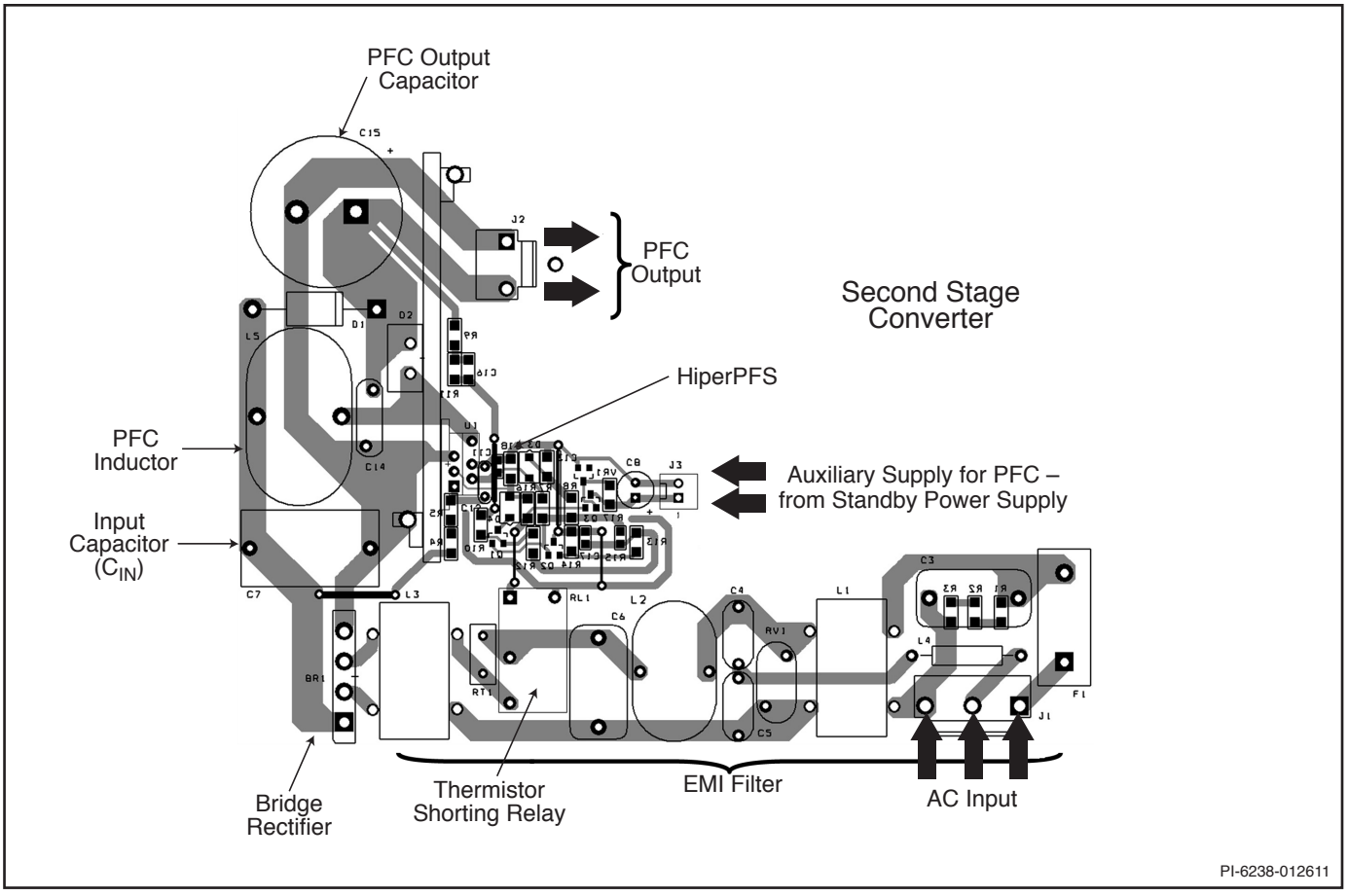


Figure 19. PCB Layout Example for System Power Supply consisting of a PFC and a Second Stage Converter.

To minimize effect of trace impedance affecting regulation, output feedback should be taken directly from the output capacitor positive terminal. The upper end of the line-sense resistors should be connected to the high frequency filter capacitor connected at the output of the bridge rectifier.

Quick Design Checklist

As with any power supply design, all HiperPFS designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – verify that peak V_{DS} does not exceed 530 V at lowest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just above the highest rated load or before the power supply output voltage starts falling out of regulation. Additional external snubbers should be used if this voltage is exceeded. In most designs, addition of a ceramic capacitor in the range of 33 pF and 100 pF connected across the PFC output diode will reduce the maximum drain-source voltage to a level below the BV_{DSS} rating. When measuring drain-source voltage of the MOSFET, a high voltage probe should be used. When the probe tip is removed, a silver ring in the vicinity of the probe tip can be seen. This ring is at ground potential and the best ground connection point for making noise free measurements. Wrapping stiff wire around the ground ring and then connecting that ground wire into the circuit with the shortest possible wire length, and connecting the probe tip to the point being measured, ensures error free measurement.
2. Maximum drain current – at maximum ambient temperature, minimum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of inductor saturation and excessive leading edge current spikes. HiperPFS has a leading edge blanking time of 220 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit for the drain current waveform at the end of the 220 ns blanking period. If a wire loop is inserted in series with the drain, it forms a small stray inductance in series with the drain. This stray inductance will add to the leading edge voltage spike on the drain source waveform. The drain-source voltage waveform should therefore never be measured with this loop. An alternate measurement that can provide drain current level and information regarding slope of the inductor current can be obtained by monitoring the inductor current instead. A wire loop can be added in series with the PFC inductor connection that connects the inductor to the input rectifier for the purpose of measurement.
3. Thermal check – at maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for the HiperPFS, PFC inductor, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of HiperPFS, as specified in the data sheet. A maximum package temperature of 100 °C is recommended to allow for these variations.
4. Input PF should improve with load, if performance is found to progressively deteriorate with loading then that is a sign of possible noise pickup by the VOLTAGE MONITOR pin circuit or the feedback divider network and the compensation circuit.

Absolute Maximum Ratings

DRAIN Pin Peak Current: PFS704 ..... 7.5 A
PFS706 ..... 9.0 A
PFS708 ..... 11.3 A
PFS710 ..... 13.5 A
PFS712 ..... 15.8 A
PFS714 ..... 18.0 A
PFS716 ..... 21.0 A
PFS723 ..... 7.5 A
PFS724 ..... 9.0 A
PFS725 ..... 11.3 A
PFS726 ..... 13.5 A
PFS727 ..... 15.8 A
PFS728 ..... 18.0 A
PFS729 ..... 21.0 A

DRAIN Pin Voltage ..... -0.3 V to 530 V
VCC Pin Voltage ..... -0.3 V to 13.4 V
VCC Pin Current ..... 25 mA
VOLTAGE MONITOR Pin Voltage ..... -0.3 V to 9 V
FEEDBACK Pin Voltage ..... -0.3 V to 9 V
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature[2] ..... -40 °C to 150 °C
Lead Temperature[3] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.

Thermal Resistance

Thermal Resistance: e Package:
(θ_{JA})[1] ..... 103 °C/W
(θ_{JC}) ..... (see Figure 20)

Notes:
1. MOSFET only – controller junction temperature (T_C) may be less than the power MOSFET junction temperature (T_M).

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
Maximum Operating ON-time	$t_{ON(MAX)}$	0 °C < T_C < 100 °C	30	40	50	µs
Minimum Operating ON-time	$t_{ON(MIN)}$	See Note A 0 °C < T_C < 100 °C	0		1	
Maximum Operating OFF-time	$t_{OFF(MAX)}$	0 °C < T_C < 100 °C	30	40	50	
Minimum Operating OFF-time	$t_{OFF(MIN)}$	0 °C < T_C < 100 °C	1		3	
Internal Feedback Voltage Reference	V_{REF}	T_C = 25 °C See Note A	5.955	6.00	6.045	V
FEEDBACK Pin Voltage	V_{FB}	0 °C < T_C < 100 °C (In Regulation)	5.82	6.00	6.18	V
FEEDBACK Pin Current	I_{FB}	T_C = 25 °C	340	500	640	nA
Soft-Start Time	t_{SOFT}	T_C = 25 °C	12			ms
Internal Compensation Frequency	f_{COMP}	See Note A Pole (fp)		1		kHz
Error-Amplifier Gain	A_v	See Note A		100		-

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)	Min	Typ	Max	Units
Line-Sense/Peak Detector						
Brown-In Threshold Current	I_{UV+}	0 °C < T_C < 100 °C		27.50	28.88	µA
Brown-Out Threshold Current	I_{UV-}	0 °C < T_C < 100 °C	22.52	24.50		µA
Brown-In/Out Hysteresis	$I_{UV(HYST)}$	T_C = 25 °C	1		5.5	µA
Soft-Start Brown-Out Threshold Current	I_{UV-SS}	T_C = 25 °C	20.5	22.5	24.5	µA
VOLTAGE MONITOR Pin Voltage Threshold	$V_{V(THR)}$	0 °C < T_C < 100 °C I_V = I_{UV+}		2.3		V
VOLTAGE MONITOR Pin Short-Circuit Current	$I_{V(SC)}$	0 °C < T_C < 100 °C V_V = 6 V		350		µA
VOLTAGE MONITOR Pin Pre-Soft-Start Current	$I_{V(SS)}$	0 °C < T_C < 100 °C V_V = 3 V		6		mA
Maximum Line Sample Refresh Period	$T_{REFRESH}$	T_C = 25 °C	30		60	ms
VOLTAGE MONITOR Pin Shutdown Current Threshold	$I_{V(OFF)}$	0 °C < T_C < 100 °C		200		µA
VOLTAGE MONITOR Pin Shutdown Delay	$t_{V(OFF)}$	T_C = 25 °C	65	110	135	µs

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)		Min	Typ	Max	Units
Current Limit/Circuit Protection							
Over-Current Protection	I_{OCP}	PFS704 di/dt = 250 mA/µs T_C = 25 °C	I_V < 48 µA	3.8	4.1	4.3	A
			I_V > 59 µA	2.5	2.7	2.8	
		PFS706 di/dt = 300 mA/µs T_C = 25 °C	I_V < 48 µA	4.5	4.8	5.1	
			I_V > 59 µA	3.0	3.2	3.4	
		PFS708 di/dt = 400 mA/µs T_C = 25 °C	I_V < 48 µA	5.5	5.9	6.2	
			I_V > 59 µA	3.7	4.0	4.2	
		PFS710 di/dt = 500 mA/µs T_C = 25 °C	I_V < 48 µA	6.8	7.2	7.5	
			I_V > 59 µA	4.6	4.9	5.1	
		PFS712 di/dt = 650 mA/µs T_C = 25 °C	I_V < 48 µA	8.0	8.4	8.8	
			I_V > 59 µA	5.4	5.7	6.0	
		PFS714 di/dt = 800 mA/µs T_C = 25 °C	I_V < 48 µA	9.0	9.5	9.9	
			I_V > 59 µA	6.0	6.3	6.6	
		PFS716 di/dt = 920 mA/µs T_C = 25 °C	I_V < 48 µA	9.5	10.0	10.5	
			I_V > 59 µA	6.3	6.7	7.0	
		PFS723 di/dt = 250 mA/µs T_C = 25 °C		3.8	4.1	4.3	
		PFS724 di/dt = 300 mA/µs T_C = 25 °C		4.5	4.8	5.1	
		PFS725 di/dt = 400 mA/µs T_C = 25 °C		5.5	5.9	6.2	
		PFS726 di/dt = 500 mA/µs T_C = 25 °C		6.8	7.2	7.5	
		PFS727 di/dt = 650 mA/µs T_C = 25 °C		8.0	8.4	8.8	
		PFS728 di/dt = 800 mA/µs T_C = 25 °C		9.0	9.5	9.9	
		PFS729 di/dt = 920 mA/µs T_C = 25 °C		9.7	10.2	10.7	

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)	Min	Typ	Max	Units
Current Limit/Circuit Protection (cont.)						
SOA Protection Time-out	t_{OCP}	T_C = 25 °C	200	280	360	µs
SOA On-time	t_{SOA}	See Note A			1	µs
Leading Edge Blanking Time	t_{LEB}	See Note A		220		ns
Current Limit Delay	$t_{IL(D)}$	See Note A		100		ns
LEB + ILD + Driver Delay	$t_{LEB} + t_{IL(D)} + t_{DRIVER}$	T_C = 25 °C	370	470	570	ns
Thermal Shutdown Temperature	T_{SHUT}	See Note A	111	118	126	°C
Thermal Shutdown Hysteresis	T_{HYST}	See Note A		50		°C
FEEDBACK Pin Undervoltage	FB_{UV}	T_C = 25 °C	3	3.5	4	V
FEEDBACK Pin Undervoltage Delay	$t_{FB(UV)}$	T_C = 25 °C	65	110	135	µs
FEEDBACK Pin Overvoltage Threshold and Hysteresis	FB_{OV}	0 °C < T_C < 100 °C Threshold	V_{FB} +40 mV	V_{FB} +90 mV	V_{FB} +160 mV	V
		0 °C < T_C < 100 °C Hysteresis		75		mV
FEEDBACK Pin Overvoltage Delay	$t_{FB(OV)}$	T_C = 25 °C	1	2	3	µs
FEEDBACK Pin Start-Up Threshold	FB_{OFF}	0 °C < T_C < 100 °C	0.5	1.2	1.65	V
FEEDBACK Pin OFF Delay	$t_{FB(OFF)}$	0 °C < T_C < 100 °C	0.5	2	4	µs
Start-Up V_{CC} (Rising Edge)	V_{CC+}	T_C = 25 °C	9.5		10.2	V
Shutdown V_{CC} (Falling Edge)	V_{CC-}	T_C = 25 °C	9.0		9.5	V
V_{CC} Hysteresis	$V_{CC(HYST)}$	T_C = 25 °C	0.2	0.5	0.8	V
Supply Current Characteristics	I_{CD1}	0 °C < T_C < 100 °C Switching			3.5	mA
	I_{CD2}	0 °C < T_C < 100 °C Not Switching			1.5	
V_{CC} Power-Up Reset Threshold	$V_{CC(POR)}$	T_C = 25 °C	2.85	3.6	4.25	V
V_{CC} Power-Up Reset Current	$I_{VCC(POR)}$	T_C = 25 °C			1.5	mA

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)			Min	Typ	Max	Units
Power MOSFET								
ON-State Resistance	$R_{DS(ON)}$	PFS704	$I_D = I_{OCP} \times 0.5$ See Note E	T_M = 25 °C		0.61	0.72	Ω
				T_M = 100 °C			1.16	
		PFS706		T_M = 25 °C		0.52	0.61	
				T_M = 100 °C			0.97	
		PFS708		T_M = 25 °C		0.41	0.48	
				T_M = 100 °C			0.77	
		PFS710		T_M = 25 °C		0.35	0.41	
				T_M = 100 °C			0.65	
		PFS712		T_M = 25 °C		0.30	0.35	
				T_M = 100 °C			0.55	
		PFS714		T_M = 25 °C		0.26	0.31	
				T_M = 100 °C			0.48	
		PFS716		T_M = 25 °C		0.22	0.26	
				T_M = 100 °C			0.42	
		PFS723		T_M = 25 °C		0.58	0.69	
				T_M = 100 °C			1.10	
		PFS724		T_M = 25 °C		0.49	0.58	
				T_M = 100 °C			0.92	
		PFS725		T_M = 25 °C		0.39	0.46	
				T_M = 100 °C			0.73	
		PFS726		T_M = 25 °C		0.33	0.39	
				T_M = 100 °C			0.62	
		PFS727		T_M = 25 °C		0.28	0.33	
				T_M = 100 °C			0.52	
		PFS728		T_M = 25 °C		0.25	0.29	
				T_M = 100 °C			0.46	
		PFS729		T_M = 25 °C		0.21	0.25	
				T_M = 100 °C			0.40	

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)		Min	Typ	Max	Units
Power MOSFET (cont.)							
Effective Output Capacitance	C_{OSS}	T_C = 25 °C, V_{GS} = 0 V, V_{DS} = 0 to 80% V_{DSS} See Note A	PFS704			176	pF
			PFS706			210	
			PFS708			265	
			PFS710			312	
			PFS712			320	
			PFS714			420	
			PFS716			487	
			PFS723			185	
			PFS724			221	
			PFS725			278	
			PFS726			328	
			PFS727			389	
			PFS728			441	
			PFS729			511	
Breakdown Voltage	BV_{DSS}	T_M = 25 °C, V_{CC} = 12 V I_D = 250 µA, V_{FB} = V_V = 0 V		530			V
Breakdown Voltage Temperature Coefficient	$BV_{DSS(TC)}$				0.048		%/°C

Parameter	Symbol	Conditions SOURCE = 0 V; T_C = -40 °C to 125 °C (Note D) (Unless Otherwise Specified)		Min	Typ	Max	Units
Power MOSFET (cont.)							
OFF-State Drain Current Leakage	I_{DSS}	T_M = 100 °C V_{DS} = 80% BV_{DSS} V_{CC} = 12 V V_{FB} = V_V = 0	PFS704			80	µA
			PFS706			100	
			PFS708			120	
			PFS710			150	
			PFS712			170	
			PFS714			200	
			PFS716			235	
			PFS723			84	
			PFS724			105	
			PFS725			126	
			PFS726			158	
			PFS727			179	
			PFS728			210	
			PFS729			247	
Turn-Off Voltage Rise Time	t_R	See Note A, B, C			50		ns
Turn-On Voltage Fall Time	t_F				100		
Start-up Time Delay	$t_{START-DELAY}$	0 °C < T_C < 100 °C See Note A, B, C		2	6	10	ms

NOTES:
A. Not a tested parameter. Guaranteed by design.
B. Tested in typical boost PFC application circuit with 0.1 µF capacitor between the V pin and G pin and a 4 MΩ resistor from rectified line to the V pin for PFS70x and PFS71x.
C. Tested in typical boost PFC application circuit with 0.047 µF capacitor between the V pin and G pin and a 9 MΩ resistor from rectified line to the V pin for PFS72x.
D. Normally limited by internal circuitry.
E. Refer to I_{OCP} with I_V <48 µA for PFS704-716.

Typical Performance Characteristics

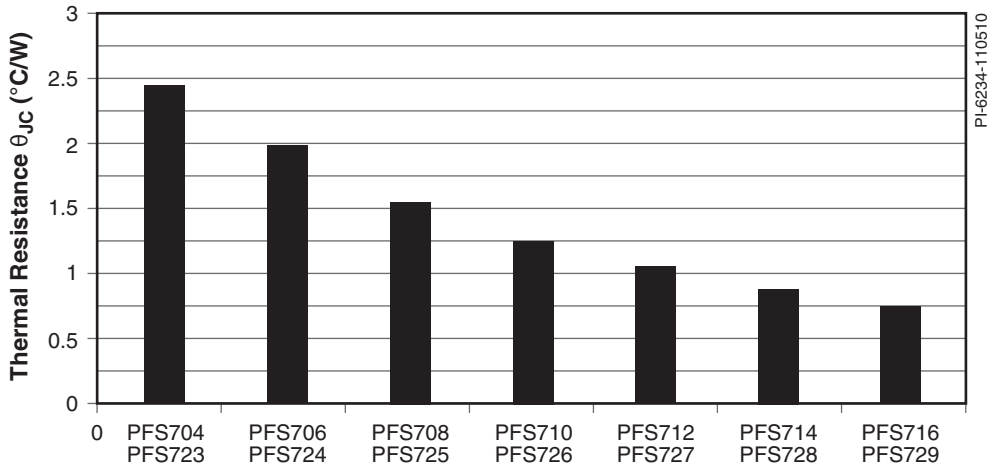


Figure 20. Thermal Resistance (θ_{JC}).

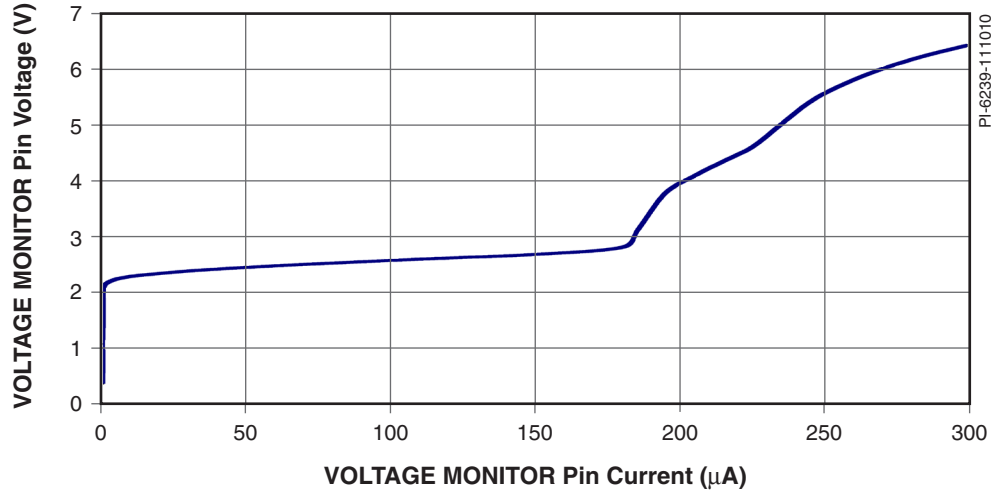


Figure 21. Typical Characteristic: VOLTAGE MONITOR Pin Voltage vs. Current.

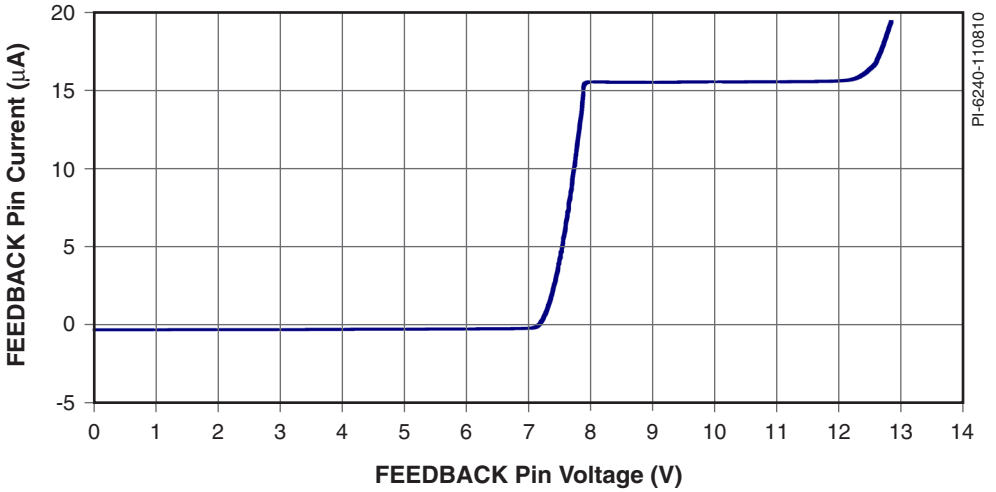


Figure 22. Typical Characteristic: FEEDBACK Pin Current vs. Voltage.

Typical Performance Characteristics (cont.)

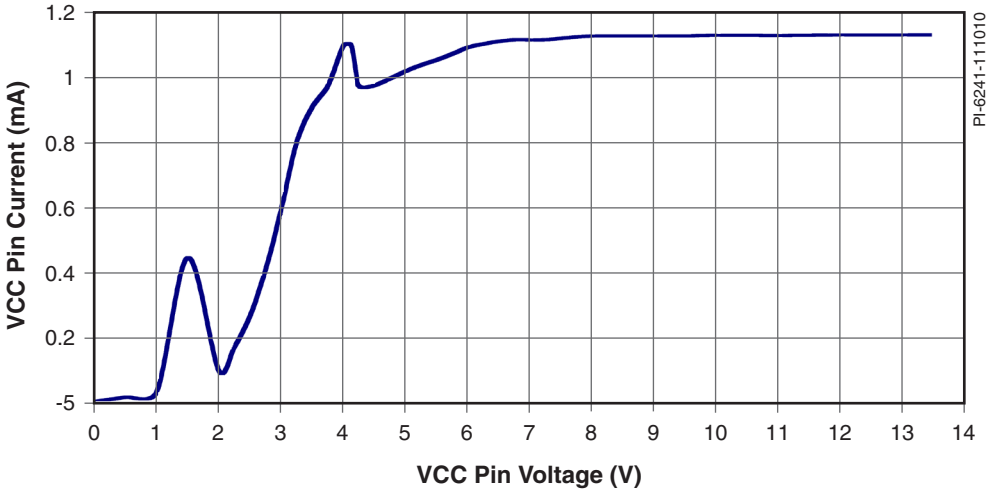
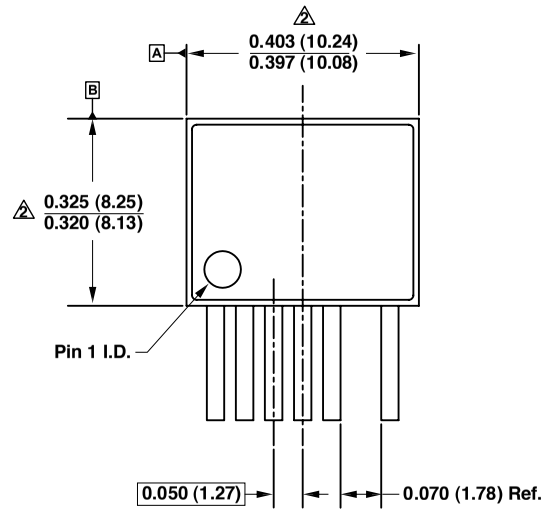
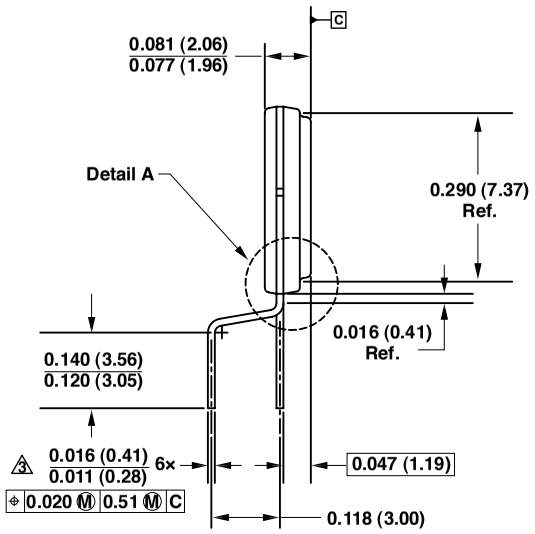


Figure 23. Typical Characteristic: VCC Pin Current vs. Voltage (Device not Switching).

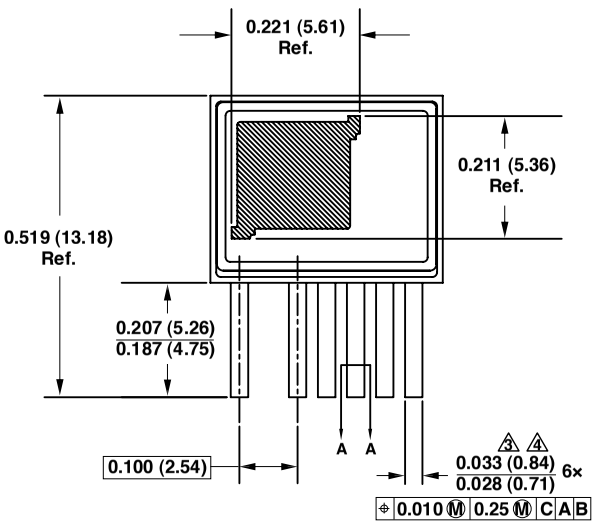
eSIP-7G (E Package)



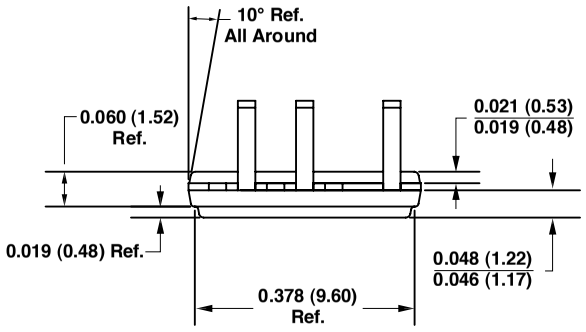
FRONT VIEW



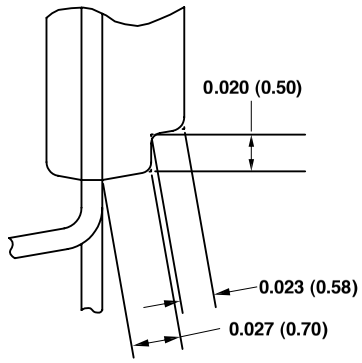
SIDE VIEW



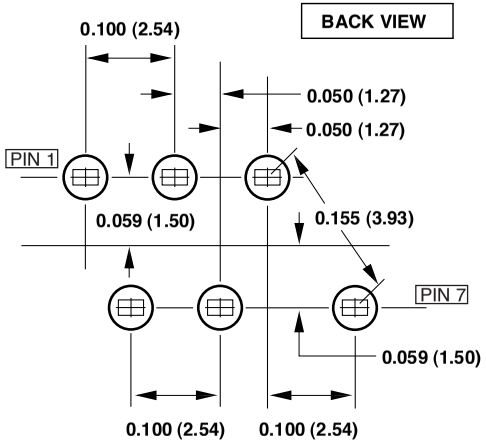
BACK VIEW



END VIEW



Detail A



MOUNTING HOLE PATTERN (not to scale)

Notes:

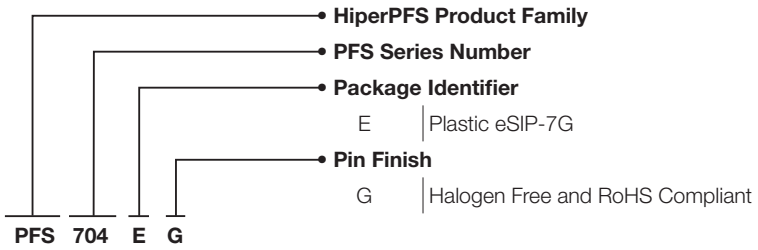
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 (0.18) per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-5711-110810

Part Ordering Information

Part Number	Option	Quantity
PFS704EG	Tube	48
PFS706EG	Tube	48
PFS708EG	Tube	48
PFS710EG	Tube	48
PFS712EG	Tube	48
PFS714EG	Tube	48
PFS716EG	Tube	48
PFS723EG	Tube	48
PFS724EG	Tube	48
PFS725EG	Tube	48
PFS726EG	Tube	48
PFS727EG	Tube	48
PFS728EG	Tube	48
PFS729EG	Tube	48

Part Marking Information



Revision	Notes	Date
A	Initial Release.	11/09/10
B	Updated Figure 9 and deleted sentence on page 7.	02/11
C	Updated FEEDBACK pin voltage rating in Absolute Maximum Rating table.	02/11
D	Updated Inductor Design paragraph on page 12 and BVDSS(TC).	12/11

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