Spartan and Spartan-XL Families Field Programmable Gate Arrays

November 25, 1997 (Version 0.6)

Advance Product Specification

Introduction

The Spartan^{TM} Series is the first high-volume production FPGA solution to deliver all the key requirements for ASIC replacement up to 40,000 gates. These requirements include high performance, on-chip RAM, Core Solutions and prices that, in high volume, approach and in many cases are equivalent to mask programmed ASIC devices.

The Spartan series is the result of more than thirteen years of FPGA design experience and feedback from thousands of customers. By streamlining the Spartan feature set, leveraging advanced hybrid process technologies and focusing on total cost management, the Spartan series delivers the key features required by ASIC and other high volume logic users while avoiding the initial cost, long development cycles and inherent risk of conventional ASICs.

The Spartan Series currently has 10 members, as shown in Table 1.

Spartan Series Features

Note: The Spartan series devices described in this data sheet include the Spartan^{TM} family of devices and the Spartan-XL^{TM} family of devices.

- Next generation ASIC replacement technology
  - First ASIC replacement FPGA for high-volume production with on-chip RAM
  - Advanced Ultradense^{TM} 0.35µm/0.50µm process
  - Density up to 1862 logic cells or 40,000 system gates
  - Streamlined feature set based on XC4000 architecture
  - System performance beyond 80 MHz
  - Broad set of AllianceCORE^{TM} and LogiCORE^{TM} solutions available
  - Unlimited reprogrammability
- System level features
  - Available in both 5.0 Volt and 3.3 Volt versions
  - On-chip Select-RAM™ memory
  - Fully PCI compliant
  - Low power segmented routing architecture
  - Full readback capability for program verification and internal node observability
  - Dedicated high-speed carry logic
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
  - IEEE 1149.1-compatible boundary scan logic support
- Versatile I/O and packaging
  - Low cost plastic packages available in all densities
  - Footprint compatibility in common packages across all Spartan and Spartan-XL devices
  - Individually programmable output slew-rate control maximizes performance and reduces noise
  - Hold time of 0.0 ns for input registers simplifies system timing
  - 12-mA sink current per output
- Fully supported by powerful Xilinx development system
  - Foundation series: Fully integrated, shrink-wrap software
  - Alliance series: Over 100 PC and engineering workstation 3RD party development systems supported
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization

Table 1: Spartan and Spartan-XL Series Field Programmable Gate Arrays

Device	Logic Cells	Max System Gates	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O
XCS05 & XCS05XL	238	5,000	2,000 - 5,000	10 x 10	100	360	80
XCS10 & XCS10XL	466	10,000	3,000 - 10,000	14 x 14	196	616	112
XCS20 & XCS20XL	950	20,000	7,000 - 20,000	20 x 20	400	1,120	160
XCS30 & XCS30XL	1368	30,000	10,000 - 30,000	24 x 24	576	1,536	192
XCS40 & XCS40XL	1862	40,000	13,000 - 40,000	28 x 28	784	2,016	224

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

General Overview

Spartan Series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in Figure 1. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

Spartan Series devices achieve high-performance, low-cost operation through the use of an advanced architecture and semiconductor technology. Spartan and Spartan-XL provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In contrast to other FPGA devices, Spartan offers the most cost-effective solution while maintaining leading-edge performance. In addition to the conventional benefit of high volume programmable logic solutions Spartan also offers on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan Series leverages the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XL and XC4000XV process developments.

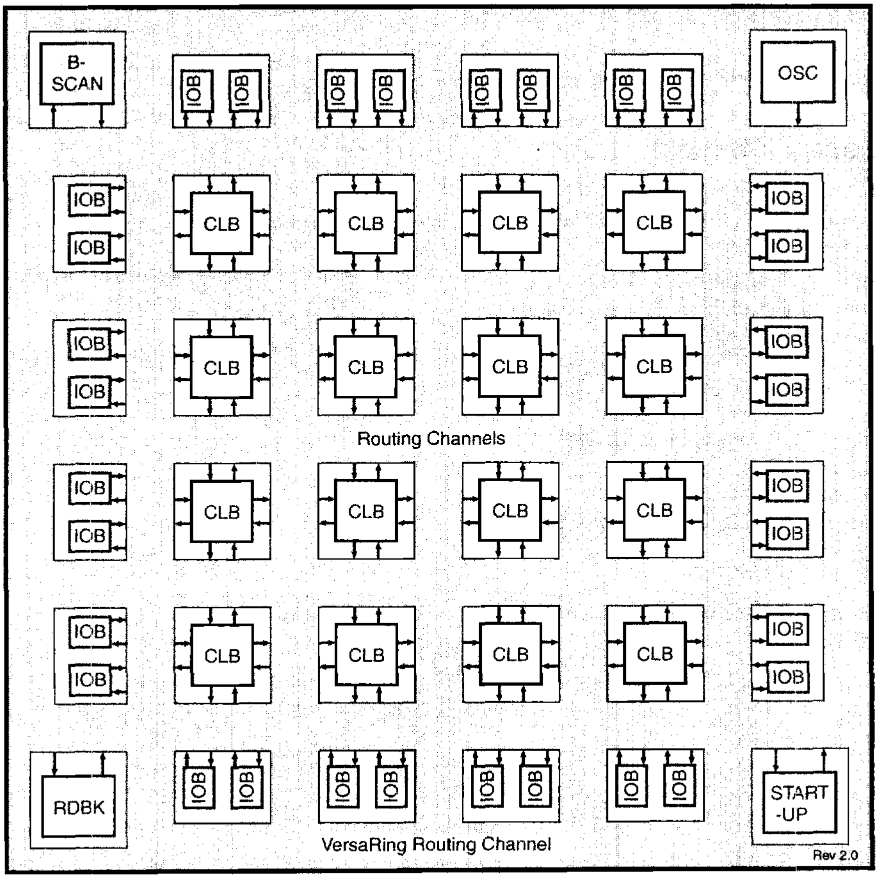

Figure 1: Basic FPGA Block Diagram

Logic Functional Description

The Spartan Series uses a standard FPGA structure as shown in Figure 1. The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in Figure 2. There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the "Advanced Features Description" on page 4-183.

Function Generators

Two 16x1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of Figure 2). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

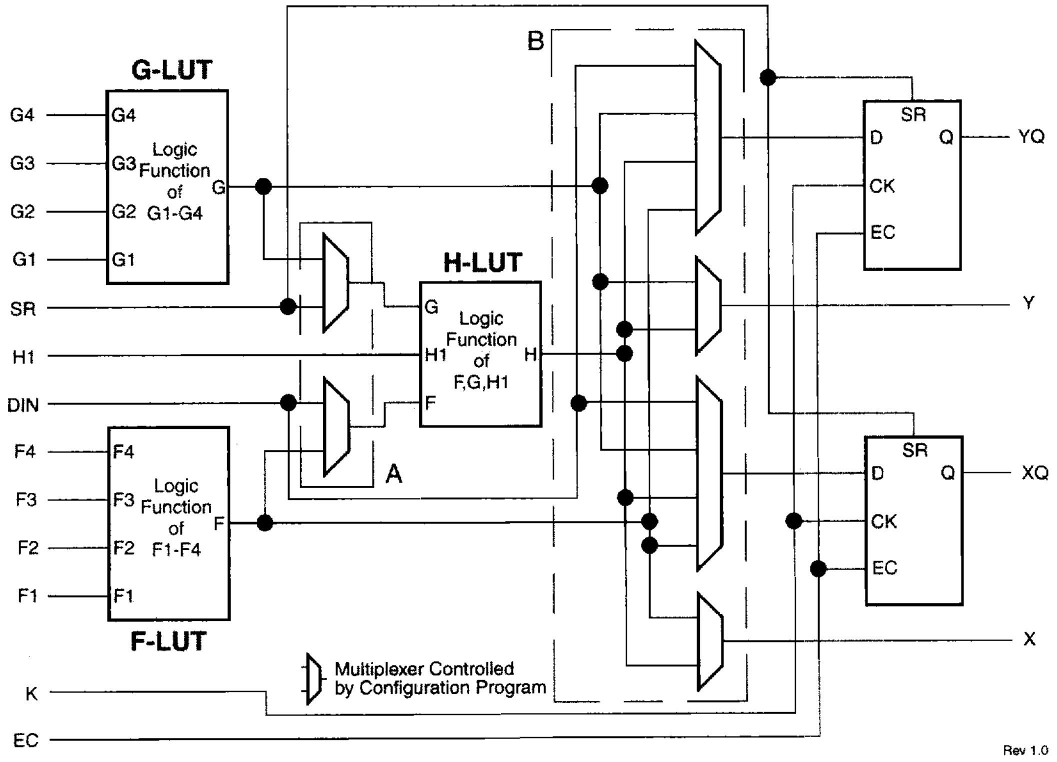

Figure 2: Spartan Simplified CLB Logic Diagram (some features not shown)

A CLB can be used to implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in "Global Signals: GSR and GTS" on page 4-189.

Functionality of the flip-flop is described in Table 2.

Table 2: CLB Flip-Flop Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
	_/‾	1*	0*	D	D
	0	X	0*	X	Q
	X	0	0*	X	Q

Legend:

X	Don't care
_/‾	Rising edge (clock not inverted)
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

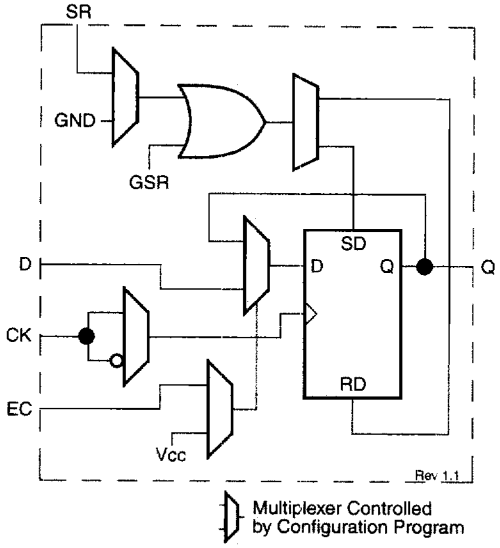

Figure 3: CLB Flip-Flop Functional Block Diagram

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinatorial CLB outputs (X and Y).

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1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinatorial output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1 - C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

The four internal control signals are:

- EC - Enable Clock
- SR - Asynchronous Set/Reset or H function generator Input
- DIN - Direct In or H function generator Input
- H1 - H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 5 shows a simplified functional block diagram of the Spartan IOB.

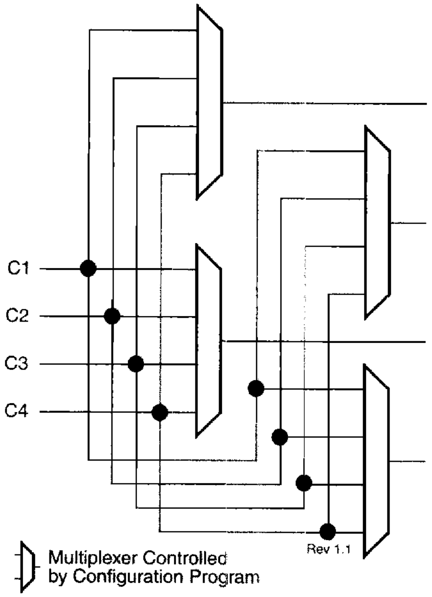


Figure 4: CLB Control Signal Interface

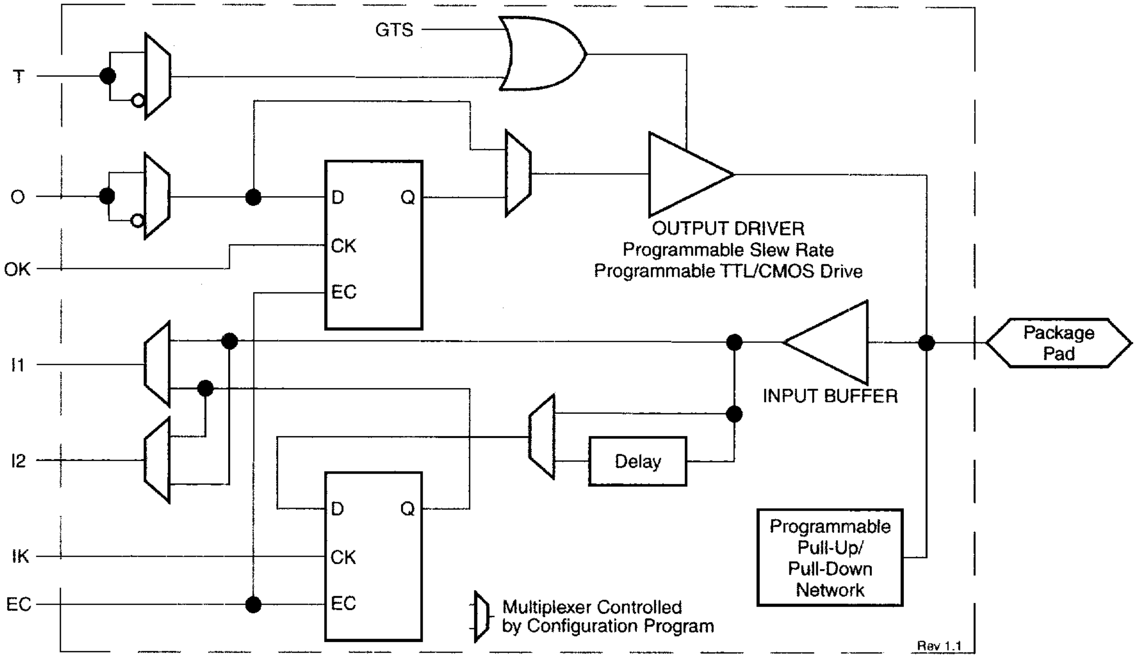


Figure 5: Simplified Spartan IOB Block Diagram

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 5) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 6.

Table 3: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	_/‾	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care
_/‾	Rising edge (clock not inverted)
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 6 on the CK line.

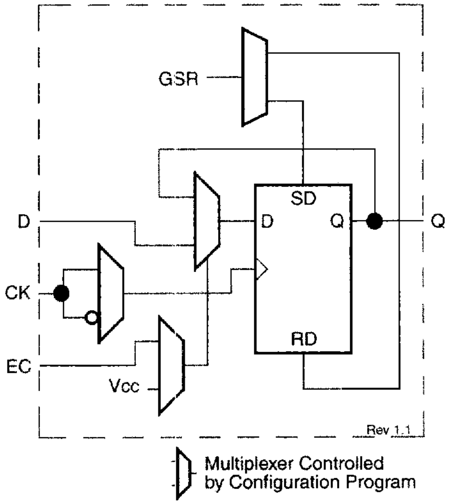


Figure 6: IOB Flip-Flop/Latch Functional Block Diagram

The Spartan IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The added delay guarantees a zero hold time with respect to clocks routed through any of the Spartan global clock buffers. (See "Global Nets and Buffers" on page 4-182 for a description of the global clock buffers in the Spartan Series.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.

The output of the input register goes to the routing channels (via I1 and I2 in Figure 5). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The Spartan input buffers can be globally configured for either TTL (1.2 V) or CMOS (0.5 Vcc) thresholds, using an option in the bitstream generation software. The inputs of Spartan devices can be driven by the outputs of any 3.3 V device, if the Spartan inputs are in TTL mode. There is a slight input hysteresis of about 300 mV. Inputs on the Spartan-XL are TTL compatible and 3.3 V CMOS compatible. The Spartan output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Supported sources for Spartan Series device inputs are shown in Table 4.

Table 4: Supported Sources for Spartan Series Device Inputs

Source	Spartan Inputs		Spartan-XL Inputs
	5.0 V, TTL	5.0 V, CMOS	3.3 V CMOS
Any device, Vcc = 3.3 V, CMOS outputs	√	**Unreliable Data**	√
Spartan Series, Vcc = 5 V, TTL outputs	√		√
Any device, Vcc = 5 V, TTL outputs (Voh ≤ 3.7 V)	√		√
Any device, Vcc = 5 V, CMOS outputs	√	√	√

The I/Os on the Spartan-XL are fully 5 V tolerant even though the Vcc is 3.3 volts. This allows 5 V signals to directly connect to the Spartan-XL inputs without damage, as shown in Table 4. In addition, the 3.3 volt Vcc can be applied before or after 5 volt signals are applied to the I/Os. This makes the Spartan-XL immune to power supply sequencing problems.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 5.

Table 5: Output Flip-Flop Functionality

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	_/‾	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
_/‾	Rising edge (clock not inverted)
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

Output Buffer

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see Figure 5).

By default, a Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to Vcc. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

In a Spartan-XL device, all outputs are configured as CMOS drivers, therefore driving rail-to-rail.

Any Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3 V device. (For a detailed discussion of how to interface between 5.0 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book.*)

Supported destinations for Spartan Series device outputs are shown in Table 6.

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

Table 6: Supported Destinations for Spartan Series Outputs

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3 V, CMOS	5.0 V, TTL	5.0 V, CMOS
Any device, Vcc = 3.3 V, CMOS-threshold inputs	√	√	some[1]
Any device, Vcc = 5.0 V, TTL-threshold inputs	√	√	√
Any device, Vcc = 5 V, CMOS-threshold inputs	**Unreliable Data**		√

1. Only if destination device has 5-V tolerant inputs

Spartan Series devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 kΩ – 100 kΩ (see specifications section). This high value makes them unsuitable as wired-AND pull-up resistors.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (see Figure 6). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (EC), which through configuration, can be activated individually (see EC signal in Figure 6) for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan Series CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

This section describes the routing channels available in Spartan series devices. Figure 7 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the EPIC design editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

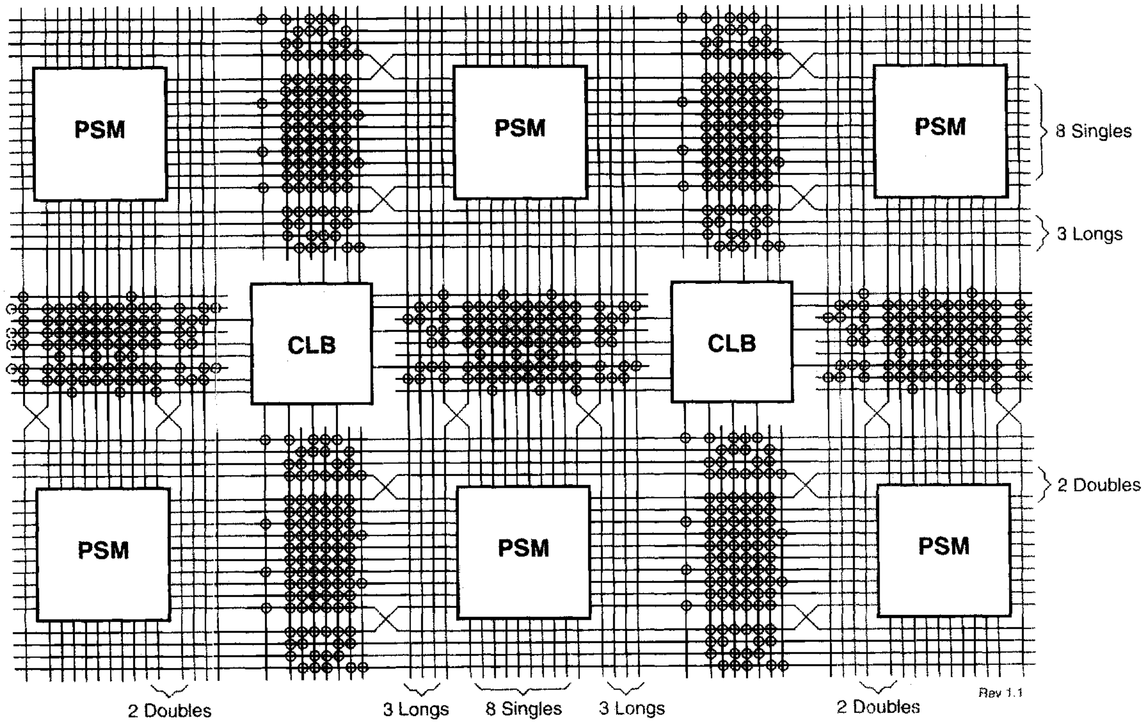


Figure 7: Spartan Series CLB Routing Channels and Interface Block Diagram

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 7 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 8. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as 4 single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.

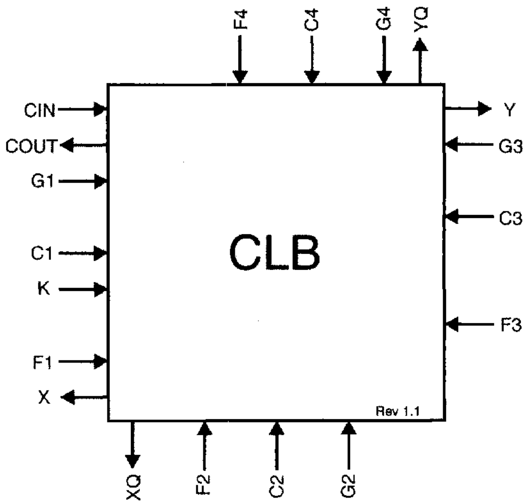


Figure 8: CLB Interconnect Signals

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 9).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs.

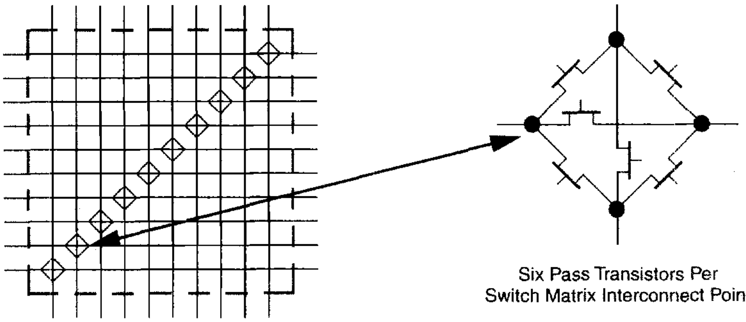


Figure 9: Programmable Switch Matrix

Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 9. Routing connectivity is shown in Figure 7.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 7).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan series longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 7. The longlines also interface to some 3-state buffers which is described later in "3-State Long Line Drivers" on page 4-188.

I/O Routing

Spartan series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan series devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 10. The clock pins of every CLB and IOB can also be sourced from local interconnect.

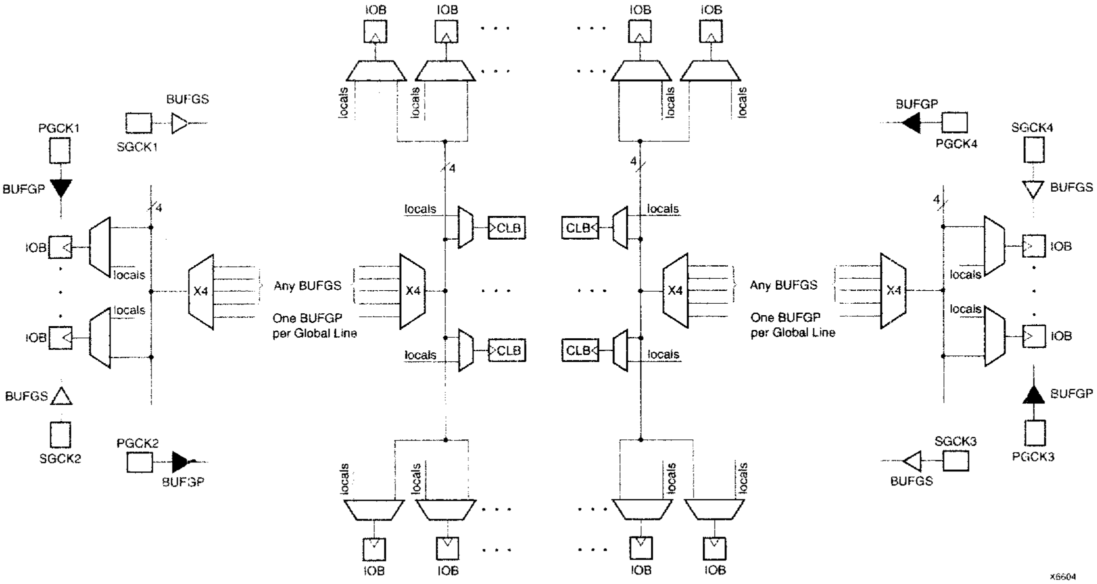


Figure 10: Spartan Series Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the Single-Port Mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2 or 32 x 1 RAM array. In the Dual-Port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 7. Any of these possibilities can be individually programmed into a Spartan Series CLB.

- The 16 x 1 Single-Port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 Single-Port configuration combines two 16 x 1 Single Port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 Single-Port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The Dual Port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

Table 7: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√		

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 Single-Port, the (16 x 1) x 2 Single-Port and the 16 x 1 Dual-Port configurations each use one entire CLB, the 16 x 1 Single-Port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the Dual-Port RAM can transfer twice as much data as the Single-Port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

Single-Port Mode

There are three CLB memory configurations for the Single-Port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in Figure 11.

The Single-Port RAM signals and the CLB signals (Figure 2 on page 4-175) from which they are originally derived are shown in Table 8.

Table 8: Single-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN or H_1
A[3:0]	Address	F_1-F_4 or G_1-G_4
A_4 (32 x 1 only)	Address	H_1
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (Data Out)	F_{OUT} or G_{OUT}

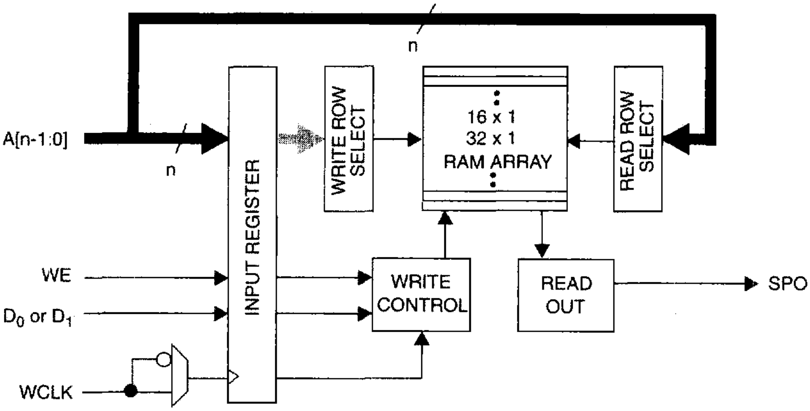


Figure 11: Logic Diagram for the Single-Port RAM

NOTE: 1. The (16 x 1) x 2 configuration combines two 16 x 1 Single Port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration

Writing data to the Single-Port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 12. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

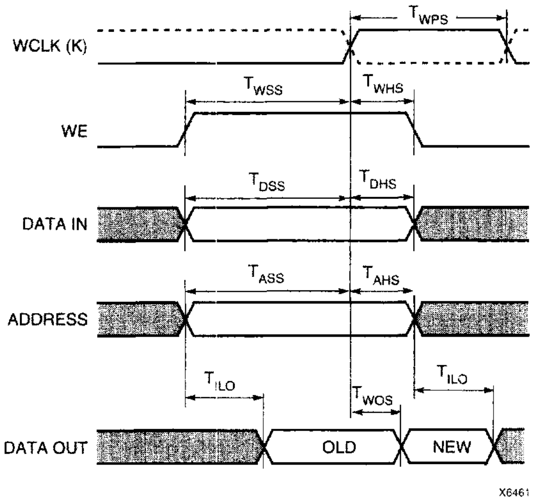


Figure 12: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM's SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active-High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO}, the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS}, the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 Dual-Port memory. Of the two data ports available, one permits read and write operations at the address specified by A[3:0] while the second provides only for read operations at the address specified independently by DPRA[3:0]. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 Dual-Port RAM is shown in Figure 13.

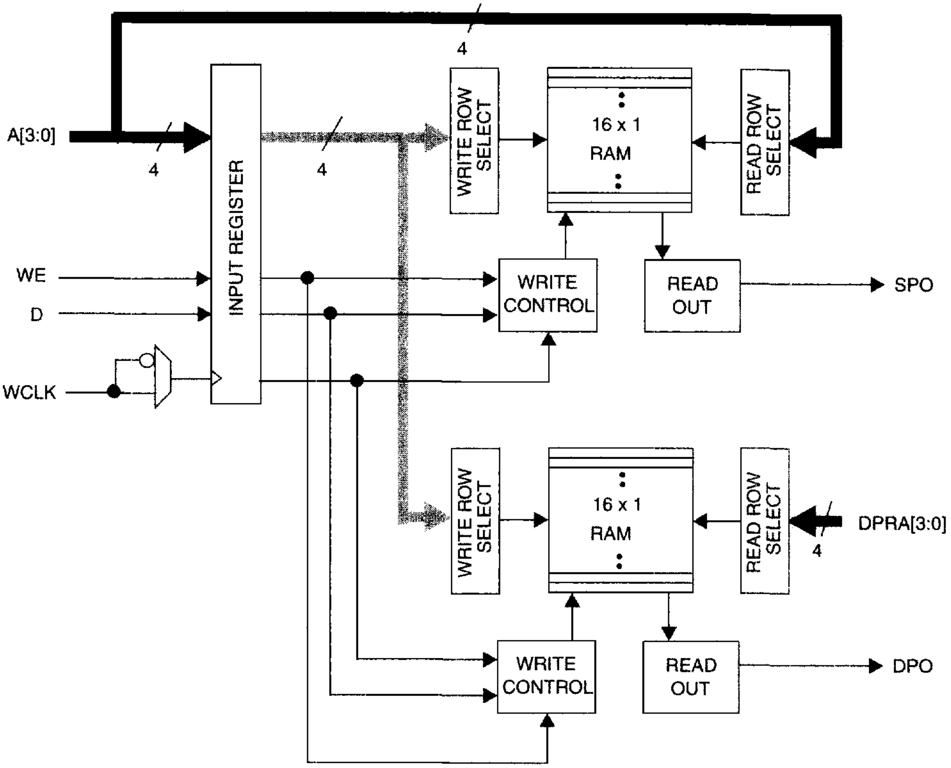


Figure 13: Logic Diagram for the Dual-Port RAM

The Dual-Port RAM signals and the CLB signals from which they are originally derived are shown in Table 9.

Table 9: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F_1-F_4
DPRA[3:0]	Read Address for Dual-Port	G_1-G_4
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the Dual-Port consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 Single-Port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the Dual-Port RAM can provide twice the effective data throughput of a Single-Port RAM alternating read and write operations.

The timing relationships for the Dual-Port RAM mode are shown in Figure 12.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations of the Spartan series are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the schematic library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on using RAM inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "*Xilinx Edge-Triggered and Dual-Port RAM Capability*," "*Implementing FIFOs in Xilinx RAM*," and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both the Spartan and the Spartan-XL series.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources.

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan series, speeding up arithmetic and counting functions.

The carry chain in Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. (See Figure 14.)

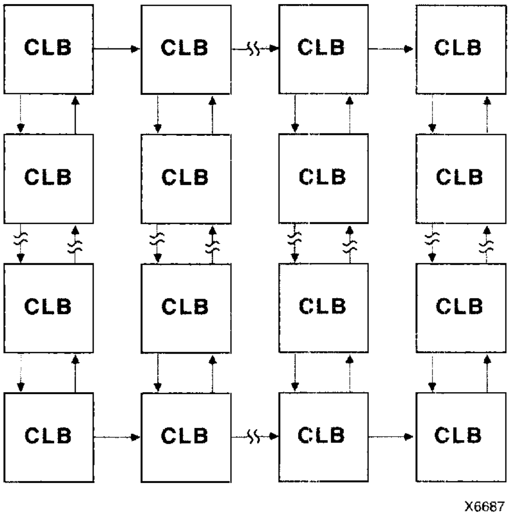


Figure 14: Available Spartan Carry Propagation Paths

Figure 15 on page 4-187 shows a Spartan series CLB with dedicated fast carry logic. The carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 16 on page 4-188 shows the details of the carry logic for the Spartan. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 15.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

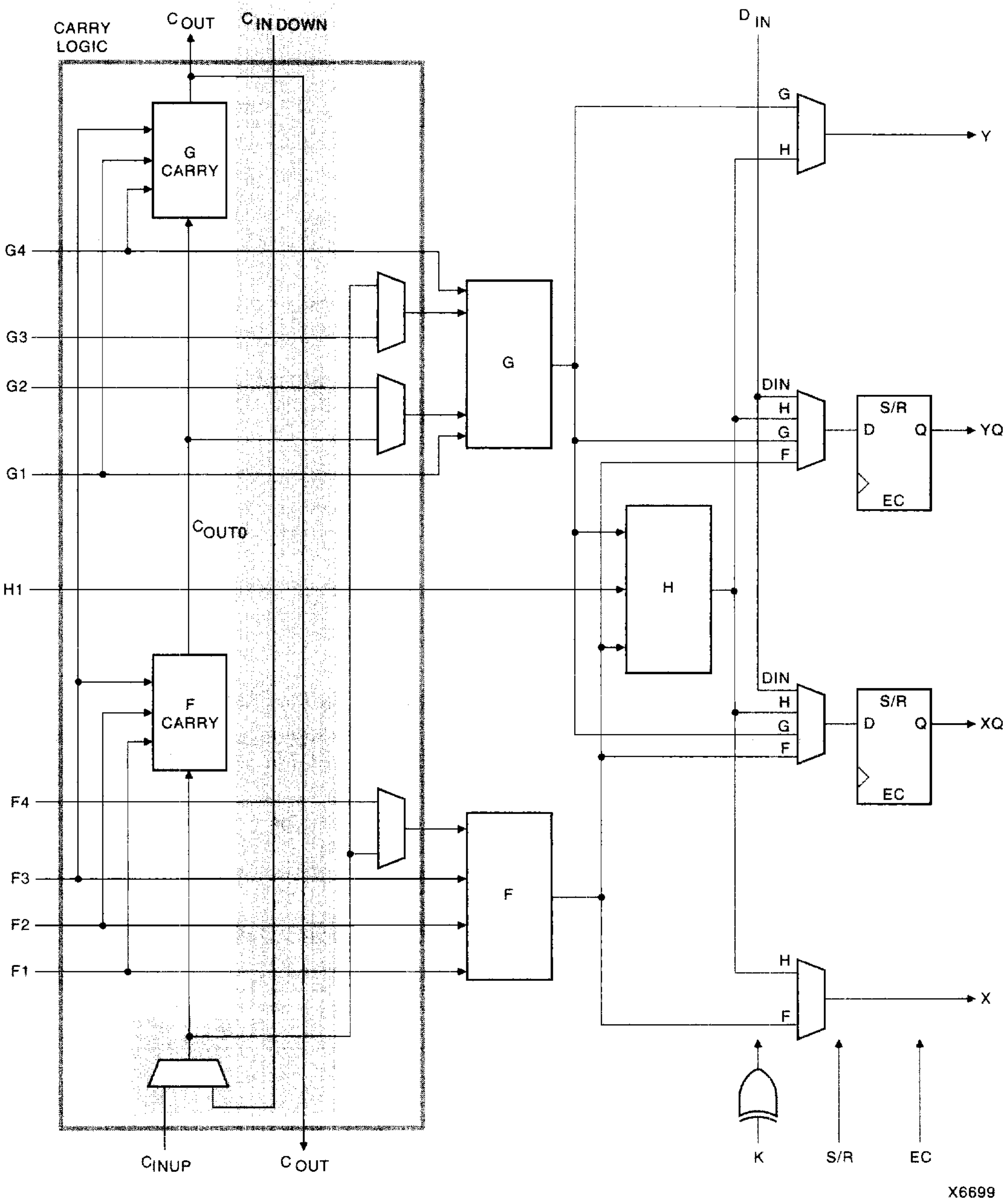


Figure 15: Fast Carry Logic in Spartan CLB

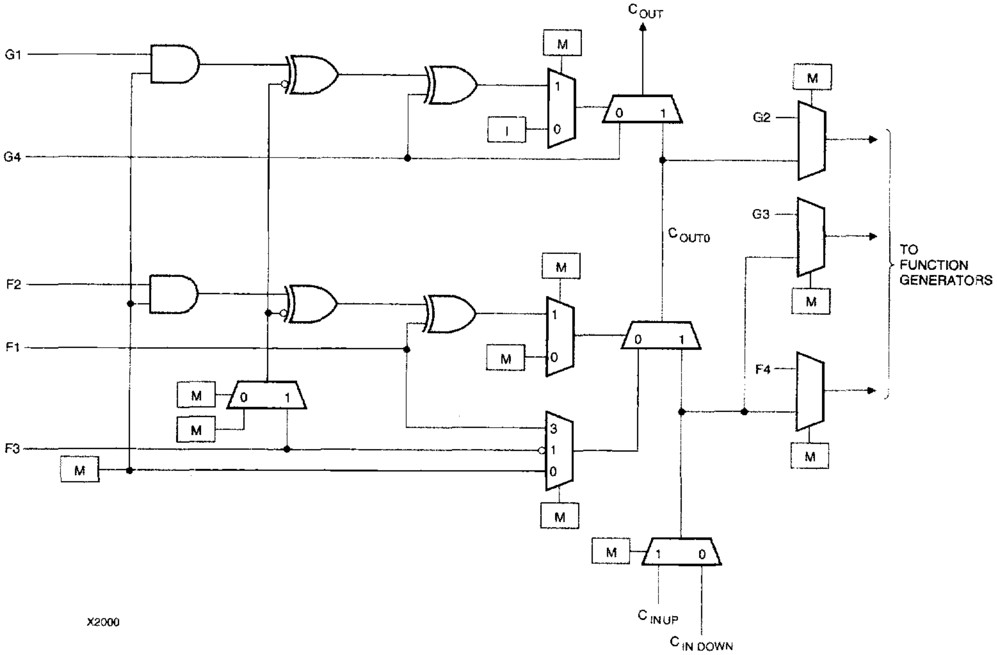


Figure 16: Detail of Spartan Dedicated Carry Logic

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 10.

Three-State Buffer Examples

Figure 17 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in Table 10.

Table 10: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

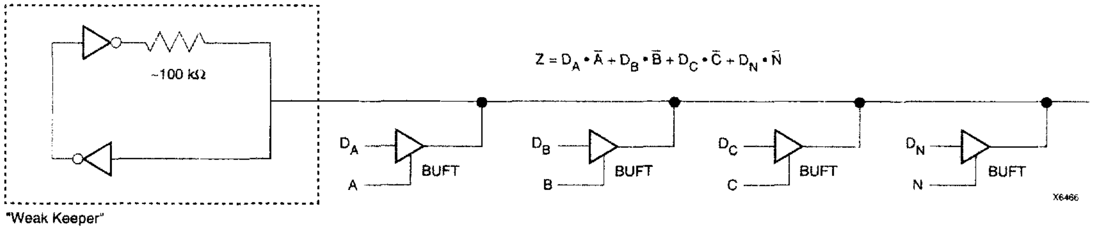


Figure 17: 3-State Buffers Implement a Multiplexer

On-Chip Oscillator

Spartan series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3 on page 4-176 for the CLB and Figure 6 on page 4-178 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

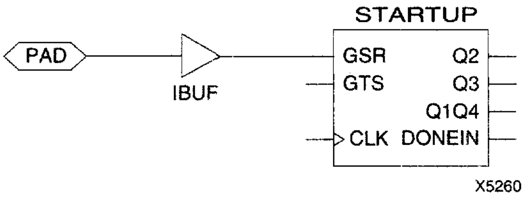


Figure 18: Schematic Symbols for Global Set/Reset

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 18.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-State line (GTS) as shown in Figure 5 on page 4-177 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 18 for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Alternatively, GTS can be driven from any internal node.

Boundary Scan

The 'bed of nails' has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan Series implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices.*"

Figure 19 on page 4-190 is a diagram of the Spartan Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan Series devices can also be configured through the boundary scan logic. See "Configuration Through the Boundary Scan Pins" on page 4-197.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 11.

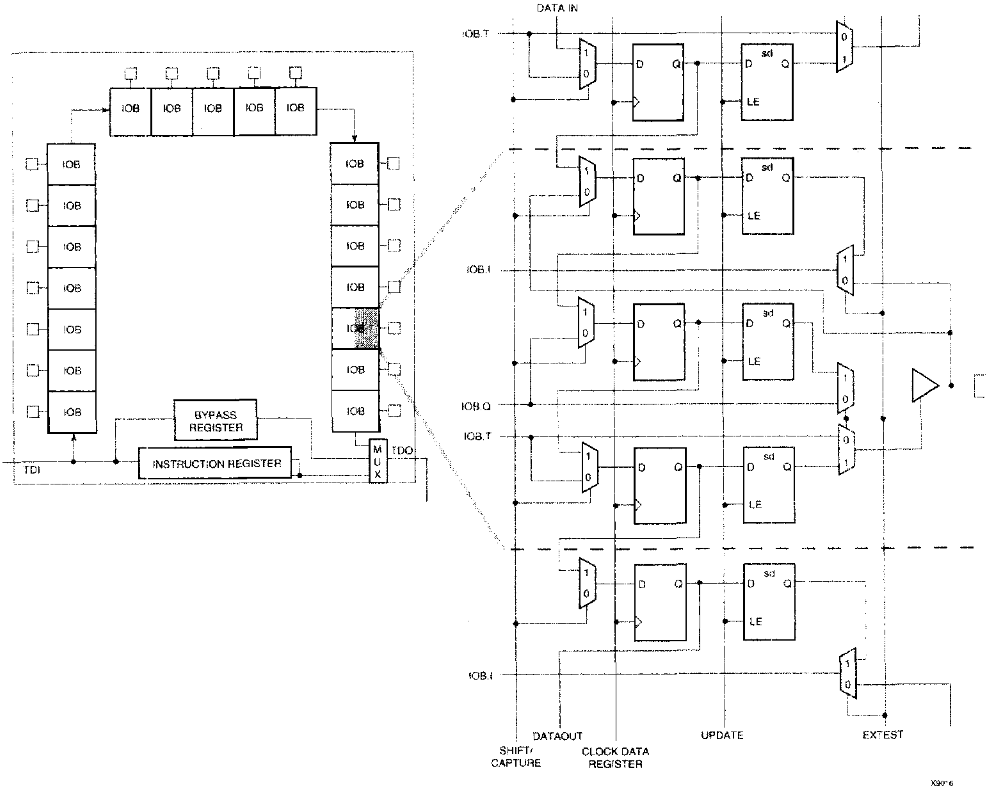


Figure 19: Spartan Series Boundary Scan Logic

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 20. The device-specific pinout tables for the Spartan Series include the boundary scan locations for each IOB pin.

BSDL (Boundary Scan Description Language) files for Spartan Series devices are available on the Xilinx FTP site.

Including Boundary Scan in a Schematic

If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 21.

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Table 11: Boundary Scan Instructions

Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	BYPASS	Bypass Register	—

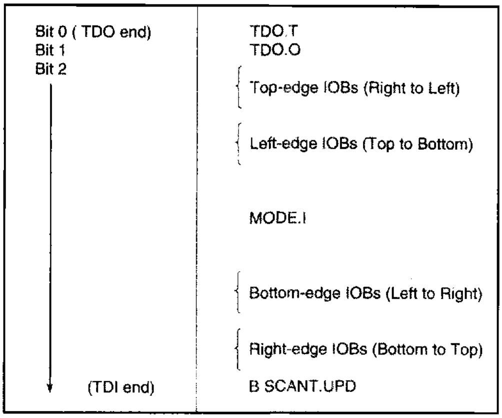


Figure 20: Boundary Scan Bit Sequence

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—don't toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "*Boundary Scan in FPGA Devices.*"

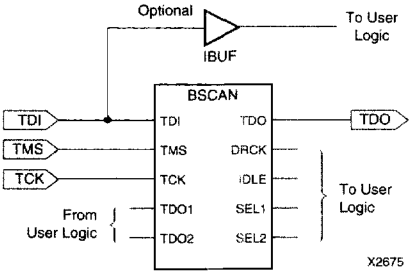


Figure 21: Boundary Scan Schematic Example

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

Spartan series devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

The control pin (MODE) is sampled prior to starting configuration to determine the configuration mode. After configuration, this pin is unused. The MODE pin has a weak pull-up resistor turned on during configuration. With MODE High, Slave Serial mode is selected, which is the most popular configuration mode used primarily for daisy-chained devices. Therefore, for the most common configuration mode, the MODE pin can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) If the Master Serial mode is desired, an external pull-down resistor value of 4.7 kΩ, connected to the MODE pin, is recommended.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 12 on page 4-192.

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 22.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Devices such as XC3000A and XC3100A do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

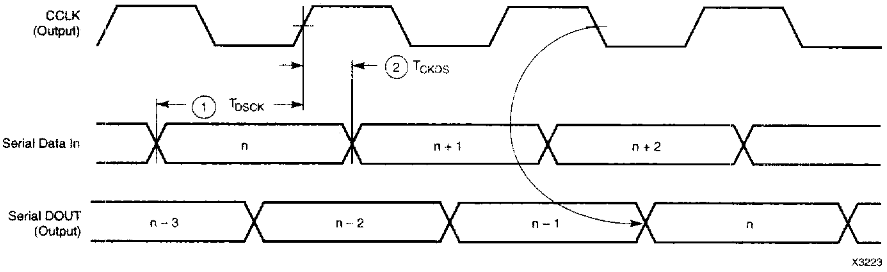
Figure 23 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.

Master Serial mode is selected by a Low on the MODE pin.

Table 12: Pin Functions During Configuration

CONFIGURATION MODE <MODE Pin>		
SLAVE SERIAL <High>	MASTER SERIAL <Low>	USER OPERATION
MODE (I)	MODE (I)	MODE
HDC (HIGH)	HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DSCK}	20		ns
	DIN hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 22: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 23 shows a full master/slave system. A Spartan series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a high on the MODE pin. Slave Serial is the default mode if the MODE pin is left unconnected, as it has a weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 23 on page 4-194. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

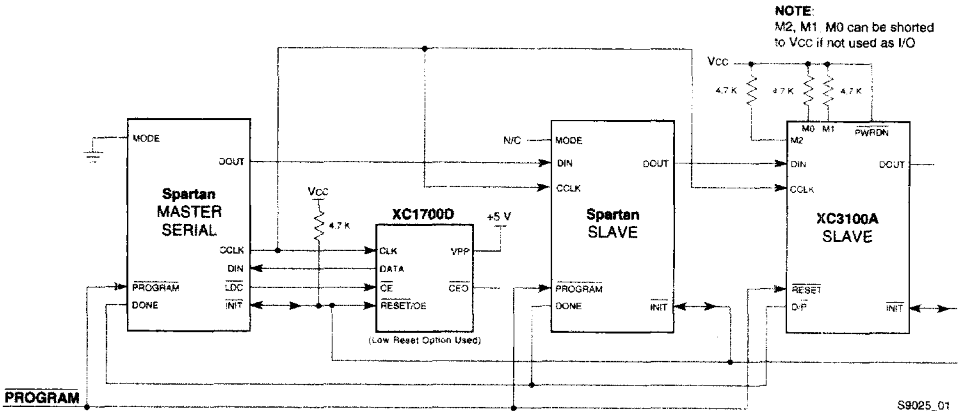
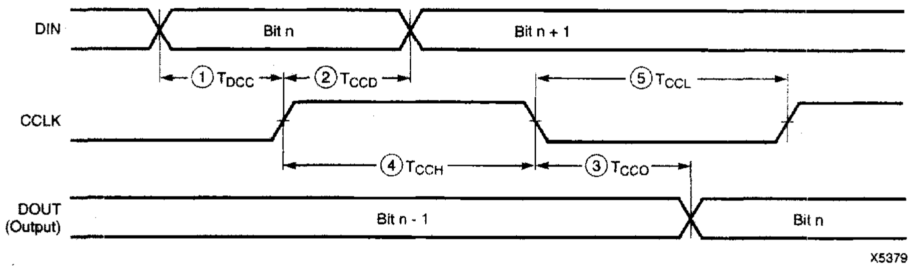


Figure 23: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Figure 24: Slave Serial Mode Programming Switching Characteristics

Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan series devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan series devices. The frequency is selected by an option when running the bitstream generation software. Slow mode is the default.

Data Stream Format

The data stream ("bitstream") format is identical for both configuration modes. The data stream format is shown in Table 13. Bit-serial data is read from left to right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones. This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 14). Each frame begins with a start field and ends with an error check. A postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

Table 13: Spartan Series Data Stream Formats

Data Type	
Fill Byte	11111111b
Preamble Code	0010b
Length Count	COUNT(23:0)
Fill Bits	1111b
Start Field	0b
Data Frame	DATA(n-1:0)
CRC or Constant Field Check	xxxx (CRC) or 0110b
Extend Write Cycle	—
Postamble	01111111b
Start-Up Bytes	xxh

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master serial mode, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 13. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

Table 14: Spartan Program Data

Device	XCS05/XL	XCS10/XL	XCS20/XL	XCS30/XL	XCS40/XL
Max System Gates	5,000	10,000	20,000	30,000	40,000
CLBs (Row x Col.)	100 (10 x 10)	196 (14 x 14)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)
IOBs	80	112	160	192	224
Flip-Flops	360	616	1,120	1,536	2,016
Horizontal Longlines	20	28	40	48	56
TBUFs per Longline	12	16	22	26	30
Bits per Frame	126	166	226	266	306
Frames	428	572	788	932	1,076
Program Data	53,936	94,960	178,096	247,920	329,264
PROM Size (bits)	53,984	95,008	178,144	247,968	329,312

Notes: 1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40 (header) + 8

2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 25. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

Configuration Sequence

There are four major steps in the Spartan Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 26.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms, and up to 10% longer in the Spartan-XL devices. The delay is four times as long when in Master Serial Mode (MODE is Low), to allow ample time for all slaves to reach a stable Vcc. When all $\overline{\text{INIT}}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{\text{PROGRAM}}$ pin

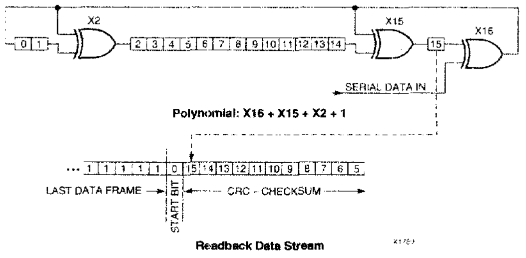


Figure 25: Circuit for Generating CRC-16

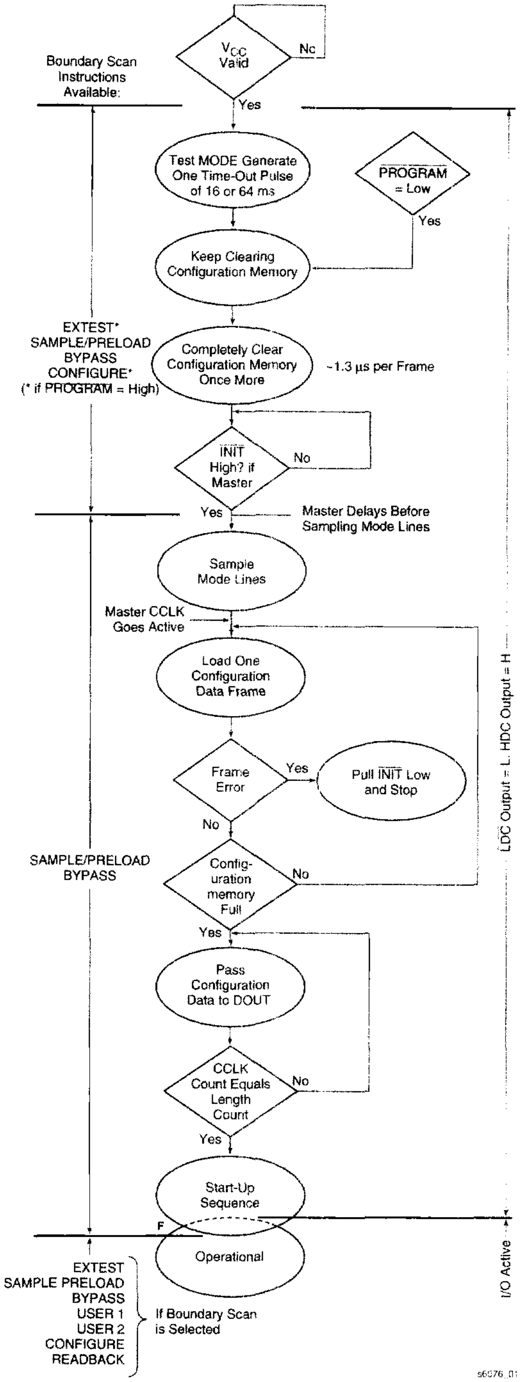


Figure 26: Power-up Configuration Sequence

Low. During this time delay, or as long as the $\overline{\text{PROGRAM}}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{\text{PROGRAM}}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{\text{INIT}}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE provide status outputs for the system interface. The outputs $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{\text{INIT}}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive $\overline{\text{INIT}}$. Two internal clocks after the $\overline{\text{INIT}}$ pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 26 on page 4-196.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The Spartan Series $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing the state of the MODE pin, and is ready to start the configuration process. A master device waits up to an additional 300 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

Configuration Through the Boundary Scan Pins

Spartan Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note also applies to Spartan and Spartan-XL devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

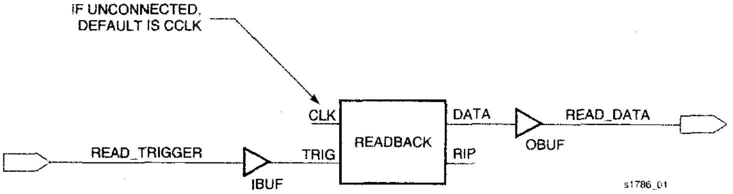


Figure 27: Readback Schematic Example

Spartan Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 27.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in Figure 28.

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in Figure 28.

Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

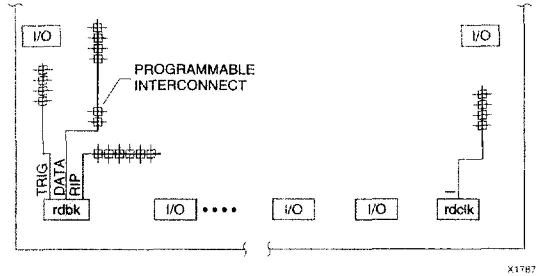


Figure 28: READBACK Symbol in Graphical Editor

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 13 and Table 14.

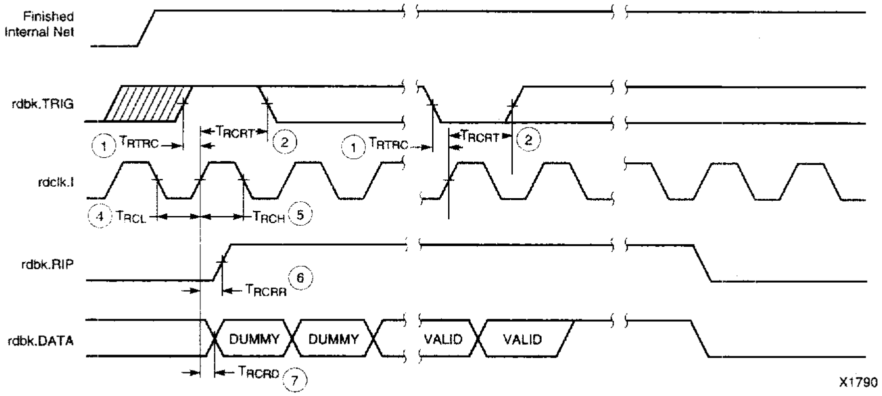
Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

Spartan Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



Spartan and Spartan-XL

	Description	Symbol		Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1	T_{RTRC}	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2	T_{RCRT}	50	-	ns
rdclk.1	rdbk.DATA delay	7	T_{RCRD}	-	250	ns
	rdbk.RIP delay	6	T_{RCRR}	-	250	ns
	High time	5	T_{RCH}	250	500	ns
	Low time	4	T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.
Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Spartan Detailed Specification

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance:	Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary:	Based on preliminary characterization. Further changes are not expected.
Unmarked:	Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

Spartan Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Spartan Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Note: At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output Measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

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[1] Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Spartan DC Characteristics Over Operating Conditions

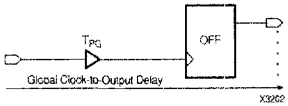
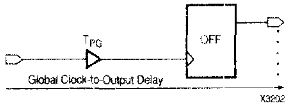
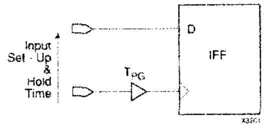
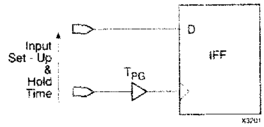
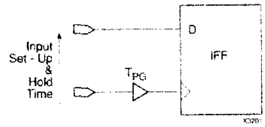
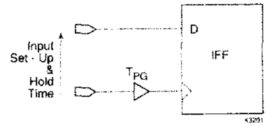
Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
I_L	Input or output leakage current		-10	+10	μA
C_{IN}	Input capacitance (sample tested)	PC, VQ, TQ, PQ, BG packages		10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		-0.02	-0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02		mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.

Note 2: With no output current loads, no active input pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with the Tie option.

Spartan Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all Spartan devices unless otherwise noted.

	Speed Grade		-3	-4	Units
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF}	XCS05	8.7	6.0	ns
		XCS10	9.1	6.4	ns
		XCS20	9.3	7.0	ns
		XCS30	9.4	7.4	ns
	(Max)	XCS40	10.2	7.6	
Global Clock to Output (slew-limited) using OFF 	T_{ICKO}	XCS05	11.5	8.0	ns
		XCS10	12.0	8.4	ns
		XCS20	12.2	9.0	ns
		XCS30	12.8	9.4	ns
	(Max)	XCS40	12.8	9.6	
Input Setup Time, using IFF (no delay) 	T_{PSUF}	XCS05	2.3	1.7	ns
		XCS10	1.2	1.0	ns
		XCS20	0.2	0	ns
		XCS30	0	0	ns
	(Min)	XCS40	0	0	
Input Hold Time, using IFF (no delay) 	T_{PHF}	XCS05	4.0	1.7	ns
		XCS10	4.5	2.2	ns
		XCS20	5.5	2.7	ns
		XCS30	5.5	3.2	ns
	(Min)	XCS40	5.7	3.7	
Input Setup Time, using IFF (with delay) 	T_{PSU}	XCS05	6.0	5.2	ns
		XCS10	6.0	5.2	ns
		XCS20	6.0	5.2	ns
		XCS30	6.0	5.2	ns
	(Min)	XCS40	6.8	5.2	
Input Hold Time, using IFF (with delay) 	T_{PH}	XCS05	0	0	ns
		XCS10	0	0	ns
		XCS20	0	0	ns
		XCS30	0	0	ns
	(Min)	XCS40	0	0	

OFF = Output Flip-Flop IFF = Input Flip-Flop/Latch

Advance

Spartan-XL Detailed Specification

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

Spartan-XL Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes: 1. Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Spartan-XL Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~40% of V_{CC}.

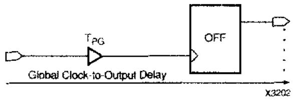
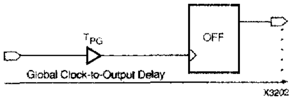
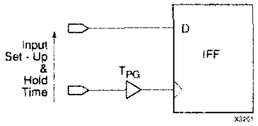
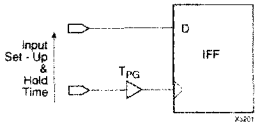
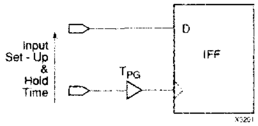
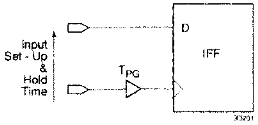
Spartan-XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			5	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PC, VQ, TQ, PQ, BG packages		10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.3V (sample tested)		0.02		mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with the Tie option.

Spartan-XL Guaranteed Input and Output Parameters (Pin-to-Pin)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all Spartan-XL devices unless otherwise noted.

		Speed Grade	-3	-4	Units
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XCS05XL	8.7	6.0	ns
		XCS10XL	9.1	6.4	ns
		XCS20XL	9.3	7.0	ns
		XCS30XL	9.4	7.4	ns
		XCS40XL	10.2	7.6	ns
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XCS05XL	11.5	8.0	ns
		XCS10XL	12.0	8.4	ns
		XCS20XL	12.2	9.0	ns
		XCS30XL	12.8	9.4	ns
		XCS40XL	12.8	9.6	ns
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XCS05XL	2.3	1.7	ns
		XCS10XL	1.2	1.0	ns
		XCS20XL	0.2	0	ns
		XCS30XL	0	0	ns
		XCS40XL	0	0	ns
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XCS05XL	4.0	1.7	ns
		XCS10XL	4.5	2.2	ns
		XCS20XL	5.5	2.7	ns
		XCS30XL	5.5	3.2	ns
		XCS40XL	5.7	3.7	ns
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XCS05XL	6.0	5.2	ns
		XCS10XL	6.0	5.2	ns
		XCS20XL	6.0	5.2	ns
		XCS30XL	6.0	5.2	ns
		XCS40XL	6.8	5.2	ns
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XCS05XL	0	0	ns
		XCS10XL	0	0	ns
		XCS20XL	0	0	ns
		XCS30XL	0	0	ns
		XCS40XL	0	0	ns
			Advance		

OFF = Output Flip-Flop IFF = Input Flip-Flop/Latch

Pin Descriptions

There are three types of pins in the Spartan Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Spartan Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See "Global Signals: GSR and GTS" on page 4-189 for more information on GSR.

Spartan Series devices have no dedicated 3-state pin, they use the global 3-state net, GTS, instead. This net 3-states all outputs. See "Global Signals: GSR and GTS" on page 4-189 for more information on GTS.

Device pins for Spartan Series devices are described in Table 15.

Table 15: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	X	X	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 µF capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan Series devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 4-198 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
MODE	I	I	The Mode input is sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, this pin has a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pin can be left unconnected. A pull-down resistor value of 4.7 kΩ is recommended for Master Serial mode.
Don't Connect	X	X	Pins reserved for factory testing and possible future enhancements. Pins must be left floating.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.

Table 15: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Pin Locations for XCS05 & XCS05XL Devices

XCS05 & XCS05XL Pad Name	PC84	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2	P29	P21	119
Don't Connect	P30	P22	122
GND	P31	P23	-
MODE	P32	P24	125
VCC	P33	P25	-
Don't Connect	P34	P26	126
I/O, PGCK2	P35	P27	127
I/O (HDC)	P36	P28	130
I/O	-	P29	133
I/O ($\overline{\text{LDC}}$)	P37	P30	136
I/O	P38	P31	139
I/O	P39	P32	142
I/O	-	P33	145
I/O	-	P34	148
I/O	P40	P35	151
I/O ($\overline{\text{INIT}}$)	P41	P36	154
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157
I/O	P45	P40	160
I/O	-	P41	163
I/O	-	P42	166
I/O	P46	P43	169
I/O	P47	P44	172
I/O	P48	P45	175
I/O	P49	P46	178
I/O	P50	P47	181
I/O, SGCK3	P51	P48	184
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
$\overline{\text{PROGRAM}}$	P55	P52	-
I/O	P56	P53	187
I/O, PGCK3	P57	P54	190
I/O	P58	P55	193
I/O	-	P56	196
I/O	P59	P57	199
I/O	P60	P58	202
I/O	-	P59	205
I/O	-	P60	208
I/O	P61	P61	211
I/O	P62	P62	214
VCC	P63	P63	-
GND	P64	P64	-
I/O	P65	P65	217
I/O	P66	P66	220
I/O	-	P67	223
I/O	P67	P68	229
I/O	P68	P69	232
I/O	P69	P70	235
I/O	P70	P71	238
I/O (DIN)	P71	P72	241
I/O, SGCK4 (DOUT)	P72	P73	244
CCLK	P73	P74	-
VCC	P74	P75	-
O, TDO	P75	P76	0
GND	P76	P77	-
I/O	P77	P78	2
I/O, PGCK4	P78	P79	5
I/O	P79	P80	8
I/O	P80	P81	11
I/O	P81	P82	14
I/O	P82	P83	17
I/O	-	P84	20
I/O	-	P85	23
I/O	P83	P86	26

XCS05 & XCS05XL Pad Name	PC84	VQ100	Bndry Scan
I/O	P84	P87	29
GND	P1	P88	-

9/24/97

Pin Locations for XCS10 & XCS10XL Devices

XCS10 & XCS10XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
VCC	P2	P89	P128	-
I/O	P3	P90	P129	44
I/O	P4	P91	P130	47
I/O	-	P92	P131	50
I/O	-	P93	P132	53
I/O	P5	P94	P133	56
I/O	P6	P95	P134	59
I/O	-	-	P135	62
I/O	-	-	P136	65
GND	-	-	P137	-
I/O	P7	P96	P138	68
I/O	P8	P97	P139	71
I/O	-	-	P140	74
I/O	-	-	P141	77
I/O	P9	P98	P142	80
I/O, SGCK1	P10	P99	P143	83
VCC	P11	P100	P144	-
GND	P12	P1	P1	-
I/O, PGCK1	P13	P2	P2	86
I/O	P14	P3	P3	89
I/O	-	-	P4	92
I/O	-	-	P5	95
I/O, TDI	P15	P4	P6	98
I/O, TCK	P16	P5	P7	101
GND	-	-	P8	-
I/O	-	-	P9	104
I/O	-	-	P10	107
I/O, TMS	P17	P6	P11	110
I/O	P18	P7	P12	113
I/O	-	-	P13	116
I/O	-	P8	P14	119
I/O	P19	P9	P15	122
I/O	P20	P10	P16	125
GND	P21	P11	P17	-
VCC	P22	P12	P18	-
I/O	P23	P13	P19	128
I/O	P24	P14	P20	131
I/O	-	P15	P21	134
I/O	-	-	P22	137
I/O	P25	P16	P23	140
I/O	P26	P17	P24	143
I/O	-	-	P25	146
I/O	-	-	P26	149
GND	-	-	P27	-
I/O	P27	P18	P28	152
I/O	-	P19	P29	155
I/O	-	-	P30	158
I/O	-	-	P31	161
I/O	P28	P20	P32	164
I/O, SGCK2	P29	P21	P33	167
Don't Connect	P30	P22	P34	170
GND	P31	P23	P35	-
MODE	P32	P24	P36	173
VCC	P33	P25	P37	-
Don't Connect	P34	P26	P38	174
I/O, PGCK2	P35	P27	P39	175
I/O (HDC)	P36	P28	P40	178
I/O	-	-	P41	181
I/O	-	-	P42	184
I/O	-	P29	P43	187
I/O ($\overline{\text{LDC}}$)	P37	P30	P44	190
GND	-	-	P45	-
I/O	-	-	P46	193
I/O	-	-	P47	196
I/O	P38	P31	P48	199
I/O	P39	P32	P49	202
I/O	-	P33	P50	205
I/O	-	P34	P51	208
I/O	P40	P35	P52	211
I/O ($\overline{\text{INIT}}$)	P41	P36	P53	214
VCC	P42	P37	P54	-
GND	P43	P38	P55	-
I/O	P44	P39	P56	217
I/O	P45	P40	P57	220
I/O	-	P41	P58	223
I/O	-	P42	P59	226
I/O	P46	P43	P60	229
I/O	P47	P44	P61	232
I/O	-	-	P62	235
I/O	-	-	P63	238
GND	-	-	P64	-
I/O	P48	P45	P65	241
I/O	P49	P46	P66	244
I/O	-	-	P67	247
I/O	-	-	P68	250
I/O	P50	P47	P69	253
I/O, SGCK3	P51	P48	P70	256
GND	P52	P49	P71	-
DONE	P53	P50	P72	-
VCC	P54	P51	P73	-
$\overline{\text{PROGRAM}}$	P55	P52	P74	-
I/O	P56	P53	P75	259
I/O, PGCK3	P57	P54	P76	262
I/O	-	-	P77	265
I/O	-	-	P78	268
I/O	P58	P55	P79	271

XCS10 & XCS10XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
I/O	-	P56	P80	274
GND	-	-	P81	-
I/O	-	-	P82	277
I/O	-	-	P83	280
I/O	P59	P57	P84	283
I/O	P60	P58	P85	286
I/O	-	P59	P86	289
I/O	-	P60	P87	292
I/O	P61	P61	P88	295
I/O	P62	P62	P89	298
VCC	P63	P63	P90	-
GND	P64	P64	P91	-
I/O	P65	P65	P92	301
I/O	P66	P66	P93	304
I/O	-	P67	P94	307
I/O	-	-	P95	310
I/O	P67	P68	P96	313
I/O	P68	P69	P97	316
I/O	-	-	P98	319
I/O	-	-	P99	322
GND	-	-	P100	-
I/O	P69	P70	P101	325
I/O	P70	P71	P102	328
I/O	-	-	P103	331
I/O	-	-	P104	334
I/O (DIN)	P71	P72	P105	337
I/O, SGCK4 (DOUT)	P72	P73	P106	340

XCS10 & XCS10XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
CCLK	P73	P74	P107	-
VCC	P74	P75	P108	-
O, TDO	P75	P76	P109	0
GND	P76	P77	P110	-
I/O	P77	P78	P111	2
I/O, PGCK4	P78	P79	P112	5
I/O	-	-	P113	8
I/O	-	-	P114	11
I/O	P79	P80	P115	14
I/O	P80	P81	P116	17
GND	-	-	P118	-
I/O	-	-	P119	20
I/O	-	-	P120	23
I/O	P81	P82	P121	26
I/O	P82	P83	P122	29
I/O	-	P84	P123	32
I/O	-	P85	P124	35
I/O	P83	P86	P125	38
I/O	P84	P87	P126	41
GND	P1	P88	P127	-

9/24/97

Additional XCS10/XL Package Pins

TQ144

Not Connected Pins					
P117	-	-	-	-	-

5/5/97

Pin Locations for XCS20 & XCS20XL Devices

XCS20 & XCS20XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
VCC	P89	P128	P183	-
I/O	P90	P129	P184	62
I/O	P91	P130	P185	65
I/O	P92	P131	P186	68
I/O	P93	P132	P187	71
I/O	-	-	P188	74
I/O	-	-	P189	77
I/O	P94	P133	P190	80
I/O	P95	P134	P191	83
VCC	-	-	P192	-
I/O	-	P135	P193	86
I/O	-	P136	P194	89
GND	-	P137	P195	-
I/O	-	-	P196	92
I/O	-	-	P197	95
I/O	-	-	P198	98
I/O	-	-	P199	101
I/O	P96	P138	P200	104
I/O	P97	P139	P201	107
I/O	-	-	P202	110
I/O	-	-	P203	113
I/O	-	P140	P204	110

XCS20 & XCS20XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
I/O	-	P141	P205	113
I/O	P98	P142	P206	116
I/O, SGCK1	P99	P143	P207	119
VCC	P100	P144	P208	-
GND	P1	P1	P1	-
I/O, PGCK1	P2	P2	P2	122
I/O	P3	P3	P3	125
I/O	-	P4	P4	128
I/O	-	P5	P5	131
I/O, TDI	P4	P6	P6	134
I/O, TCK	P5	P7	P7	137
I/O	-	-	P8	140
I/O	-	-	P10	143
I/O	-	-	P11	143
I/O	-	-	P11	146
I/O	-	-	P12	149
GND	-	P8	P13	-
I/O	-	P9	P14	152
I/O	-	P10	P15	155
I/O, TMS	P6	P11	P16	158
I/O	P7	P12	P17	161
VCC	-	-	P18	-

XCS20 & XCS20XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
I/O	-	-	P19	164
I/O	-	-	P20	167
I/O	-	P13	P21	170
I/O	P8	P14	P22	173
I/O	P9	P15	P23	176
I/O	P10	P16	P24	179
GND	P11	P17	P25	-
VCC	P12	P18	P26	-
I/O	P13	P19	P27	182
I/O	P14	P20	P28	185
I/O	P15	P21	P29	188
I/O	-	P22	P30	191
I/O	-	-	P31	194
I/O	-	-	P32	197
VCC	-	-	P33	-
I/O	P16	P23	P34	200
I/O	P17	P24	P35	203
I/O	-	P25	P36	206
I/O	-	P26	P37	209
GND	-	P27	P38	-
I/O	-	-	P39	212
I/O	-	-	P40	215
I/O	-	-	P41	218
I/O	-	-	P42	221
I/O	-	-	P43	221
I/O	P18	P28	P44	224
I/O	P19	P29	P45	227
I/O	-	P30	P46	230
I/O	-	P31	P47	233
I/O	P20	P32	P48	236
I/O, SGCK2	P21	P33	P49	239
Don't Connect	P22	P34	P50	242
GND	P23	P35	P51	-
MODE	P24	P36	P52	245
VCC	P25	P37	P53	-
Don't Connect	P26	P38	P54	246
I/O, PGCK2	P27	P39	P55	247
I/O (HDC)	P28	P40	P56	250
I/O	-	P41	P57	253
I/O	-	P42	P58	256
I/O	P29	P43	P59	259
I/O ($\overline{\text{LDC}}$)	P30	P44	P60	262
I/O	-	-	P61	265
I/O	-	-	P62	265
I/O	-	-	P63	268
I/O	-	-	P64	271
I/O	-	-	P65	274
GND	-	P45	P66	-
I/O	-	P46	P67	277
I/O	-	P47	P68	280
I/O	P31	P48	P69	283
I/O	P32	P49	P70	286
VCC	-	-	P71	-
I/O	-	-	P72	289
I/O	-	-	P73	292
I/O	P33	P50	P74	295

XCS20 & XCS20XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
I/O	P34	P51	P75	298
I/O	P35	P52	P76	301
I/O ($\overline{\text{INIT}}$)	P36	P53	P77	304
VCC	P37	P54	P78	-
GND	P38	P55	P79	-
I/O	P39	P56	P80	307
I/O	P40	P57	P81	310
I/O	P41	P58	P82	313
I/O	P42	P59	P83	316
I/O	-	-	P84	319
I/O	-	-	P85	322
VCC	-	-	P86	-
I/O	P43	P60	P87	325
I/O	P44	P61	P88	328
I/O	-	P62	P89	331
I/O	-	P63	P90	334
GND	-	P64	P91	-
I/O	-	-	P92	337
I/O	-	-	P93	340
I/O	-	-	P94	343
I/O	-	-	P95	343
I/O	-	-	P96	346
I/O	P45	P65	P97	349
I/O	P46	P66	P98	352
I/O	-	P67	P99	355
I/O	-	P68	P100	358
I/O	P47	P69	P101	361
I/O, SGCK3	P48	P70	P102	364
GND	P49	P71	P103	-
DONE	P50	P72	P104	-
VCC	P51	P73	P105	-
$\overline{\text{PROGRAM}}$	P52	P74	P106	-
I/O	P53	P75	P107	367
I/O, PGCK3	P54	P76	P108	370
I/O	-	P77	P109	373
I/O	-	P78	P110	376
I/O	-	-	P111	
I/O	P55	P79	P112	379
I/O	P56	P80	P113	382
I/O	-	-	P114	385
I/O	-	-	P115	388
I/O	-	-	P116	391
I/O	-	-	P117	394
GND	-	P81	P118	-
I/O	-	P82	P119	397
I/O	-	P83	P120	400
VCC	-	-	P121	-
I/O	P57	P84	P122	403
I/O	P58	P85	P123	406
I/O	-	-	P124	409
I/O	-	-	P125	412
I/O	P59	P86	P126	415
I/O	P60	P87	P127	418
I/O	P61	P88	P128	421
I/O	P62	P89	P129	424
VCC	P63	P90	P130	-

XCS20 & XCS20XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
GND	P64	P91	P131	-
I/O	P65	P92	P132	427
I/O	P66	P93	P133	430
I/O	P67	P94	P134	433
I/O	-	P95	P135	436
I/O	-	-	P136	439
I/O	-	-	P137	442
I/O	P68	P96	P138	445
I/O	P69	P97	P139	448
VCC	-	-	P140	-
I/O	-	P98	P141	451
I/O	-	P99	P142	454
GND	-	P100	P143	-
I/O	-	-	P144	457
I/O	-	-	P145	460
I/O	-	-	P146	463
I/O	-	-	P147	463
I/O	-	-	P148	466
I/O	P70	P101	P149	469
I/O	P71	P102	P150	472
I/O	-	P103	P151	475
I/O	-	P104	P152	478
I/O (DIN)	P72	P105	P153	481
I/O, SGCK4 (DOUT)	P73	P106	P154	484
CCLK	P74	P107	P155	-
VCC	P75	P108	P156	-

XCS20 & XCS20XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
O, TDO	P76	P109	P157	0
GND	P77	P110	P158	-
I/O	P78	P111	P159	2
I/O, PGCK4	P79	P112	P160	5
I/O	-	P113	P161	8
I/O	-	P114	P162	11
I/O	P80	P115	P163	14
I/O	P81	P116	P164	17
I/O	-	-	P165	20
I/O	-	P117	P166	20
I/O	-	-	P167	23
I/O	-	-	P168	26
I/O	-	-	P169	29
GND	-	P118	P170	-
I/O	-	P119	P171	32
I/O	-	P120	P172	35
VCC	-	-	P173	-
I/O	P82	P121	P174	38
I/O	P83	P122	P175	41
I/O	-	-	P176	44
I/O	-	-	P177	47
I/O	P84	P123	P178	50
I/O	P85	P124	P179	53
I/O	P86	P125	P180	56
I/O	P87	P126	P181	59
GND	P88	P127	P182	-

10/22/97

Pin Locations for XCS30 & XCS30XL Devices

XCS30 & XCS30XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
VCC	P89	P128	P183	P212	VCC*	-
I/O	P90	P129	P184	P213	C10	74
I/O	P91	P130	P185	P214	D10	77
I/O	P92	P131	P186	P215	A9	80
I/O	P93	P132	P187	P216	B9	83
I/O	-	-	P188	P217	C9	86
I/O	-	-	P189	P218	D9	89
I/O	P94	P133	P190	P220	A8	92
I/O	P95	P134	P191	P221	B8	95
VCC	-	-	P192	P222	VCC*	-
I/O	-	-	-	P223	A6	98
I/O	-	-	-	P224	C7	101
I/O	-	P135	P193	P225	B6	104
I/O	-	P136	P194	P226	A5	107
GND	-	P137	P195	P227	GND*	-
I/O	-	-	P196	P228	C6	110
I/O	-	-	P197	P229	B5	113
I/O	-	-	P198	P230	A4	116
I/O	-	-	P199	P231	C5	119
I/O	P96	P138	P200	P232	B4	122
I/O	P97	P139	P201	P233	A3	125
I/O	-	-	P202	P234	D5	128
I/O	-	-	P203	P235	C4	131

XCS30 & XCS30XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
I/O	-	P140	P204	P236	B3	134
I/O	-	P141	P205	P237	B2	137
I/O	P98	P142	P206	P238	A2	140
I/O, SGCK1	P99	P143	P207	P239	C3	143
VCC	P100	P144	P208	P240	VCC*	-
GND	P1	P1	P1	P1	GND*	-
I/O, PGCK1	P2	P2	P2	P2	B1	146
I/O	P3	P3	P3	P3	C2	149
I/O	-	P4	P4	P4	D2	152
I/O	-	P5	P5	P5	D3	155
I/O, TDI	P4	P6	P6	P6	E4	158
I/O, TCK	P5	P7	P7	P7	C1	161
I/O	-	-	P8	P8	D1	164
I/O	-	-	P9	P9	E3	167
I/O	-	-	P10	P10	E2	170
I/O	-	-	P11	P11	E1	173
I/O	-	-	P12	P12	F3	176
I/O	-	-	-	P13	F2	179
GND	-	P8	P13	P14	GND*	-
I/O	-	P9	P14	P15	G3	182
I/O	-	P10	P15	P16	G2	185
I/O, TMS	P6	P11	P16	P17	G1	188
I/O	P7	P12	P17	P18	H3	191

XCS30 & XCS30XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
VCC	-	-	P18	P19	VCC*	-
I/O	-	-	-	P20	H2	194
I/O	-	-	-	P21	H1	197
I/O	-	-	P19	P23	J2	200
I/O	-	-	P20	P24	J1	203
I/O	-	P13	P21	P25	K2	206
I/O	P8	P14	P22	P26	K3	209
I/O	P9	P15	P23	P27	K1	212
I/O	P10	P16	P24	P28	L1	215
GND	P11	P17	P25	P29	GND*	-
VCC	P12	P18	P26	P30	VCC*	-
I/O	P13	P19	P27	P31	L2	218
I/O	P14	P20	P28	P32	L3	221
I/O	P15	P21	P29	P33	L4	224
I/O	-	P22	P30	P34	M1	227
I/O	-	-	P31	P35	M2	230
I/O	-	-	P32	P36	M3	233
I/O	-	-	-	P38	N1	236
I/O	-	-	-	P39	N2	239
VCC	-	-	P33	P40	VCC*	-
I/O	P16	P23	P34	P41	P1	242
I/O	P17	P24	P35	P42	P2	245
I/O	-	P25	P36	P43	R1	248
I/O	-	P26	P37	P44	P3	251
GND	-	P27	P38	P45	GND*	-
I/O	-	-	-	P46	T1	254
I/O	-	-	P39	P47	R3	257
I/O	-	-	P40	P48	T2	260
I/O	-	-	P41	P49	U1	263
I/O	-	-	P42	P50	T3	266
I/O	-	-	P43	P51	U2	269
I/O	P18	P28	P44	P52	V1	272
I/O	P19	P29	P45	P53	T4	275
I/O	-	P30	P46	P54	U3	278
I/O	-	P31	P47	P55	V2	281
I/O	P20	P32	P48	P56	W1	284
I/O, SGCK2	P21	P33	P49	P57	V3	287
Don't Connect	P22	P34	P50	P58	W2	290
GND	P23	P35	P51	P59	GND*	-
MODE	P24	P36	P52	P60	Y1	293
VCC	P25	P37	P53	P61	VCC*	-
Don't Connect	P26	P38	P54	P62	W3	294
I/O, PGCK2	P27	P39	P55	P63	Y2	295
I/O (HDC)	P28	P40	P56	P64	W4	298
I/O	-	P41	P57	P65	V4	301
I/O	-	P42	P58	P66	U5	304
I/O	P29	P43	P59	P67	Y3	307
I/O ($\overline{\text{LDC}}$)	P30	P44	P60	P68	Y4	310
I/O	-	-	P61	P69	V5	313
I/O	-	-	P62	P70	W5	316
I/O	-	-	P63	P71	Y5	319
I/O	-	-	P64	P72	V6	322
I/O	-	-	P65	P73	W6	325
I/O	-	-	-	P74	Y6	328
GND	-	P45	P66	P75	GND*	-
I/O	-	P46	P67	P76	W7	331
I/O	-	P47	P68	P77	Y7	334
I/O	P31	P48	P69	P78	V8	337
I/O	P32	P49	P70	P79	W8	340
VCC	-	-	P71	P80	VCC*	-
I/O	-	-	P72	P81	Y8	343
I/O	-	-	P73	P82	U9	346
I/O	-	-	-	P84	Y9	349
I/O	-	-	-	P85	W10	352
I/O	P33	P50	P74	P86	V10	355
I/O	P34	P51	P75	P87	Y10	358
I/O	P35	P52	P76	P88	Y11	361
I/O ($\overline{\text{INIT}}$)	P36	P53	P77	P89	W11	364
VCC	P37	P54	P78	P90	VCC*	-
GND	P38	P55	P79	P91	GND*	-
I/O	P39	P56	P80	P92	V11	367
I/O	P40	P57	P81	P93	U11	370
I/O	P41	P58	P82	P94	Y12	373
I/O	P42	P59	P83	P95	W12	376
I/O	-	-	P84	P96	V12	379
I/O	-	-	P85	P97	U12	382
I/O	-	-	-	P99	V13	385
I/O	-	-	-	P100	Y14	388
VCC	-	-	P86	P101	VCC*	-
I/O	P43	P60	P87	P102	Y15	391
I/O	P44	P61	P88	P103	V14	394
I/O	-	P62	P89	P104	W15	397
I/O	-	P63	P90	P105	Y16	400
GND	-	P64	P91	P106	GND*	-
I/O	-	-	-	P107	V15	403
I/O	-	-	-	P108	W16	406
I/O	-	-	P93	P109	Y17	409
I/O	-	-	P94	P110	V16	412
I/O	-	-	P95	P111	W17	415
I/O	-	-	P96	P112	Y18	418
I/O	P45	P65	P97	P113	U16	421
I/O	P46	P66	P98	P114	V17	424
I/O	-	P67	P99	P115	W18	427
I/O	-	P68	P100	P116	Y19	430
I/O	P47	P69	P101	P117	V18	433
I/O, SGCK3	P48	P70	P102	P118	W19	436
GND	P49	P71	P103	P119	GND*	-
DONE	P50	P72	P104	P120	Y20	-
VCC	P51	P73	P105	P121	VCC*	-
$\overline{\text{PROGRAM}}$	P52	P74	P106	P122	V19	-
I/O	P53	P75	P107	P123	U19	439
I/O, PGCK3	P54	P76	P108	P124	U18	442
I/O	-	P77	P109	P125	T17	445
I/O	-	P78	P110	P126	V20	448
I/O	-	-	-	P127	U20	451
I/O	-	-	P111	P128	T18	454
I/O	P55	P79	P112	P129	T19	457
I/O	P56	P80	P113	P130	T20	460
I/O	-	-	P114	P131	R18	463
I/O	-	-	P115	P132	R19	466
I/O	-	-	P116	P133	R20	469
I/O	-	-	P117	P134	P18	472

XCS30 & XCS30XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
GND	-	P81	P118	P135	GND*	-
I/O	-	-	-	P136	P20	475
I/O	-	-	-	P137	N18	478
I/O	-	P82	P119	P138	N19	481
I/O	-	P83	P120	P139	N20	484
VCC	-	-	P121	P140	VCC*	-
I/O	P57	P84	P122	P141	M17	487
I/O	P58	P85	P123	P142	M18	490
I/O	-	-	P124	P144	M20	493
I/O	-	-	P125	P145	L19	496
I/O	P59	P86	P126	P146	L18	499
I/O	P60	P87	P127	P147	L20	502
I/O	P61	P88	P128	P148	K20	505
I/O	P62	P89	P129	P149	K19	508
VCC	P63	P90	P130	P150	VCC*	-
GND	P64	P91	P131	P151	GND*	-
I/O	P65	P92	P132	P152	K18	511
I/O	P66	P93	P133	P153	K17	514
I/O	P67	P94	P134	P154	J20	517
I/O	-	P95	P135	P155	J19	520
I/O	-	-	P136	P156	J18	523
I/O	-	-	P137	P157	J17	526
I/O	P68	P96	P138	P159	H19	529
I/O	P69	P97	P139	P160	H18	532
VCC	-	-	P140	P161	VCC*	-
I/O	-	P98	P141	P162	G19	535
I/O	-	P99	P142	P163	F20	538
I/O	-	-	-	P164	G18	541
I/O	-	-	-	P165	F19	544
GND	-	P100	P143	P166	GND*	-
I/O	-	-	-	P167	F18	547
I/O	-	-	P144	P168	E19	550
I/O	-	-	P145	P169	D20	553
I/O	-	-	P146	P170	E18	556
I/O	-	-	P147	P171	D19	559
I/O	-	-	P148	P172	C20	562
I/O	P70	P101	P149	P173	E17	565
I/O	P71	P102	P150	P174	D18	568
I/O	-	P103	P151	P175	C19	571
I/O	-	P104	P152	P176	B20	574
I/O (DIN)	P72	P105	P153	P177	C18	577
I/O, SGCK4 (DOUT)	P73	P106	P154	P178	B19	580
CCLK	P74	P107	P155	P179	A20	-
VCC	P75	P108	P156	P180	VCC*	-
O, TDO	P76	P109	P157	P181	A19	0
GND	P77	P110	P158	P182	GND*	-
I/O	P78	P111	P159	P183	B18	2
I/O, PGCK4	P79	P112	P160	P184	B17	5
I/O	-	P113	P161	P185	C17	8
I/O	-	P114	P162	P186	D16	11
I/O	P80	P115	P163	P187	A18	14
I/O	P81	P116	P164	P188	A17	17
I/O	-	-	P165	P189	C16	20
I/O	-	-	-	P190	B16	23
I/O	-	P117	P166	P191	A16	26
I/O	-	-	P167	P192	C15	29
I/O	-	-	P168	P193	B15	32
I/O	-	-	P169	P194	A15	35
GND	-	P118	P170	P196	GND*	-
I/O	-	P119	P171	P197	B14	38
I/O	-	P120	P172	P198	A14	41
I/O	-	-	-	P199	C13	44
I/O	-	-	-	P200	B13	47
VCC	-	-	P173	P201	VCC*	-
I/O	P82	P121	P174	P202	C12	50
I/O	P83	P122	P175	P203	B12	53
I/O	-	-	P176	P205	A12	56
I/O	-	-	P177	P206	B11	59
I/O	P84	P123	P178	P207	C11	62
I/O	P85	P124	P179	P208	A11	65
I/O	P86	P125	P180	P209	A10	68
I/O	P87	P126	P181	P210	B10	71
GND	P88	P127	P182	P211	GND*	-

10/22/97

* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

9/24/97

‡ Pins marked with this symbol are used for Ground connections on some revisions of the device. These pins may not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

6/4/97

Pin Locations for XCS40 & XCS40XL Devices

XCS40 & XCS40XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
VCC	P183	P212	VCC*	-
I/O	P184	P213	C10	86
I/O	P185	P214	D10	89
I/O	P186	P215	A9	92
I/O	P187	P216	B9	95
I/O	P188	P217	C9	98
I/O	P189	P218	D9	101
I/O	P190	P220	A8	104
I/O	P191	P221	B8	107
I/O	-	-	C8	110
I/O	-	-	A7	113
VCC	P192	P222	VCC*	-
I/O	-	P223	A6	116
I/O	-	P224	C7	119
I/O	P193	P225	B6	122
I/O	P194	P226	A5	125
GND	P195	P227	GND*	-
I/O	P196	P228	C6	128
I/O	P197	P229	B5	131
I/O	P198	P230	A4	134
I/O	P199	P231	C5	137
I/O	P200	P232	B4	140
I/O	P201	P233	A3	143
I/O	P202	P234	D5	152
I/O	P203	P235	C4	155
I/O	P204	P236	B3	158
I/O	P205	P237	B2	161
I/O	P206	P238	A2	164
I/O, SGCK1	P207	P239	C3	167
VCC	P208	P240	VCC*	-
GND	P1	P1	GND*	-
I/O, PGCK1	P2	P2	B1	170
I/O	P3	P3	C2	173
I/O	P4	P4	D2	176
I/O	P5	P5	D3	179
I/O, TDI	P6	P6	E4	182
I/O, TCK	P7	P7	C1	185
I/O	P8	P8	D1	194
I/O	P9	P9	E3	197
I/O	P10	P10	E2	200
I/O	P11	P11	E1	203
I/O	P12	P12	F3	206
I/O	-	P13	F2	209
GND	P13	P14	GND*	-
I/O	P14	P15	G3	212
I/O	P15	P16	G2	215
I/O, TMS	P16	P17	G1	218
I/O	P17	P18	H3	221
VCC	P18	P19	VCC*	-
I/O	-	P20	H2	224
I/O	-	P21	H1	227
I/O	-	-	J4	230
I/O	-	-	J3	233
I/O	P19	P23	J2	236
I/O	P20	P24	J1	239
I/O	P21	P25	K2	242
I/O	P22	P26	K3	245
I/O	P23	P27	K1	248
I/O	P24	P28	L1	251
GND	P25	P29	GND*	-
VCC	P26	P30	VCC*	-
I/O	P27	P31	L2	254
I/O	P28	P32	L3	257
I/O	P29	P33	L4	260
I/O	P30	P34	M1	263
I/O	P31	P35	M2	266
I/O	P32	P36	M3	269
I/O	-	-	M4	272
I/O	-	P38	N1	278
I/O	-	P39	N2	281
VCC	P33	P40	VCC*	-
I/O	P34	P41	P1	284
I/O	P35	P42	P2	287
I/O	P36	P43	R1	290
I/O	P37	P44	P3	293
GND	P38	P45	GND*	-
I/O	-	P46	T1	296
I/O	P39	P47	R3	299
I/O	P40	P48	T2	302
I/O	P41	P49	U1	305
I/O	P42	P50	T3	308
I/O	P43	P51	U2	311
I/O	P44	P52	V1	320
I/O	P45	P53	T4	323
I/O	P46	P54	U3	326
I/O	P47	P55	V2	329
I/O	P48	P56	W1	332
I/O, SGCK2	P49	P57	V3	335
Don't Connect	P50	P58	W2	338
GND	P51	P59	GND*	-
MODE	P52	P60	Y1	341
VCC	P53	P61	VCC*	-
Don't Connect	P54	P62	W3	342
I/O PGCK2	P55	P63	Y2	343
I/O (HDC)	P56	P64	W4	346
I/O	P57	P65	V4	349
I/O	P58	P66	U5	352
I/O	P59	P67	Y3	355
I/O ($\overline{\text{LDC}}$)	P60	P68	Y4	358
I/O	P61	P69	V5	367
I/O	P62	P70	W5	370
I/O	P63	P71	Y5	373
I/O	P64	P72	V6	376
I/O	P65	P73	W6	379
I/O	-	P74	Y6	382
GND	P66	P75	GND*	-
I/O	P67	P76	W7	385
I/O	P68	P77	Y7	388

XCS40 & XCS40XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
I/O	P69	P78	V8	391
I/O	P70	P79	W8	394
VCC	P71	P80	VCC*	-
I/O	P72	P81	Y8	397
I/O	P73	P82	U9	400
I/O	-	-	V9	403
I/O	-	-	W9	406
I/O	-	P84	Y9	409
I/O	-	P85	W10	412
I/O	P74	P86	V10	415
I/O	P75	P87	Y10	418
I/O	P76	P88	Y11	421
I/O ($\overline{\text{INIT}}$)	P77	P89	W11	424
VCC	P78	P90	VCC*	-
GND	P79	P91	GND*	-
I/O	P80	P92	V11	427
I/O	P81	P93	U11	430
I/O	P82	P94	Y12	433
I/O	P83	P95	W12	436
I/O	P84	P96	V12	439
I/O	P85	P97	U12	442
I/O	-	-	Y13	445
I/O	-	-	W13	448
I/O	-	P99	V13	451
I/O	-	P100	Y14	454
VCC	P86	P101	VCC*	-
I/O	P87	P102	Y15	457
I/O	P88	P103	V14	460
I/O	P89	P104	W15	463
I/O	P90	P105	Y16	466
GND	P91	P106	GND*	-
I/O	-	P107	V15	469
I/O	P92	P108	W16	472
I/O	P93	P109	Y17	475
I/O	P94	P110	V16	478
I/O	P95	P111	W17	481
I/O	P96	P112	Y18	484
I/O	P97	P113	U16	493
I/O	P98	P114	V17	496
I/O	P99	P115	W18	499
I/O	P100	P116	Y19	502
I/O	P101	P117	V18	505
I/O, SGCK3	P102	P118	W19	508
GND	P103	P119	GND*	-
DONE	P104	P120	Y20	-
VCC	P105	P121	VCC*	-
$\overline{\text{PROGRAM}}$	P106	P122	V19	-
I/O	P107	P123	U19	511
I/O, PGCK3	P108	P124	U18	514
I/O	P109	P125	T17	517
I/O	P110	P126	V20	520
I/O	-	P127	U20	523
I/O	P111	P128	T18	526
I/O	P112	P129	T19	535
I/O	P113	P130	T20	538
I/O	P114	P131	R18	541
I/O	P115	P132	R19	544
I/O	P116	P133	R20	547
I/O	P117	P134	P18	550
GND	P118	P135	GND*	-
I/O	-	P136	P20	553
I/O	-	P137	N18	556
I/O	P119	P138	N19	559
I/O	P120	P139	N20	562
VCC	P121	P140	VCC*	-
I/O	P122	P141	M17	565
I/O	P123	P142	M18	568
I/O	-	-	M19	574
I/O	P124	P144	M20	577
I/O	P125	P145	L19	580
I/O	P126	P146	L18	583
I/O	P127	P147	L20	586
I/O	P128	P148	K20	589
I/O	P129	P149	K19	592
VCC	P130	P150	VCC*	-
GND	P131	P151	GND*	-
I/O	P132	P152	K18	595
I/O	P133	P153	K17	598
I/O	P134	P154	J20	601
I/O	P135	P155	J19	604
I/O	P136	P156	J18	607
I/O	P137	P157	J17	610
I/O	-	-	H20	613
I/O	P138	P159	H19	619
I/O	P139	P160	H18	622
VCC	P140	P161	VCC*	-
I/O	P141	P162	G19	625
I/O	P142	P163	F20	628
I/O	-	P164	G18	631
I/O	-	P165	F19	634
GND	P143	P166	GND*	-
I/O	-	P167	F18	637
I/O	P144	P168	E19	640
I/O	P145	P169	D20	643
I/O	P146	P170	E18	646
I/O	P147	P171	D19	649
I/O	P148	P172	C20	652
I/O	P149	P173	E17	655
I/O	P150	P174	D18	658
I/O	P151	P175	C19	667
I/O	P152	P176	B20	670
I/O (DIN)	P153	P177	C18	673
I/O, SGCK4 (DOUT)	P154	P178	B19	676
CCLK	P155	P179	A20	-
VCC	P156	P180	VCC*	-
O, TDO	P157	P181	A19	0
GND	P158	P182	GND*	-
I/O	P159	P183	B18	2
I/O, PGCK4	P160	P184	B17	5
I/O	P161	P185	C17	8
I/O	P162	P186	D16	11

XCS40 & XCS40XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
I/O	P163	P187	A18	14
I/O	P164	P188	A17	17
I/O	P165	P189	C16	26
I/O	-	P190	B16	29
I/O	P166	P191	A16	32
I/O	P167	P192	C15	35
I/O	P168	P193	B15	38
I/O	P169	P194	A15	41
GND	P170	P196	GND*	-
I/O	P171	P197	B14	44
I/O	P172	P198	A14	47
I/O	-	P199	C13	50
I/O	-	P200	B13	53
VCC	P173	P201	VCC*	-
I/O	-	-	A13	56
I/O	-	-	D12	59
I/O	P174	P202	C12	62
I/O	P175	P203	B12	65
I/O	P176	P205	A12	68
I/O	P177	P206	B11	71
I/O	P178	P207	C11	74
I/O	P179	P208	A11	77
I/O	P180	P209	A10	80
I/O	P181	P210	B10	83
GND	P182	P211	GND*	-

10/23/97

Additional XCS40/XL Package Pins

PQ240

GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

6/9/97

‡ Pins marked with this symbol are used for Ground connections on some revisions of the device. These pins may not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

6/17/97

Product Availability

Table 16 shows the packages and speed grades for Spartan Series devices. Table 17 shows the number of user IOs avalable for each device/package combination.

Table 16: Component Availability Chart for Spartan Series FPGAs

	PINS	84	100	144	208	240	256
	TYPE	Plast. PLCC	Plast. VQFP	Plast. TQFP	Plast. PQFP	Plast. PQFP	Plast. BGA
Device	CODE	PC84	VQ100	TQ144	PQ208	PQ240	BG256
XCS05	-3	C(I)	C(I)				
	-4	C	C				
XCS10	-3	C(I)	C(I)	C(I)			
	-4	C	C	C			
XCS20	-3		C(I)	C(I)	C(I)		
	-4		C	C	C		
XCS30	-3		C(I)	C(I)	C(I)	C(I)	C(I)
	-4		C	C	C	C	C
XCS40	-3				C(I)	C(I)	C(I)
	-4				C	C	C
XCS05XL	-3	C(I)	C(I)				
	-4	C	C				
XCS10XL	-3	C(I)	C(I)	C(I)			
	-4	C	C	C			
XCS20XL	-3		C(I)	C(I)	C(I)		
	-4		C	C	C		
XCS30XL	-3		C(I)	C(I)	C(I)	C(I)	C(I)
	-4		C	C	C	C	C
XCS40XL	-3				C(I)	C(I)	C(I)
	-4				C	C	C

9/24/97

C = Commercial $T_J = 0°$ to $+85°C$

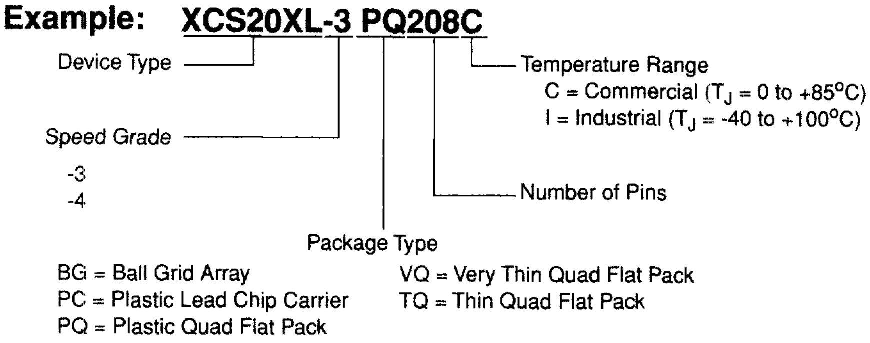
I= Industrial $T_J = -40°C$ to $+100°C$

Table 17: User I/O Chart for Spartan Series FPGAs

Device	Max I/O	Package Type					
		PC84	VQ100	TQ144	PQ208	PQ240	BG256
XCS05	80	61	77				
XCS10	112	61	77	112			
XCS20	160		77	113	160		
XCS30	192		77	113	169	192	192
XCS40	224				169	193	205
XCS05XL	80	61	77				
XCS10XL	112	61	77	112			
XCS20XL	160		77	113	160		
XCS30XL	192		77	113	169	192	192
XCS40XL	224				169	193	205

9/24/97

Ordering Information



Example: XCS20XL-3 PQ208C

Device Type

Speed Grade
-3
-4

Package Type
BG = Ball Grid Array
PC = Plastic Lead Chip Carrier
PQ = Plastic Quad Flat Pack
VQ = Very Thin Quad Flat Pack
TQ = Thin Quad Flat Pack

Number of Pins

Temperature Range
C = Commercial (T_J = 0 to +85°C)
I = Industrial (T_J = -40 to +100°C)