# FAST CMOS 8-BIT IDENTITY COMPARATOR

**IDT54/74FCT521/A/B/C**

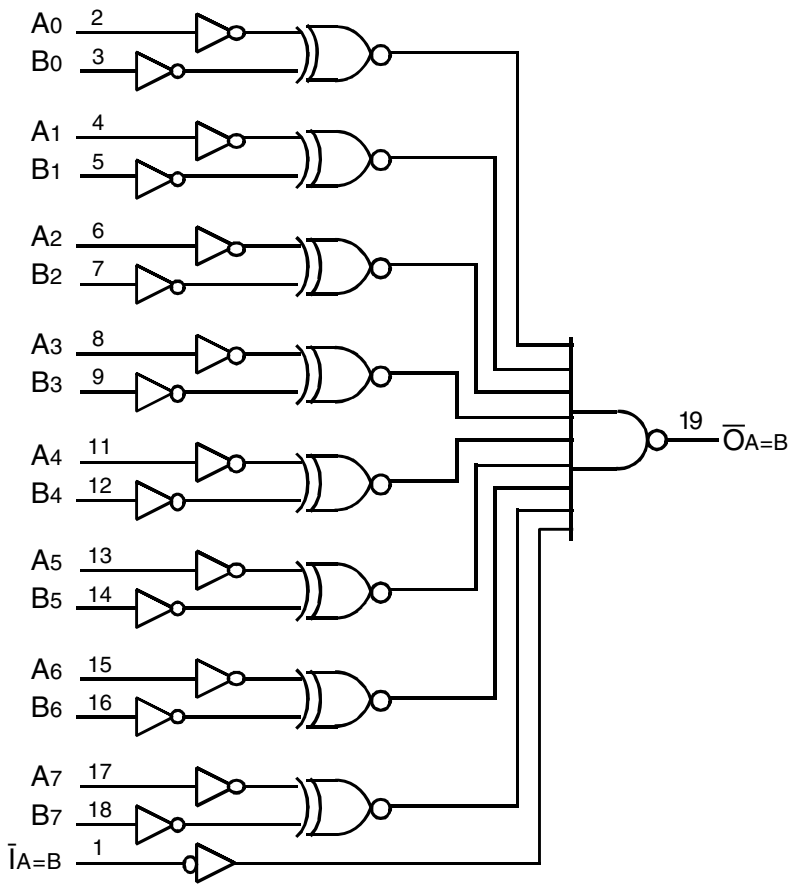
## FEATURES:

- **IDT54/74FCT521 equivalent to FAST™ speed**
- **IDT54/74FCT521A up to 35% faster than FAST**
- **IDT54/74FCT521B up to 35% faster than FAST**
- **IDT54/74FCT521C up to 60% faster than FAST**
- **Eqivalent to FAST output drive over full temperature and voltage supply extremes**
- **$I_{OL}$ = 48mA (commercial) and 32mA (military)**
- **CMOS power levels (1mW typ. static)**
- **TTL input and output level compatible**
- **CMOS output level compatible**
- **Substantially lower input current levels than FAST (5µA max.)**
- **MIlitary product compliant to MIL-STD-883, Class B**
- **Meets or exceeds JEDEC Standard 18 specifications**
- **Available in the following packages:**
  - *Commercial: SOIC*
  - *Military: CERDIP, LCC*

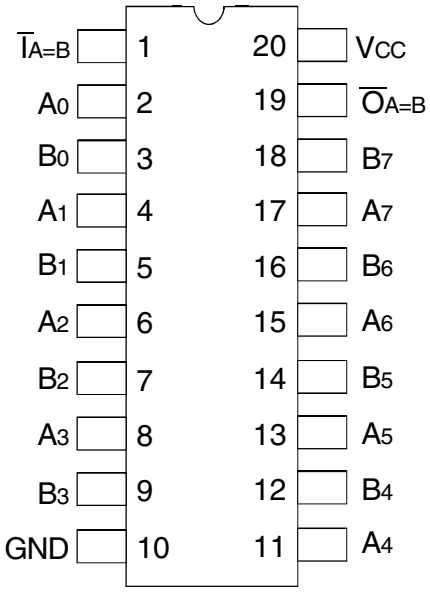
## DESCRIPTION:

The FCT521 is an 8-bit identity comparator built using an advanced dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a low output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active low enable input.

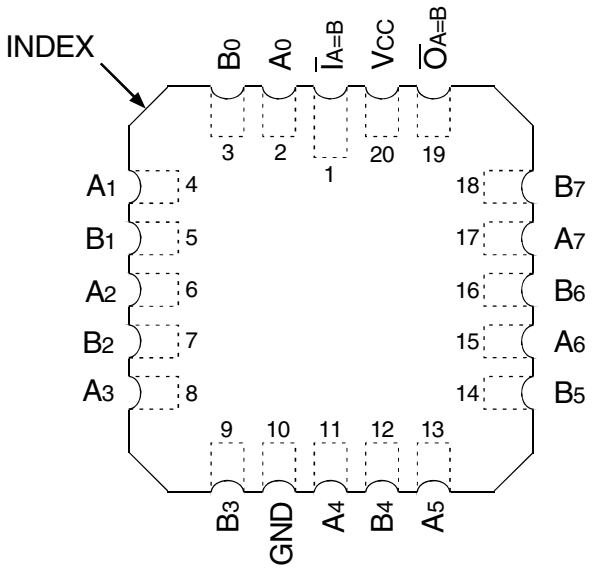
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**CERDIP/ SOIC**
**TOP VIEW**




**LCC**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7 | –0.5 to +7 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ | –0.5 to $V_{CC}$ | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature under BIAS | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 0.5 | 0.5 | W |
| $I_{OUT}$ | DC Output Current | 120 | 120 | mA |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Output and I/O terminals only.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

**NOTE:**
1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| A0 - A7 | Word A Inputs |
| B0 - B7 | Word B Inputs |
| $\overline{I}_{A=B}$ | Expansion or Enable Input (Active LOW) |
| $\overline{O}_{A=B}$ | Identity Output (Active LOW) |

## FUNCTION TABLE(1)

| Inputs | | Output |
|---|---|---|
| $\overline{I}_{A=B}$ | A, B | $\overline{O}_{A=B}$ |
| L | A = B* | L |
| L | A ≠ B | H |
| H | A = B* | H |
| H | A ≠ B | H |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   *A0 = B0, A1 = B1, A2 = B2, etc.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC}$ = 0.2V; $V_{HC}$ = $V_{CC}$ - 0.2V
Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%, Military: $T_A$ = -55°C to +125°C, $V_{CC}$ = 5.0V ±10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | 5 | µA |
| | | | $V_I$ = 2.7V | — | — | 5[4] | |
| $I_{IL}$ | Input LOW Current | | $V_I$ = 0.5V | — | — | –5[4] | |
| | | | $V_I$ = GND | — | — | –5 | |
| $I_{OZH}$ | Off State (High Impedance) Output Current | $V_{CC}$ = Max. | $V_O$ = $V_{CC}$ | — | — | 10 | µA |
| | | | $V_O$ = 2.7V | — | — | 10[4] | |
| $I_{OZL}$ | | | $V_O$ = 0.5V | — | — | –10[4] | |
| | | | $V_O$ = GND | — | — | –10 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | –60 | –120 | — | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OH}$ = –32µA | | $V_{HC}$ | $V_{CC}$ | — | V |
| | | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –300µA | $V_{HC}$ | $V_{CC}$ | — | |
| | | | $I_{OH}$ = –12mA MIL | 2.4 | 4.3 | — | |
| | | | $I_{OH}$ = –15mA COM'L | 2.4 | 4.3 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 3V, $V_{IN}$ = $V_{LC}$ or $V_{HC}$, $I_{OL}$ = 300µA | | — | GND | $V_{LC}$ | V |
| | | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 300µA | — | GND | $V_{LC}$[4] | |
| | | | $I_{OL}$ = 32mA MIL | — | 0.3 | 0.5 | |
| | | | $I_{OL}$ = 48mA COM'L | — | 0.3 | 0.5 | |

**NOTES:**
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not ttested.

## POWER SUPPLY CHARACTERISTICS

$V_{LC}$ = 0.2V; $V_{HC}$ = $V_{CC}$ - 0.2V

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max.<br>$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ | | — | 0.2 | 1.5 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 2 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>One Input Toggling<br>50% Duty Cycle | $V_{IN} \geq V_{HC}$<br>$V_{IN} \leq V_{LC}$ | — | 0.15 | 0.25 | mA/<br>MHz |
| $I_C$ | Total Power Supply Current[5,6] | $V_{CC}$ = Max.<br>Outputs Open | $V_{IN} \geq V_{HC}$<br>$V_{IN} \leq V_{LC}$ (FCT) | — | 1.7 | 4 | mA |
| | | $f_i$ = 10MHz<br>One Bit Toggling<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 2 | 5 | |

**NOTES:**
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of $\Delta I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for register devices (zero for non-register devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$

All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL

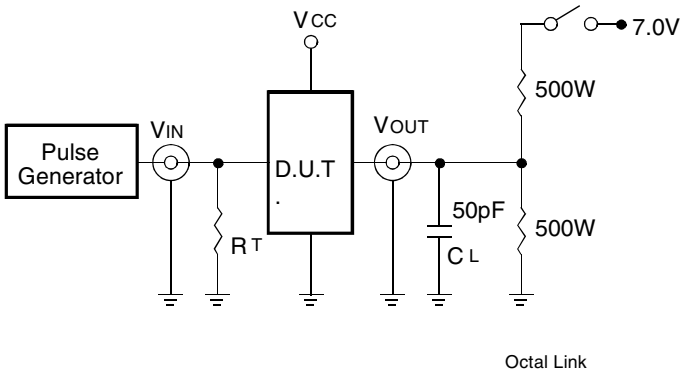
| Symbol | Parameter | Condition[1] | 74FCT521A | | 74FCT521C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Ax or Bx to $\overline{O}_{A=B}$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 7.2 | 1.5 | 4.5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | | 1.5 | 6 | 1.5 | 4.1 | ns |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

| Symbol | Parameter | Condition[1] | 54FCT521 | | 54FCT521A | | 54FCT521B | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Ax or Bx to $\overline{O}_{A=B}$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 15 | 1.5 | 9.5 | 1.5 | 7.3 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | | 1.5 | 9 | 1.5 | 7.8 | 1.5 | 6 | ns |

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

## TEST CIRCUITS AND WAVEFORMS

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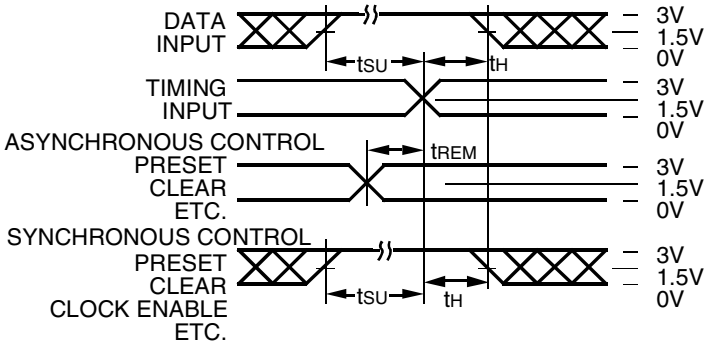
***Test Circuits for All Outputs***

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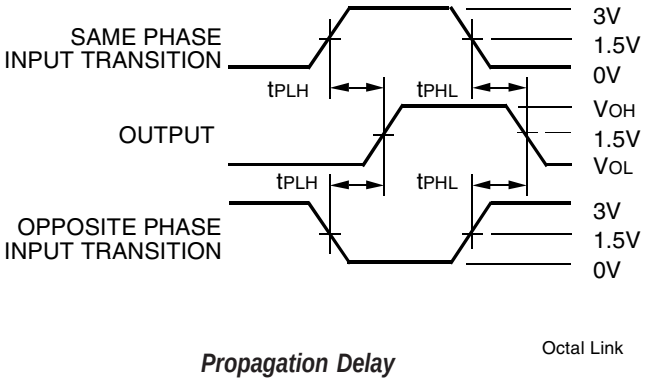
***Set-Up, Hold, and Release Times***

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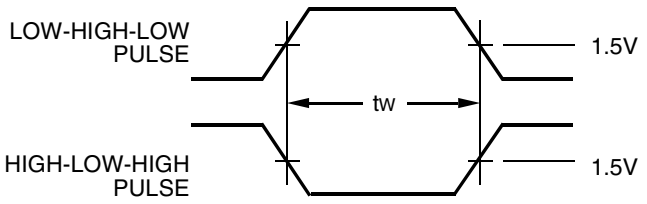
***Propagation Delay***

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

**DEFINITIONS:**
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.




***Pulse Width***

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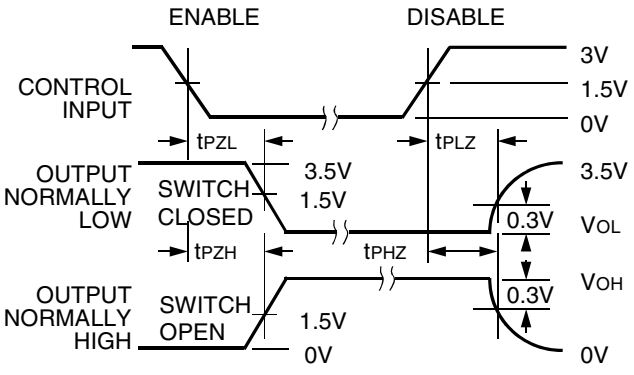


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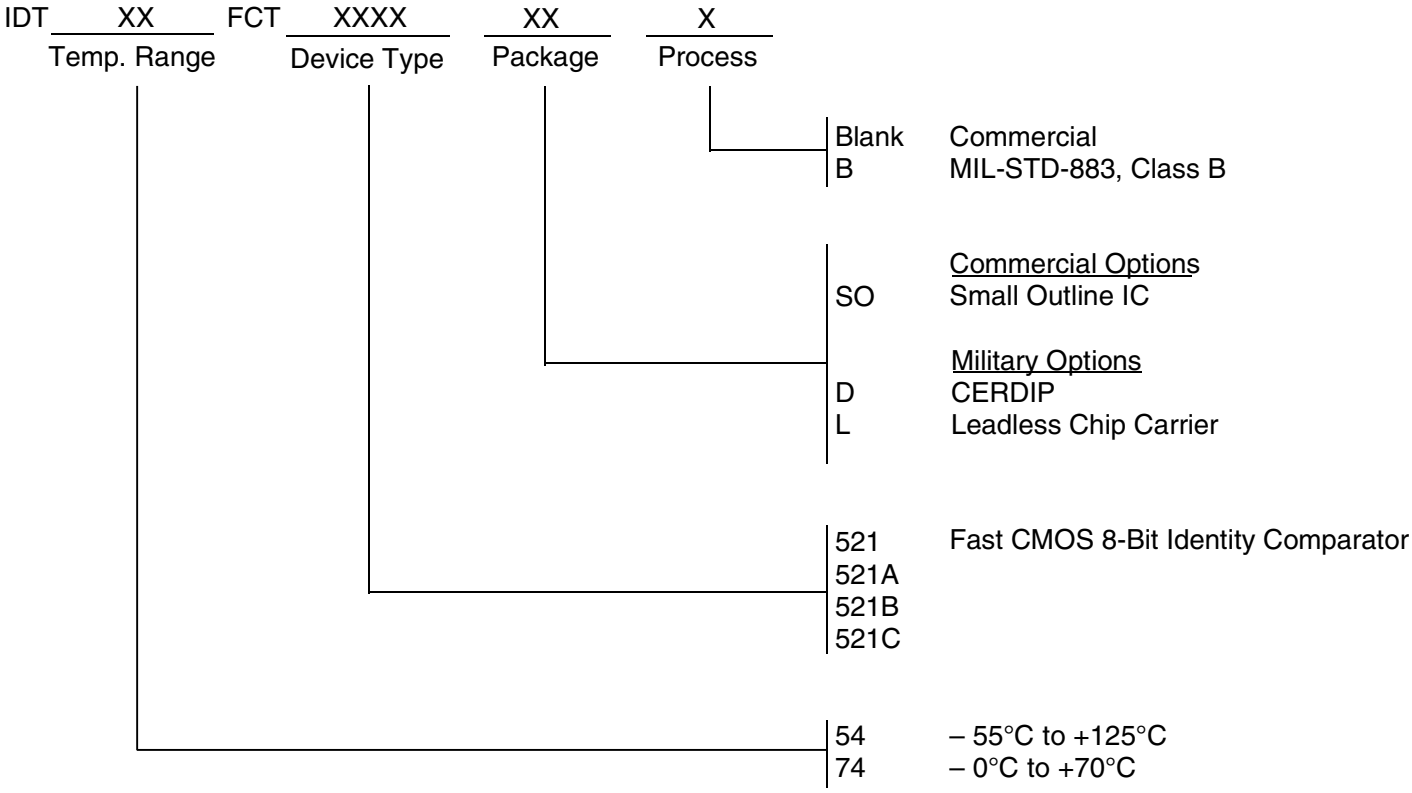
***Enable and Disable Times***

**NOTES:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_O$ ≤ 50Ω; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

## ORDERING INFORMATION

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