1-Mbit (64K x 16) Static RAM

Features

- **Pin- and function-compatible with CY7C1021CV33**
- **High speed**
  - **t_{AA} = 8 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **I_{CC} = 75 mA @ 8 ns**
- **Low CMOS standby power**
  - **I_{SB2} = 3 mA**
- **Data retention at 2.0V**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II, 400-mil SOJ, 48-ball FBGA Pb-Free Packages**

Functional Description[1]

The CY7C1021DV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A_0 through $A_{15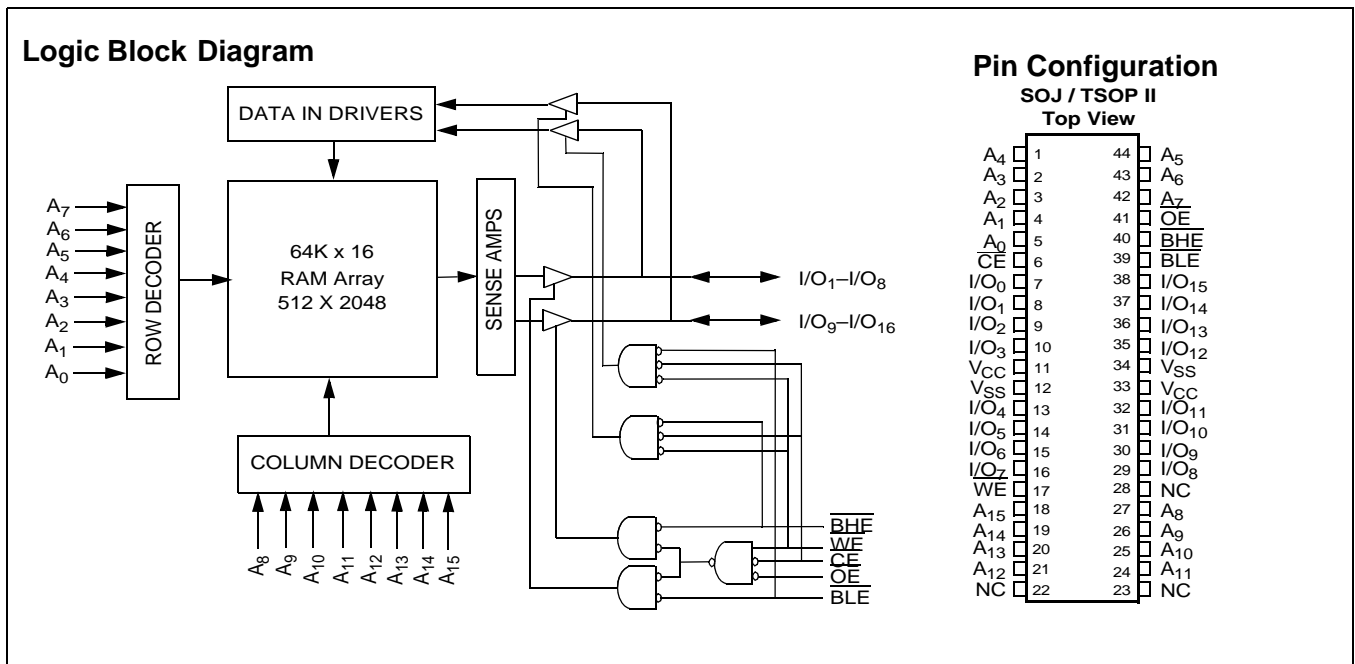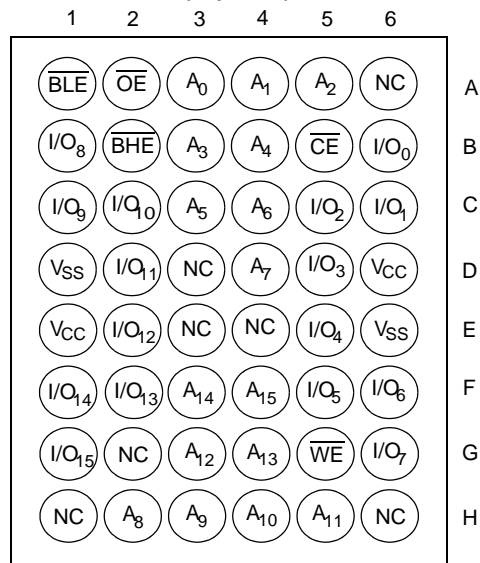}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the BHE and BLE are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021DV33 is available in standard 44-pin TSOP Type II 400-mil-wide SOJ packages, as well as a 48-ball FBGA Pb-Free packages.

Logic Block Diagram

Pin Configuration
SOJ / TSOP II
Top View

Note:
1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at www.cypress.com.

Selection Guide

	CY7C1021DV33-8	CY7C1021DV33-10	Unit
Maximum Access Time	8	10	ns
Maximum Operating Current	75	60	mA
Maximum CMOS Standby Current	3	3	mA

Pin Configuration

48-ball FBGA

(Top View)

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC	A
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	I/O_0	B
C	I/O_9	I/O_{10}	A_5	A_6	I/O_2	I/O_1	C
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{CC}	D
E	V_{CC}	I/O_{12}	NC	NC	I/O_4	V_{SS}	E
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6	F
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7	G
H	NC	A_8	A_9	A_{10}	A_{11}	NC	H

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[2] ....–0.5V to V_{CC}+0.5V

DC Input Voltage[2] ....–0.5V to V_{CC}+0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage...>2001V

(per MIL-STD-883, Method 3015)

Latch-up Current...>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1021DV33-8 Min.	1021DV33-8 Max.	1021DV33-10 Min.	1021DV33-10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	2.0	V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[2]		–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–1	+1	–1	+1	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}		75		60	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		10		10	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		3		3	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance[4]

Parameter	Description	Test Conditions	All - Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[4]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[4]		TBD	°C/W

Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[5]

8-ns devices:

OUTPUT   Z = 50Ω

50Ω   **30 pF***

1.5V

* CAPACITIVE LOAD CONSISTS
OF ALL COMPONENTS OF THE
TEST ENVIRONMENT

(a)

10 -ns devices:

3.3V   R 317Ω

OUTPUT

30 pF   R2 351Ω

(b)

High-Z characteristics:

3.3V   R 317Ω

OUTPUT

5 pF   R2 351Ω

(d)

Equivalent to: THÉVENIN EQUIVALENT
167Ω
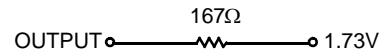
OUTPUT   1.73V

3.0V   ALL INPUT PULSES

90%   90%

GND   10%   10%

Rise Time: 1 V/ns   (c)   Fall Time: 1 V/ns

Switching Characteristics Over the Operating Range[6]

| Parameter	Description	1021DV33-8 Min.	1021DV33-8 Max.	1021DV33-10 Min.	1021DV33-10 Max.	Unit
Read Cycle						
t_{power}[7]	V_{CC}(typical) to the first access	100		100		μs
t_{RC}	Read Cycle Time	8		10		ns
t_{AA}	Address to Data Valid		8		10	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		4		5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[8]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		4		5	ns
t_{PU}[10]	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}[10]	$\overline{CE}$ HIGH to Power-Down		8		10	ns
t_{DBE}	Byte Enable to Data Valid		5		5	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		ns
t_{HZBE}	Byte Disable to High-Z		4		5	ns
Write Cycle[11]						
t_{WC}	Write Cycle Time	8		10		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		ns
t_{AW}	Address Set-Up to Write End	7		8		ns

Notes:
5. AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (d) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
10. This parameter is guaranteed by design and is not tested.
11. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

## Switching Characteristics Over the Operating Range[6]

Parameter	Description	1021DV33-8		1021DV33-10		Unit
		Min.	Max.	Min.	Max.	
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		ns
t_{SD}	Data Set-Up to Write End	5		5		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8, 9]		4		5	ns
t_{BW}	Byte Enable to End of Write	6		7		ns

Data Retention Characteristics Over the Operating Range

Parameter	Description		Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Non-L, Com'l / Ind'l	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3	mA
		L-Version Only			1.2	mA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0		ns
t_R[12]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform
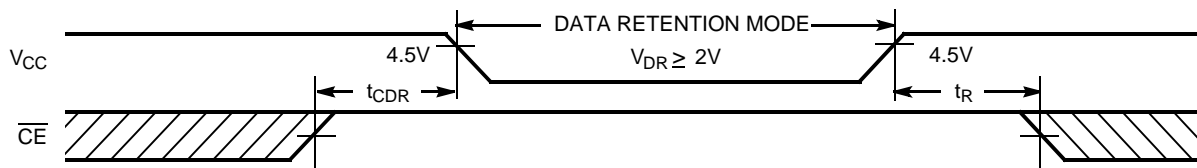
Switching Waveforms

Read Cycle No. 1[13, 14]
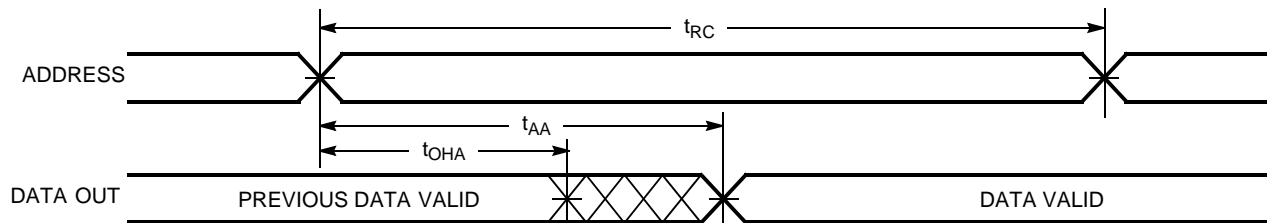
Notes:
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ μs or stable at $V_{CC(min.)} \geq 50$ μs.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
14. WE is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]
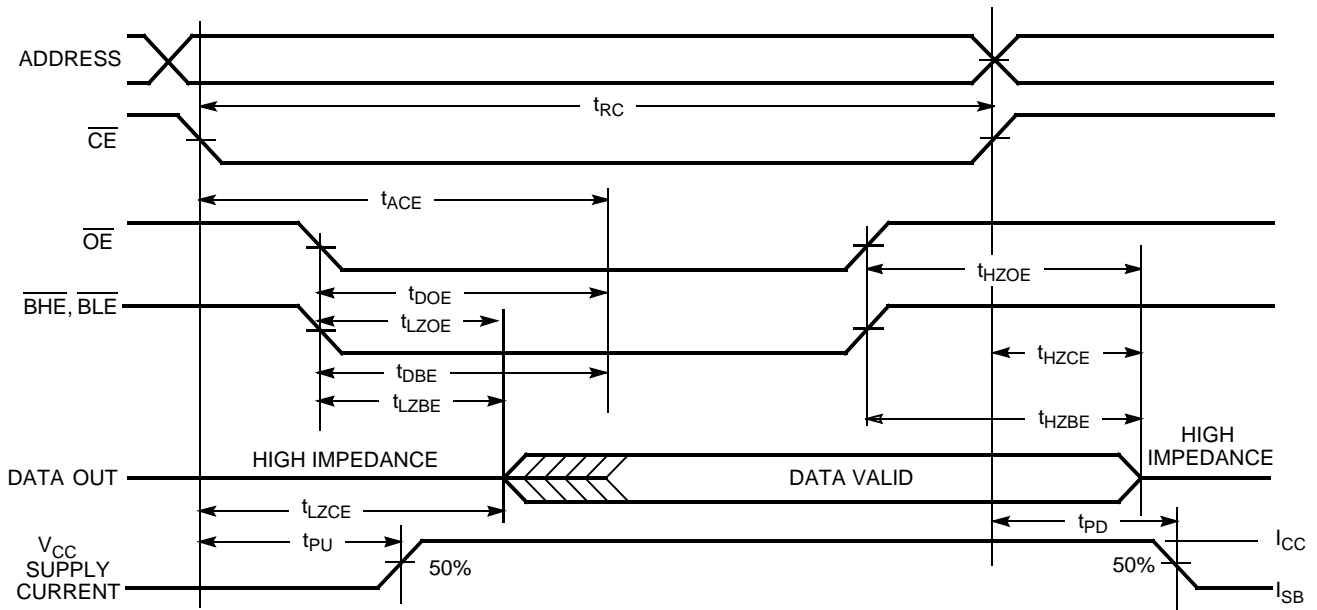
Write Cycle No. 1 ($\overline{CE}$ Controlled)[16, 17]
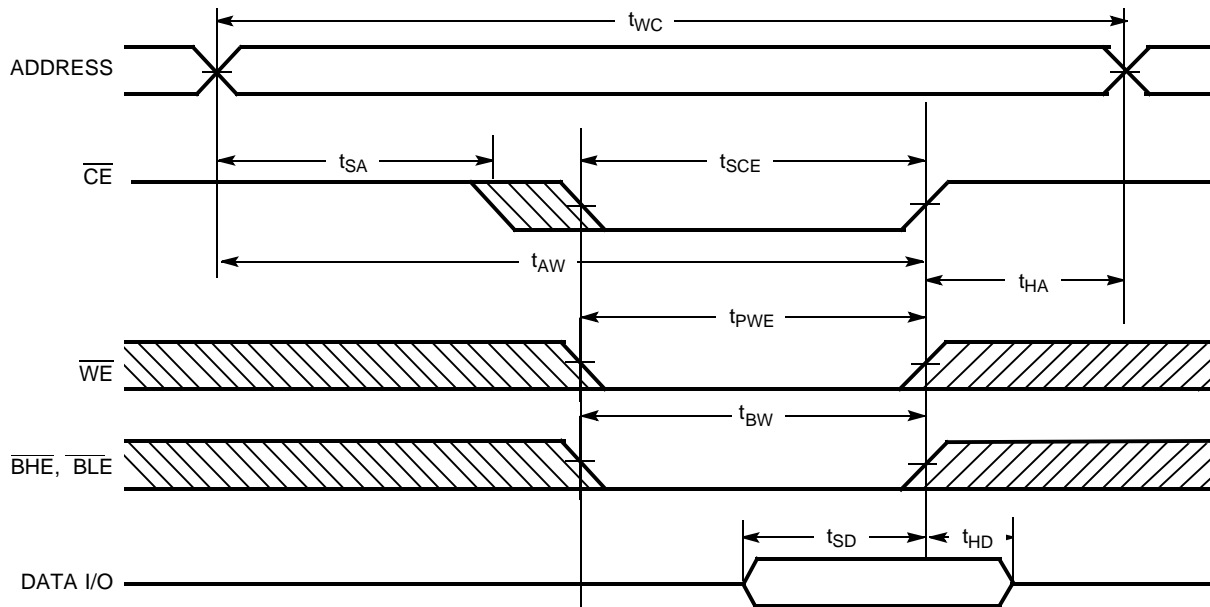
Notes:
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)
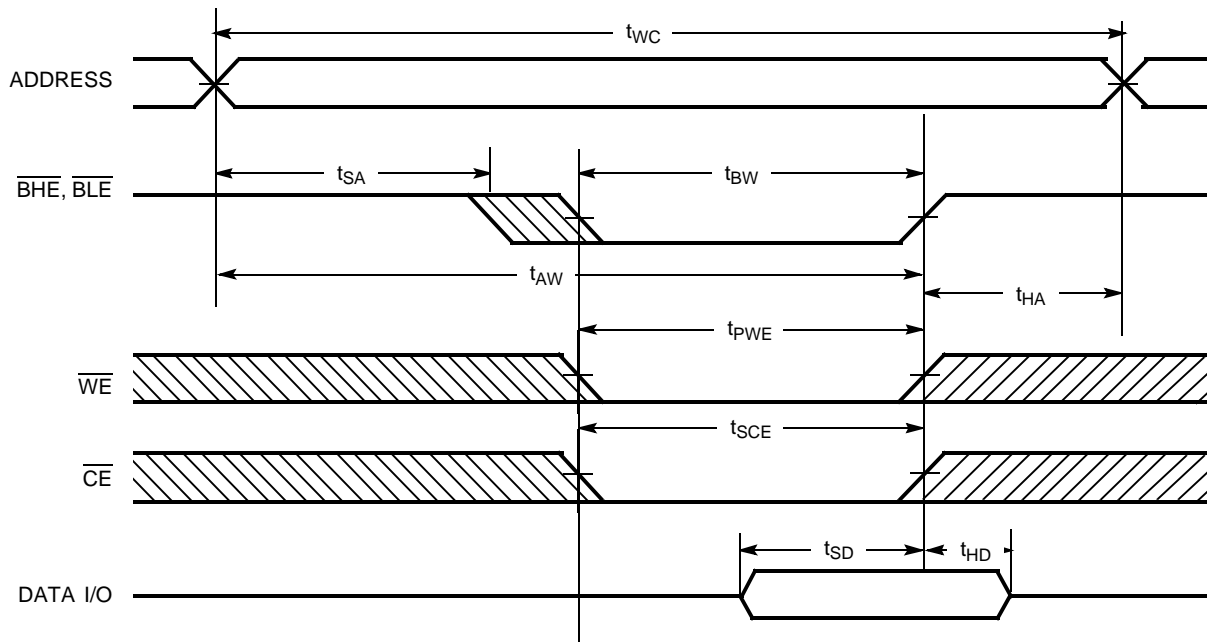
Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)
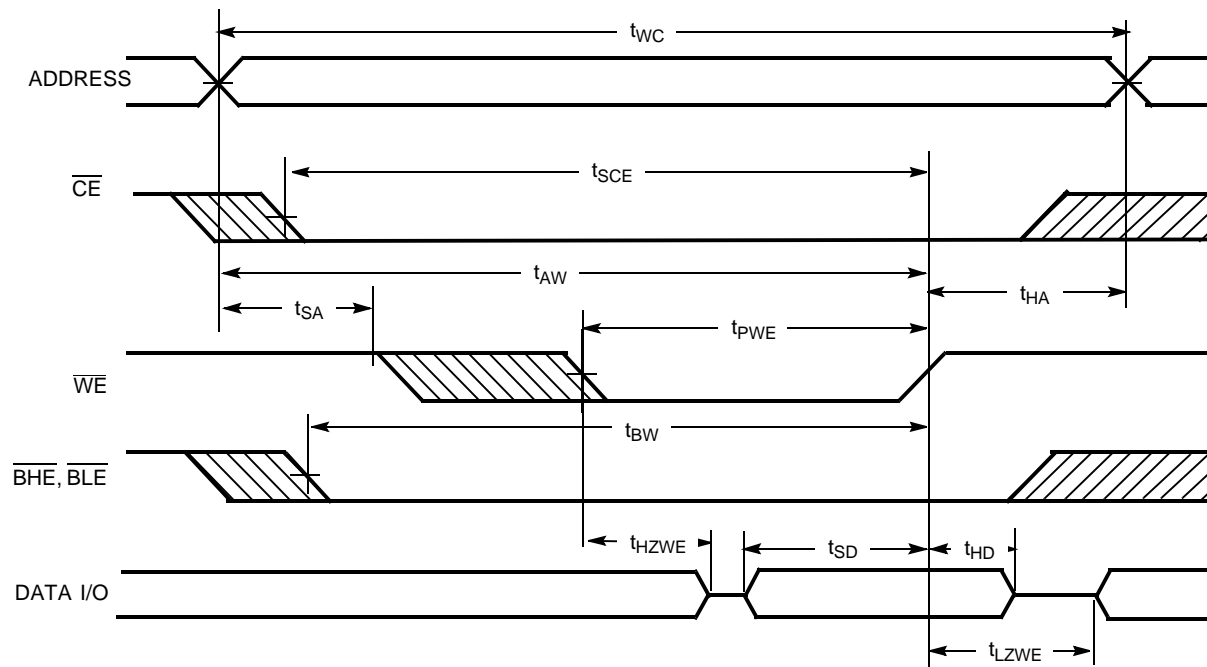
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O$_0$–I/O$_7$	I/O$_8$–I/O$_{15}$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1021DV33-8VXC	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021DV33-8VXI			Industrial
	CY7C1021DV33-8ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021DV33-8ZXI			Industrial
	CY7C1021DV33-8BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021DV33-8BAXI			Industrial
10	CY7C1021DV33-10VXC	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021DV33-10VXI			Industrial
	CY7C1021DV33-10ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021DV33-10ZXI			Industrial
	CY7C1021DV33-10BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021DV33-10BAXI			Industrial

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.
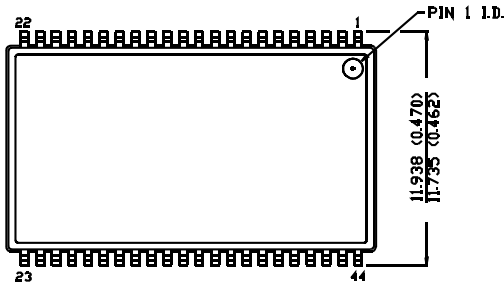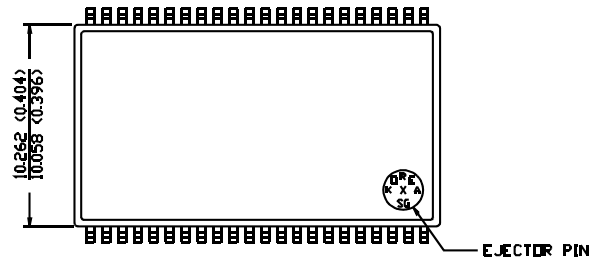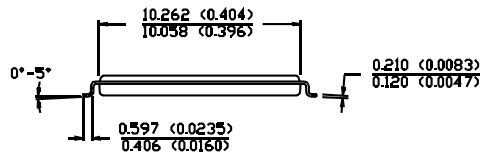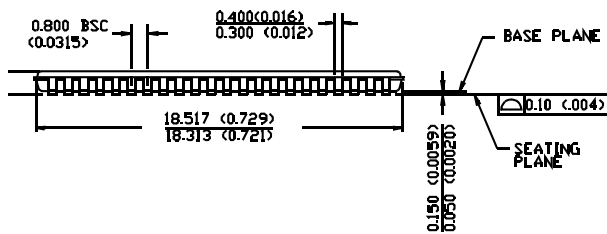
Package Diagrams

48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A

51-85096-*E
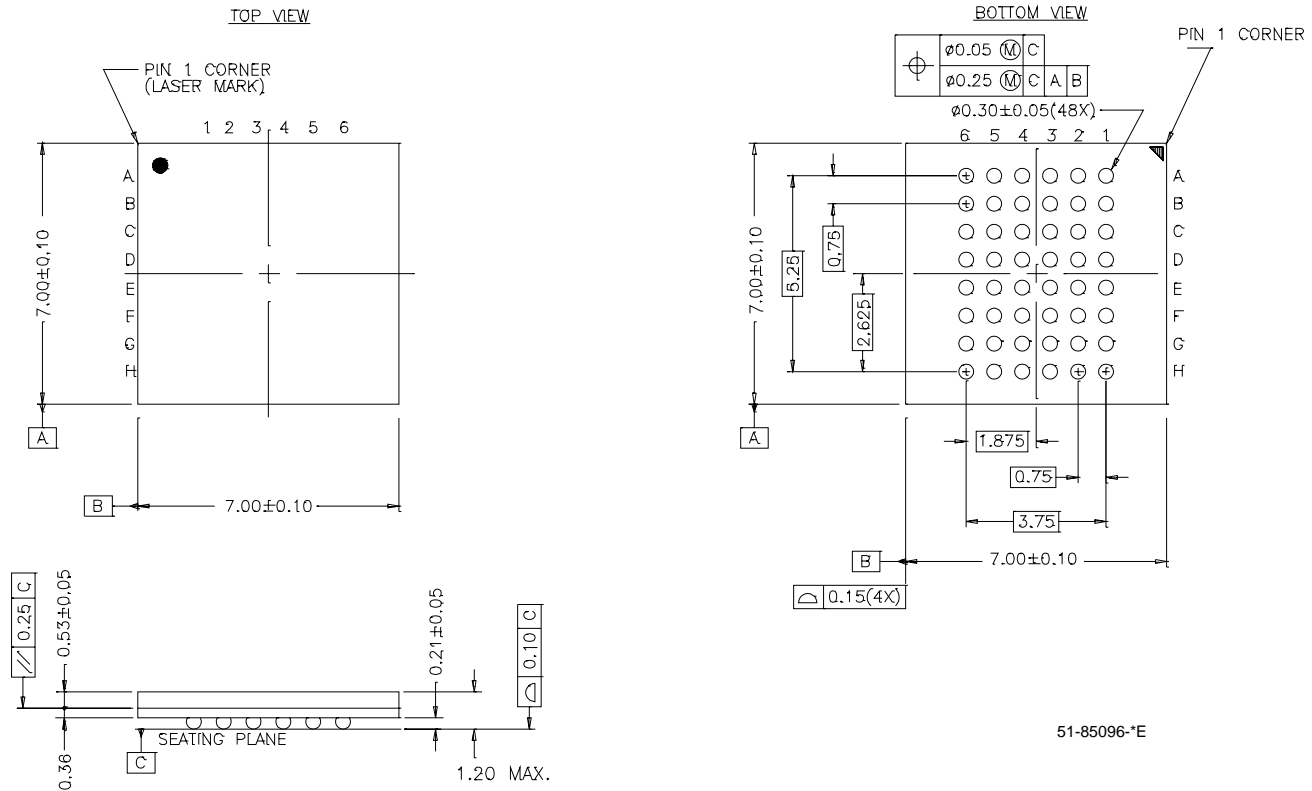
44-Lead (400-Mil) Molded SOJ V34

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$
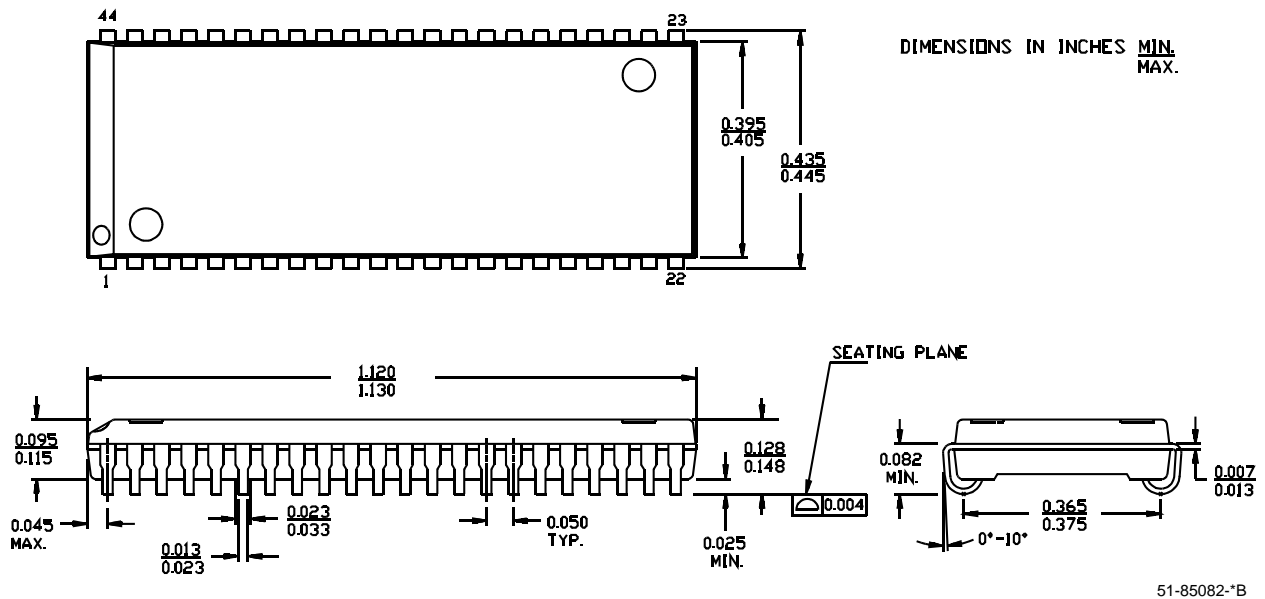
51-85082-*B

Package Diagrams (continued)

44-pin TSOP II Z44

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Document History Page

Document Title: CY7C1021DV33 1-Mbit (64K x 16) Static RAM (Preliminary) Document Number: 38-05460				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233693	See ECN	RKF	DC parameters are modified as per Eros (Spec # 01-02165). Pb-free Offering In Ordering information
*B	263769	See ECN	RKF	Changed $I/O_1 – I/O_{16}$ to $I/O_0 – I/O_{15}$ Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to -8 and -10 ns