

FQD5N60C / FQU5N60C

N-Channel QFET MOSFET

600 V, 2.8 A, 2.5 Ω

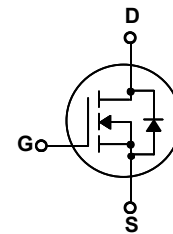
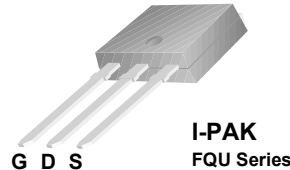
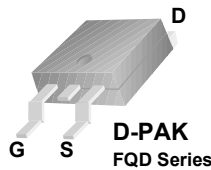


Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 2.8 A, 600 V, $R_{DS(on)} = 2.5 \Omega$ (Max) @ $V_{GS} = 10$ V, $I_D = 1.4$ A
- Low Gate Charge (Typ. 15 nC)
- Low Crss (Typ. 6.5 pF)
- 100% Avalanche Tested
- RoHS compliant



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD5N60C / FQU5N60C	Unit
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	2.8	A
		1.8	A
I_{DM}	Drain Current - Pulsed (Note 1)	11.2	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	210	mJ
I_{AR}	Avalanche Current (Note 1)	2.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)*	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	49	W
		0.39	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	2.56	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	-	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	110	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.6	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}$	--	2.0	2.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 1.4\text{ A}$ (Note 4)	--	4.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	515	670	pF
C_{oss}	Output Capacitance		--	55	72	pF
C_{rss}	Reverse Transfer Capacitance		--	6.5	8.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 4.5\text{ A},$ $R_G = 25\ \Omega$	--	10	30	ns	
t_r	Turn-On Rise Time		--	42	90	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	38	85	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	46	100	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 4.5\text{ A},$ $V_{GS} = 10\text{ V}$	--	15	19	nC	
Q_{gs}	Gate-Source Charge		(Note 4, 5)	--	2.5	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	6.6	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	2.8	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	11.2	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.8\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 4.5\text{ A},$	--	300	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	2.2	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 18.9\text{ mH}, I_{AS} = 4.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

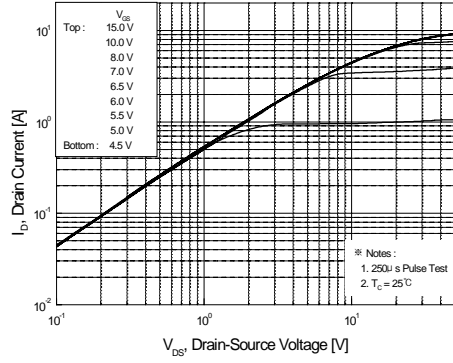


Figure 1. On-Region Characteristics

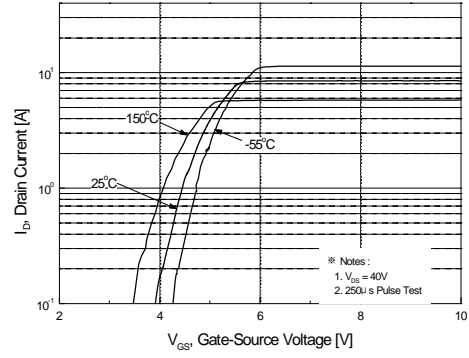


Figure 2. Transfer Characteristics

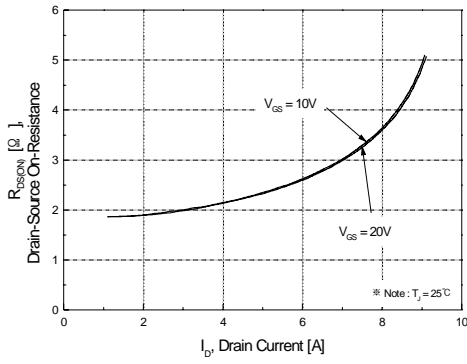


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

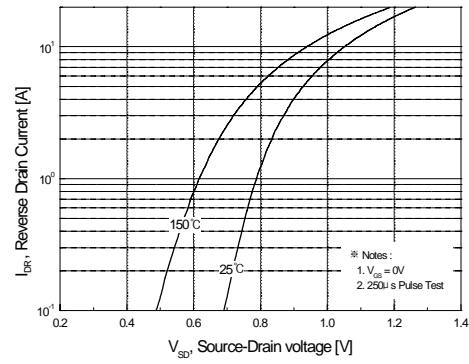


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

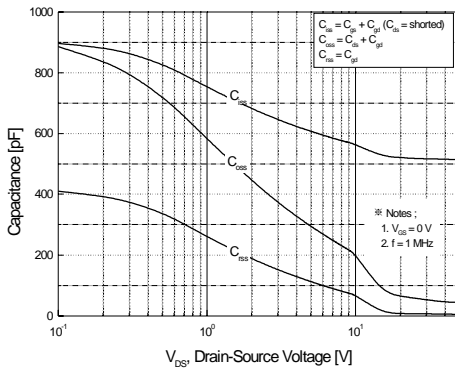


Figure 5. Capacitance Characteristics

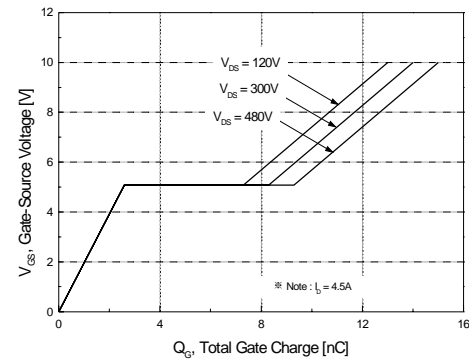


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

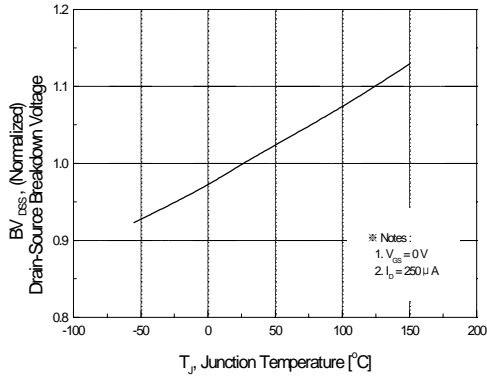


Figure 7. Breakdown Voltage Variation vs Temperature

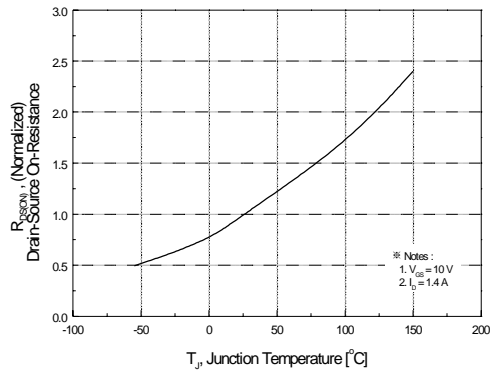


Figure 8. On-Resistance Variation vs Temperature

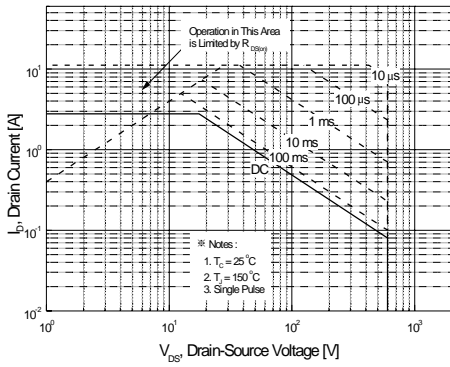


Figure 9. Maximum Safe Operating Area

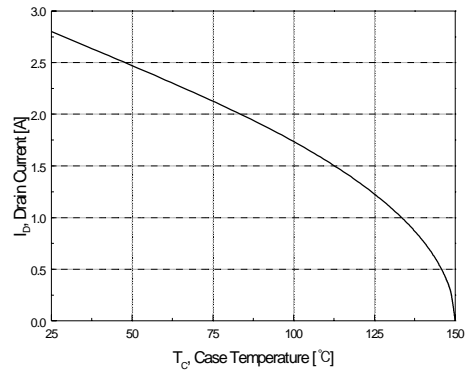


Figure 10. Maximum Drain Current vs Case Temperature

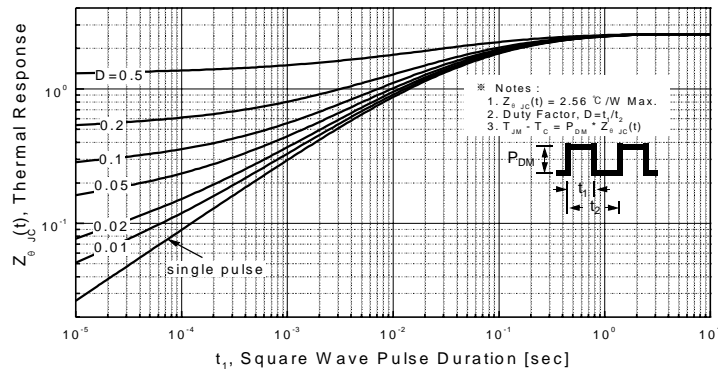
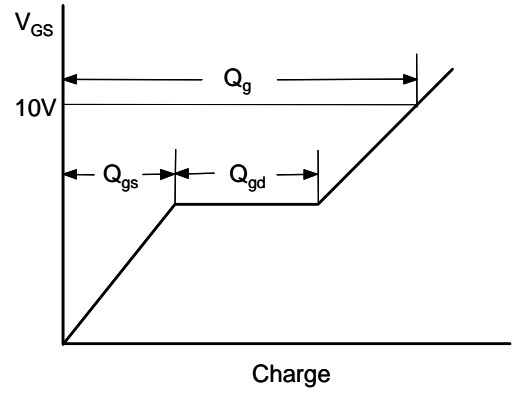
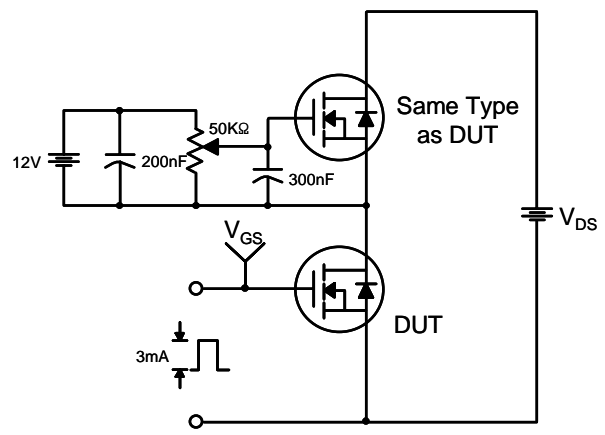
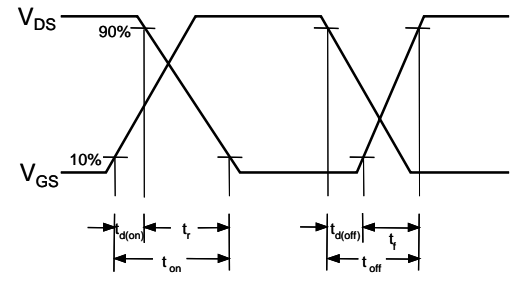
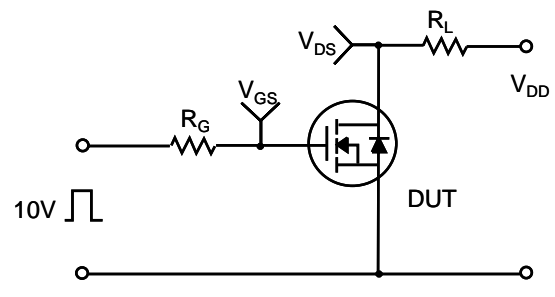


Figure 11. Transient Thermal Response Curve

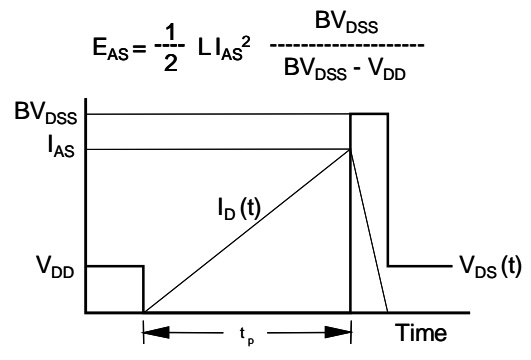
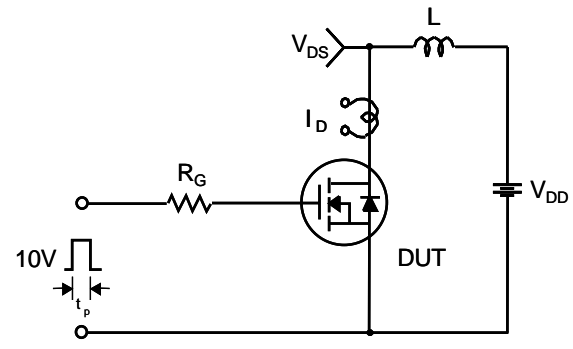
Gate Charge Test Circuit & Waveform



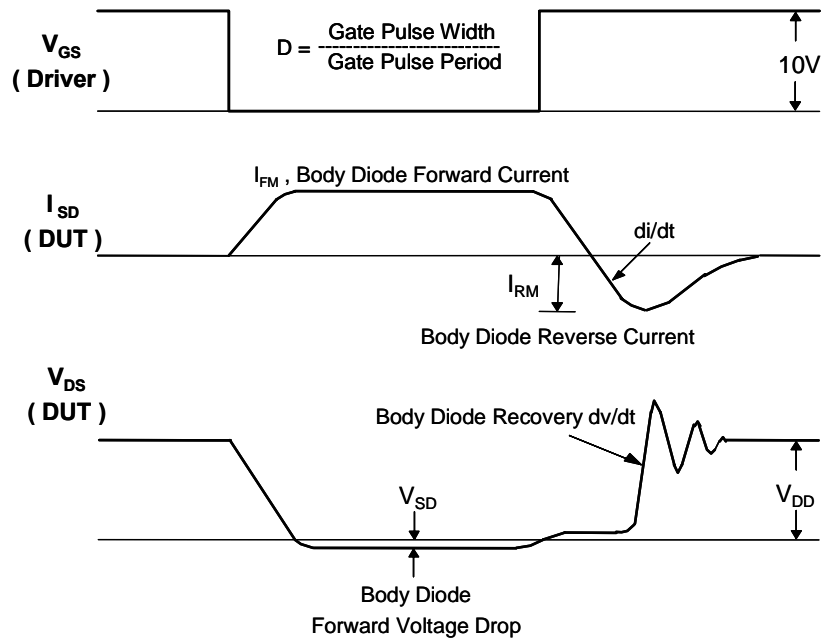
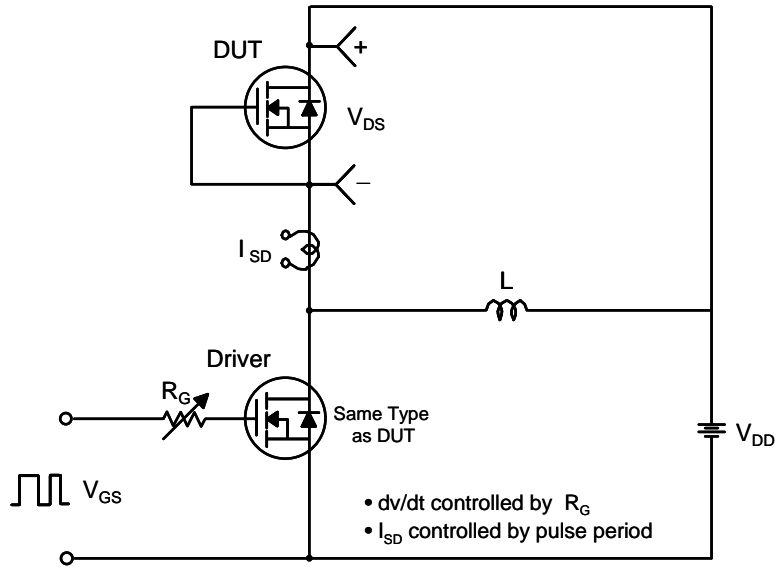
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

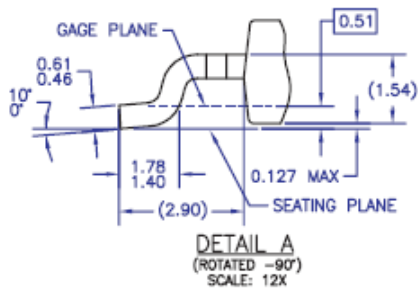
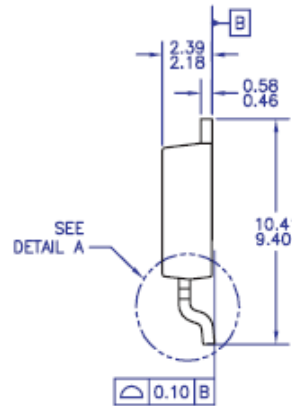
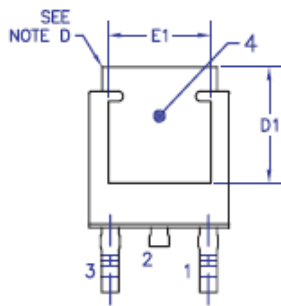
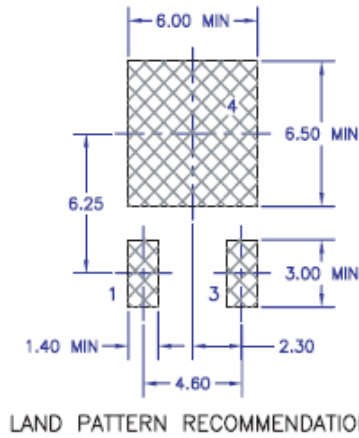
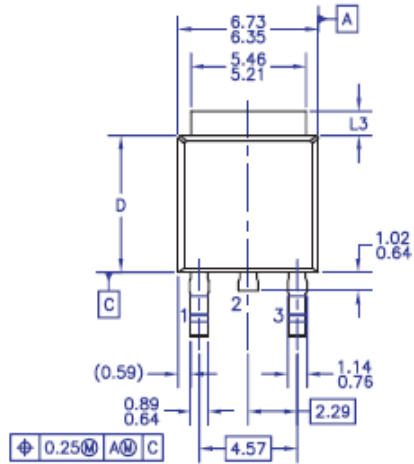


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

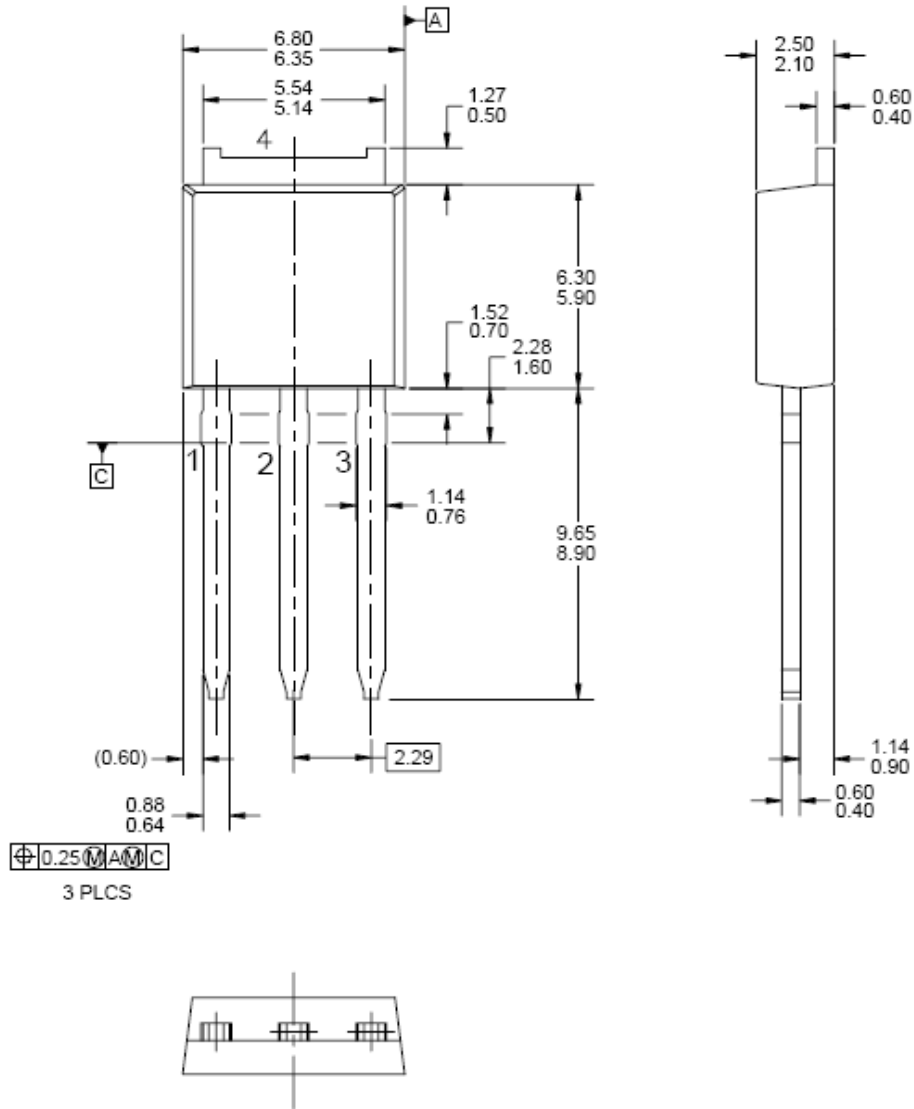
D - PAK



Dimensions in Millimeters

Mechanical Dimensions

I - PAK






Dimensions in Millimeters



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