

**256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM**

**FEATURES**

- Process Technology : 0.4µm Full CMOS
- Organization : 256Kx8
- Power Supply Voltage
  - KM68FV2000 Family : 3.0 ~ 3.6V
  - KM68FS2000 Family : 2.3 ~ 3.3V
  - KM68FR2000 Family : 1.8 ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 32-TSOP1-0820F

**GENERAL DESCRIPTION**

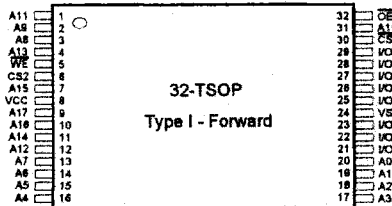
The KM68FV2000, KM68FS2000 and KM68FR2000 family is fabricated by SAMSUNG's advanced Full CMOS process technology. The family supports various operating temperature ranges and has various package types for user flexibility of system design. The family also supports low data retention voltage for battery back-up operation with low data retention current.

**PRODUCT FAMILY**

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I <sub>cc1</sub> , Max)	Operating (I <sub>cc2</sub> , Max)	
KM68FV2000	Commercial(0~70°C)	3.0~3.6V	70 <sup>1)</sup> /85@V <sub>cc</sub> =3.3±0.3V	10µA <sup>2)</sup>	60mA	32-TSOP1-F
KM68FS2000		2.3~3.3V	85@V <sub>cc</sub> =3.0±0.3V		55mA	
KM68FR2000		1.8~2.7V	120 <sup>1)</sup> /150@V <sub>cc</sub> =2.5±0.2V		30mA	
KM68FV2000I	Industrial(-40~85°C)	3.0~3.6V	70 <sup>1)</sup> /85@V <sub>cc</sub> =3.3±0.3V		60mA	
KM68FS2000I		2.3~3.3V	85@V <sub>cc</sub> =3.0±0.3V		55mA	
KM68FR2000I		1.8~2.7V	120 <sup>1)</sup> /150@V <sub>cc</sub> =2.5±0.2V		30mA	
			300 <sup>1)</sup> @V <sub>cc</sub> =2.0±0.2V		15mA	

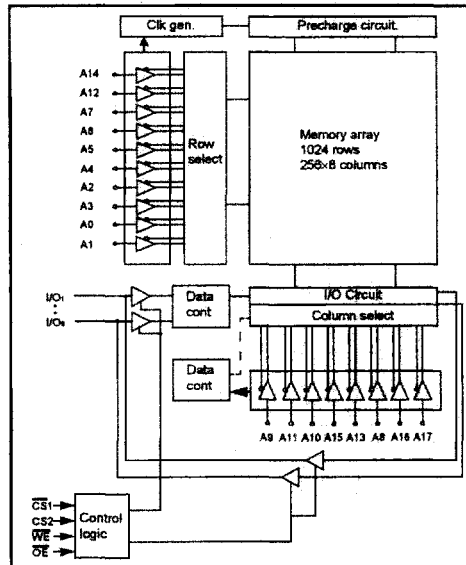
1. The parameter is measured with 30pF test load.  
 2. 2µA for super low power version with special handling.

**PIN DESCRIPTION**



Name	Function	Name	Function
A0~A17	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
CS1, CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable	N.C.	No Connection

**FUNCTIONAL BLOCK DIAGRAM**



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

**PRODUCT LIST**

Commercial Temperature Product (0-70°C)		Industrial Temperature Product (-40-85°C)	
Part Name	Function	Part Name	Function
KM68FV2000T-7	32-TSOP F, 70ns, 3.3V, LL	KM68FV2000TI-7	32-TSOP F, 70ns, 3.3V, LL
KM68FV2000T-8	32-TSOP F, 85ns, 3.3V, LL	KM68FV2000TI-8	32-TSOP F, 85ns, 3.3V, LL
KM68FS2000T-12	32-TSOP F, 120/85ns, 2.5/3.0V, LL	KM68FS2000TI-12	32-TSOP F, 120/85ns, 2.5/3.0V, LL
KM68FS2000T-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS2000TI-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL
KM68FR2000T-30	32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR2000TI-30	32-TSOP F, 300ns, 2.0/2.5V, LL

**FUNCTIONAL DESCRIPTION**

CS <sub>1</sub>	CS <sub>2</sub>	OE	WE	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disable	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be high or low states)

**ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>**

Item	Symbol	Rating	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to 3.6V <sup>2)</sup>	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.2 to 4.0V <sup>3)</sup>	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-55 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM68FV2000, KM68FS2000, KM68FR2000
		-40 to 85	°C	KM68FV2000I, KM68FS2000I, KM68FR2000I
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 5sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V<sub>IN</sub>/V<sub>OUT</sub> = -0.2 to 3.9V for KM68FV2000 Family.

3. Maximum V<sub>CC</sub> = -0.2 to 4.6V for KM68FV2000 Family.

2

**RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>**

Item	Symbol	Product	Min	Typ <sup>2)</sup>	Max	Unit
Supply voltage	Vcc	KM68FV2000 Family	3.0	3.3	3.6	V
		KM68FS2000 Family	2.3	2.5/3.0	3.3	
		KM68FR2000 Family	1.8	2.0/2.5	2.7	
Ground	Vss	All Family	0	0	0	V
Input high voltage	VIH	KM68FV2000 Family	Vcc=3.3±0.3V	-	Vcc+0.2 <sup>2)</sup>	V
		KM68FS2000 Family	Vcc=3.0±0.3V			
		KM68FR2000 Family	Vcc=2.5±0.2V			
Input low voltage	VIL	All Family	-0.2 <sup>3)</sup>	-	0.4	V

**Note**

- Commercial Product : TA=0 to 70°C, unless otherwise specified  
Industrial Product : TA=-40 to 85°C, unless otherwise specified
- Overshoot : Vcc + 1.0V in case of pulse width ≤20ns
- Undershoot : -1.0V in case of pulse width ≤20ns
- Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE<sup>1)</sup> (f=1MHz, TA=25°C)**

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	CIO	VIO=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

**DC AND OPERATING CHARACTERISTICS**

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	II	VIN=Vss to Vcc	-1	-	1	μA	
Output leakage current	ILO	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , VIO=Vss to Vcc	-1	-	1	μA	
Operating power supply current	ICC	IIO=0mA, $\overline{CS}_1=V_{IL}$ , $CS_2=V_{IH}$ , VIN=VIL or VIH, Read	-	-	10	mA	
Average operating current	ICC1	Cycle time=1/μs, 100% duty, IIO=0mA, $\overline{CS}_1 \leq 0.2V$ , $CS_2 \geq V_{cc}-0.2V$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{cc}-0.2V$	Read	-	-	10	mA
			Write	-	-	15	
			Vcc=3.3V@70ns	-	-	55 <sup>1)</sup>	
	ICC2	Cycle time=Min, 100% duty, IIO=0mA, $\overline{CS}_1=V_{IL}$ , $CS_2=V_{IH}$ , VIN=VIL or VIH	Vcc=2.7V@120ns	-	-	30	mA
			Vcc=2.2V@300ns	-	-	15	
Output low voltage	VOL	IOL	2.1mA at Vcc=3.0/3.3V	-	-	0.4	V
			0.5mA at Vcc=2.5V	-	-	0.4	
			0.33mA at Vcc=2.0V	-	-	0.4	
Output high voltage	VOH	IOH	-1.0mA at Vcc=3.0/3.3V	2.4	-	-	V
			-0.5mA at Vcc=2.5V	2.0	-	-	
			-0.44mA at Vcc=2.0V	1.6	-	-	
Standby Current(TTL)	ISB	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ , Other inputs=VIL or VIH	-	-	0.3	mA	
Standby Current(CMOS)	ISB1	$\overline{CS}_1 \geq V_{cc}-0.2V$ , $CS_2 \geq V_{cc}-0.2V$ or $CS_2 \leq 0.2V$ , Other inputs=0-Vcc	-	-	10 <sup>2)</sup>	μA	

1. The value is measured at Vcc=3.0±0.3V

- ICC2=60mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.

2. Super low power product = 2μA with special handling.

AC OPERATING CONDITIONS

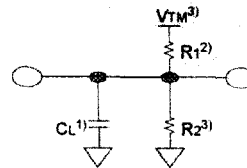
TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V  
 0.4 to 1.8V for Vcc=2.0V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V  
 1.1V for Vcc=2.5V  
 0.9V for Vcc=2.0V

Output load (See right) : CL=100pF+1TTL  
 CL=30pF+1TTL



- Including scope and jig capacitance
- R1=3070Ω, R2=3150Ω
- VTM = 2.8V for Vcc=3.0/3.3V  
 = 2.3V for Vcc=2.5V  
 = 1.8V for Vcc=2.0V

AC CHARACTERISTICS

(Commercial product : TA=0 to 70°C, Industrial product : TA=-40 to 85°C  
 KM68FV2000 Family : Vcc=3.0-3.6V, KM68FS2000 Family : Vcc=2.3-3.3V,  
 KM68FR2000 Family : Vcc=1.8-2.7V)

Parameter List	Symbol	Speed Bins										Units	
		70ns		85ns		120ns		150ns		300ns			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read	Read cycle time	tRC	70	-	85	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	120	-	150	-	300	ns
	Chip select to output	tCO1, tCO2	-	70	-	85	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	25	0	25	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	35	0	40	0	60	ns
Output hold from address change	tOH	10	-	15	-	15	-	15	-	30	-	ns	
Write	Write cycle time	tWC	70	-	85	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	50	-	60	-	120	-	ns
Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	ns	
End write to output low-Z	tOW	5	-	5	-	5	-	5	-	20	-	ns	

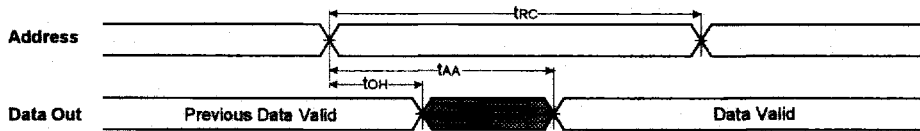
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	CS1≥Vcc-0.2V <sup>1)</sup>	1.5	-	3.6	V
Data retention current	IDR	Vcc=3.0V, CS1≥Vcc-0.2V <sup>1)</sup>	-	-	10 <sup>2)</sup>	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	trDR		tRC	-	-	

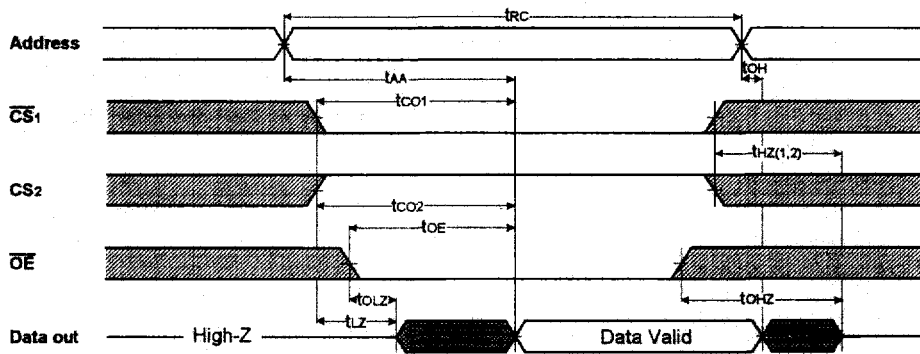
- CS1≥Vcc-0.2V, CS2≥Vcc-0.2V (CS1 controlled) or CS2≤0.2V (CS2 controlled)
- Super low power product = 2μA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



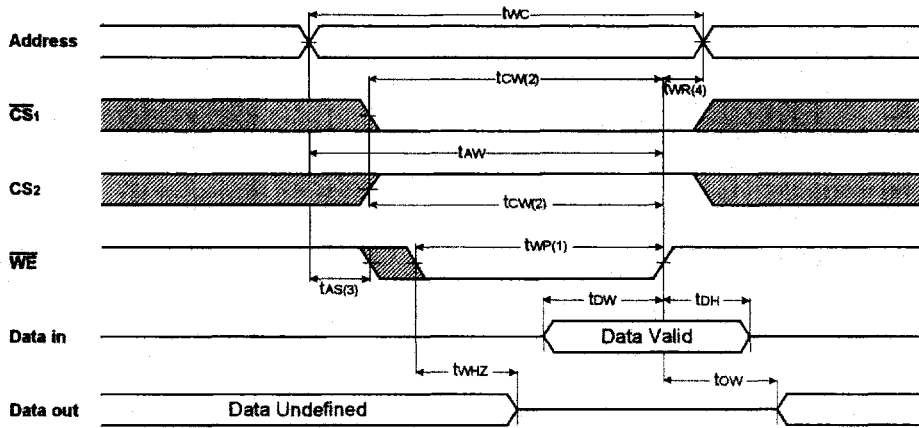
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



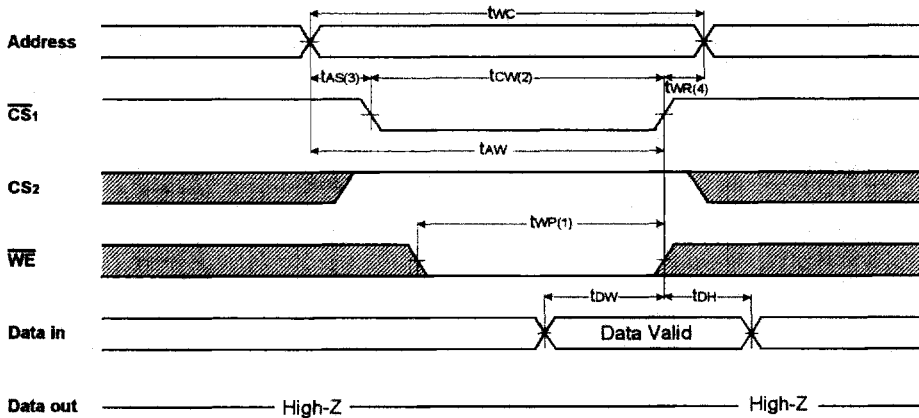
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)

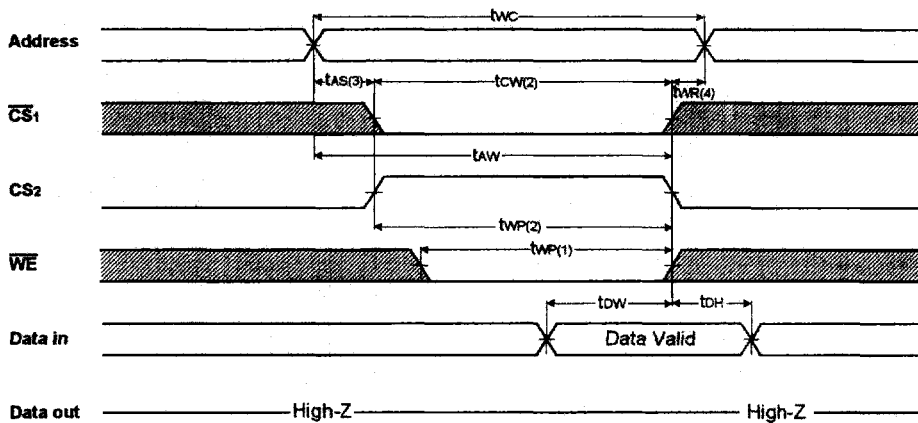


TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)



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**TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}_1$  Controlled)**

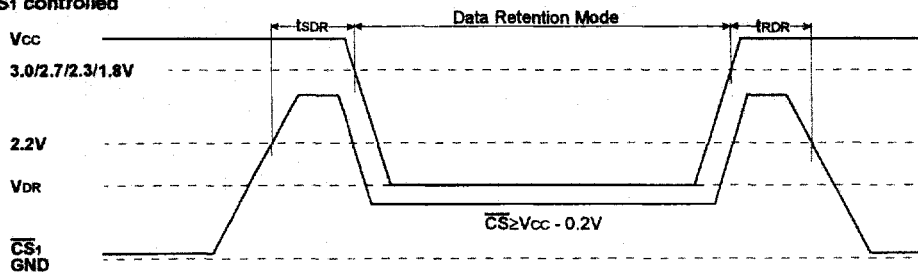


**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WC}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WP}$  is measured from the end of write to the address change.  $t_{WP(1)}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WP(2)}$  applied in case a write ends as  $CS_2$  going to low.

**DATA RETENTION WAVE FORM**

**$\overline{CS}_1$  controlled**



**$CS_2$  controlled**

