DS07-13736-1E

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16LX MB90360 Series

## MB90F362/T/S/TS, MB90362/T/S/TS, MB90F367/T/S/TS, MB90367/T/S/TS, MB90V340A-101, MB90V340A-102, MB90V340A-103, MB90V340A-104

## ■ DESCRIPTION

The MB90360-series with 1 channel FULL-CAN* interface and FLASH ROM is especially designed for automotive and other industrial applications. Its main feature is the on-board CAN Interfaces, which conform to Ver 2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35 µm CMOS technology, Fujitsu now offers on-chip FLASH-ROM program memory up to 64 Kbytes.

The power supply (3 V) is supplied to the internal MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction execution time from an external 4 MHz clock. Also, main and sub-clock can be monitored independently using the clock monitor function.

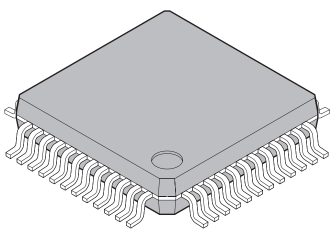
The unit features a 4 channel input capture unit 1 channel 16-bit free running timer, 2-channel LIN-UART, and 16-channel 8/10-bit A/D converter as the peripheral resource.

* : Controller Area Network (CAN) - License of Robert Bosch GmbH

Note : F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

## ■ PACKAGE

48-pin Plastic LQFP



(FPT-48P-M26)

FUJITSU

## ■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by 2 on oscillation clock and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz) .
  - Operation by sub-clock (up to 50 kHz : 100 kHz oscillation clock divided two) is allowed (devices without S-suffix only) .
  - Minimum execution time of instruction : 42 ns (when operating with 4-MHz oscillation clock and 6-time multiplied PLL clock) .
- **Clock monitor function (MB90x367x only)**
  - Main clock or sub-clock is monitored independently
  - Internal CR oscillation clock (100 kHz typical) can be used as sub-clock
- **Instruction system best suited to controller**
  - 16 Mbytes CPU memory space
  - 24-bit internal addressing
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions with sign and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  - 4-byte instruction queue
- **Powerful interrupt function**
  - Powerful 8-level, 34-condition interrupt feature
  - Up to 8 channel external interrupts are supported
- **Automatic data transfer function independent of CPU**
  - Expanded intelligent I/O service function ($EI^2OS$) : up to 16 channels
- **Low-power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Main timer mode (timebase timer mode that is transferred from main clock mode)
  - PLL timer mode (timebase timer mode that is transferred from PLL clock mode)
  - Watch mode (a mode that operates sub-clock and watch timer only, devices without S-suffix)
  - Stop mode (a mode that stops oscillation clock and sub-clock)
  - CPU blocking operation mode
- **Process**
  - CMOS technology
- **I/O port**
  - General-purpose input/output port (CMOS output)
    - 34 ports (devices without S-suffix)
    - 36 ports (devices with S-suffix)
- **Sub-clock pin (X0A and X1A)**
  - Provided (used for external oscillation), devices without S-suffix
  - Not provided (used with internal CR oscillation in sub-clock mode) , devices with S-suffix

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- **Timer**
  - Timebase timer, watch timer (device without S-suffix) , watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit × 2 channels or 16-bit × 2 channels
  - 16-bit reload timer : 2 channels
  - 16- bit input/output timer
    - 16-bit free run timer : 1 channel (FRT0 : ICU 0/1/2/3)
    - 16- bit input capture : (ICU) : 4 channels
- **Full-CAN interface : up to 1 channel**
  - Compliant with Ver 2.0A and Ver 2.0B CAN specifications
  - Flexible message buffering (mailbox and FIFO buffering can be mixed)
  - CAN wake-up function
- **UART (LIN/SCI) : up to 2 channels**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- **DTP/External interrupt : up to 8 channels, CAN wakeup : up to 1 channel**
  - Module for activation of expanded intelligent I/O service ($EI^2OS$) and generation of external interrupt by external input.
- **Delay interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter : 16 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time : 3 μs (at 24-MHz machine clock, including sampling time)
- **Program patch function**
  - Address matching detection for 6 address pointers.
- **Low voltage/CPU operation detection reset (devices with T-suffix)**
  - Detects low voltage (4.0 V ± 0.3 V) and resets automatically
  - Resets automatically when program is runaway and counter is not cleared within interval time (approx. 262 ms : external 4 MHz)
- **Capable of changing input voltage for port**
  - Automotive/CMOS-Schmitt (initial level is Automotive in single-chip mode)
- **FLASH memory security function**
  - Protects the content of FLASH memory (FLASH memory device only)

## ■ PRODUCT LINEUP

| Features | MB90362 | MB90362T | MB90362S | MB90362TS | MB90V340 A-101 | MB90V340 A-102 |
|---|---|---|---|---|---|---|
| CPU | $F^2MC$-16LX CPU | | | | | |
| System clock | PLL clock multiplier ( × 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns (4 MHz oscillation clock, PLL × 6) | | | | | |
| Sub-clock pin (X0A, X1A) | Yes | | No | | No | Yes |
| Clock monitor function | No | | | | | |
| ROM | MASK ROM, 64 Kbytes | | | | External | |
| RAM capacitance | 3 Kbytes | | | | 30 Kbytes | |
| CAN interface | 1 channel | | | | 3 channels | |
| Low voltage/CPU operation detection reset | No | Yes | No | Yes | No | |
| Package | LQFP-48P | | | | PGA-299C | |
| Emulator-specific power supply * | — | | | | Yes | |
| Corresponding EVA product | MB90V340A-102 | | MB90V340A-101 | | — | |

* : It is setting of Jumper switch (TOOL $V_{CC}$) when emulator (MB2147-01) is used. Please refer to the Emulator hardware manual for the details.

| Features | MB90F362 | MB90F362T | MB90F362S | MB90F362TS |
|---|---|---|---|---|
| CPU | $F^2MC$-16LX CPU | | | |
| System clock | PLL clock multiplier<br>( × 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns<br>(4 MHz oscillation clock, PLL × 6) | | | |
| Sub-clock pin (X0A, X1A) | Yes | | No | |
| Clock monitor function | No | | | |
| ROM | Flash memory, 64 Kbytes | | | |
| RAM capacitance | 3 Kbytes | | | |
| CAN interface | 1 channel | | | |
| Low voltage/CPU operation detection reset | No | Yes | No | Yes |
| Package | LQFP-48P | | | |
| Corresponding EVA product | MB90V340A-102 | | MB90V340A-101 | |

| Features | MB90367 | MB90367T | MB90367S | MB90367TS | MB90V340 A-103 | MB90V340 A-104 |
|---|---|---|---|---|---|---|
| CPU | F²MC-16LX CPU | | | | | |
| System clock | PLL clock multiplier ( × 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns (4 MHz oscillation clock, PLL × 6) | | | | | |
| Sub-clock pin (X0A, X1A) | Yes | | No<br>(internal CR oscillation can be used as sub-clock) | | | Yes |
| Clock monitor function | Yes | | | | | |
| ROM | MASK ROM, 64 Kbytes | | | | External | |
| RAM capacitance | 3 Kbytes | | | | 30 Kbytes | |
| CAN interface | 1 channel | | | | 3 channels | |
| Low voltage/CPU operation detection reset | No | Yes | No | Yes | No | |
| Package | LQFP-48P | | | | PGA-299C | |
| Emulator-specific power supply * | — | | | | Yes | |
| Corresponding EVA product | MB90V340A-104 | | MB90V340A-103 | | — | |

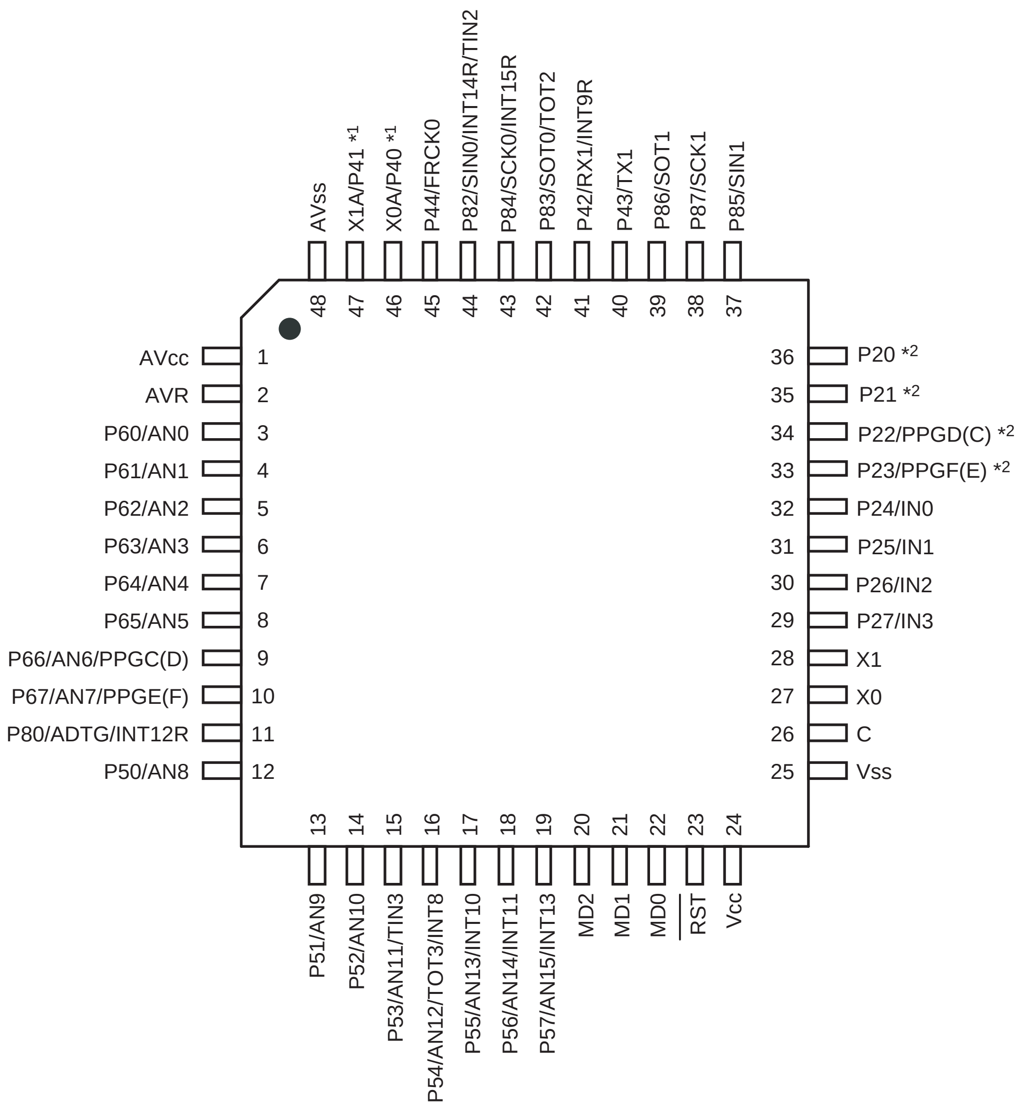
* : It is setting of Jumper switch (TOOL $V_{CC}$) when emulator (MB2147-01) is used. Please refer to the Emulator hardware manual for the details.

| Features | MB90F367 | MB90F367T | MB90F367S | MB90F367TS |
|---|---|---|---|---|
| CPU | F²MC-16LX CPU | | | |
| System clock | PLL clock multiplier<br>( × 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns<br>(4 MHz oscillation clock, PLL × 6) | | | |
| Sub-clock pin (X0A, X1A) | Yes | | No<br>(internal CR oscillation can be used as sub-clock) | |
| Clock monitor function | Yes | | | |
| ROM | Flash memory, 64 Kbytes | | | |
| RAM capacitance | 3 Kbytes | | | |
| CAN interface | 1 channel | | | |
| Low voltage/CPU operation detection reset | No | Yes | No | Yes |
| Package | LQFP-48P | | | |
| Corresponding EVA product | MB90V340A-104 | | MB90V340A-103 | |

## ■ PIN ASSIGNMENT

**• MB90F362/T/S/TS, MB90362/T/S/TS, MB90F367/T/S/TS, MB90367/T/S/TS**

(TOP VIEW)
(LQFP-48P)

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*1 : MB90F362/T, MB90362/T, MB90F367/T, MB90367/T : X0A, X1A
MB90F362S/TS, MB90362S/TS, MB90F367S/TS, MB90367S/TS : P40, P41

*2 : High current port

## ■ PIN DESCRIPTION

| Pin No. LQFP-48P* | Pin name | Circuit type | Function |
|---|---|---|---|
| 1 | $AV_{CC}$ | I | $V_{CC}$ power input pin for analog circuit. |
| 2 | AVR | — | Power (Vref+) input pin for A/D converter.<br>It should be below $V_{CC}$. |
| 3 to 8 | P60 to P65 | H | General-purpose I/O port. |
| | AN0 to AN5 | | Analog input pin for A/D converter. |
| 9, 10 | P66, P67 | H | General-purpose I/O port. |
| | AN6, AN7 | | Analog input pin for A/D converter. |
| | PPGC (D) ,<br>PPGE (F) | | Output pin for PPG. |
| 11 | P80 | F | General-purpose I/O port. |
| | ADTG | | Trigger input pin for A/D converter. |
| | INT12R | | External interrupt request input pin for INT12. |
| 12 to 14 | P50 to P52 | H | General-purpose I/O port. (P50 has different I/O circuit type from MB90V340A.) |
| | AN8 to AN10 | | Analog input pin for A/D converter. |
| 15 | P53 | H | General-purpose I/O port. |
| | AN11 | | Analog input pin for A/D converter. |
| | TIN3 | | Event input pin for reload timer 3. |
| 16 | P54 | H | General-purpose I/O port. |
| | AN12 | | Analog input pin for A/D converter. |
| | TOT3 | | Output pin for reload timer 3 |
| | INT8 | | External interrupt request input pin for INT8. |
| 17 to 19 | P55 to P57 | H | General-purpose I/O port. |
| | AN13 to AN15 | | Analog input pin for A/D converter. |
| | INT10, INT11,<br>INT13 | | External interrupt request input pin for INT10, INT11, INT13. |
| 20 | MD2 | D | Input pin for operation mode specification. |
| 21, 22 | MD1,<br>MD0 | C | Input pin for operation mode specification. |
| 23 | $\overline{RST}$ | E | Reset input. |
| 24 | $V_{CC}$ | — | Power input pin (3.5 V to 5.5 V) . |
| 25 | $V_{SS}$ | — | Power input pin (0 V) . |
| 26 | C | I | Power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 µF ceramic capacitor. |

* : FPT-48P-M26

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| Pin No. LQFP-48P* | Pin name | Circuit type | Function |
|---|---|---|---|
| 27 | X0 | A | Oscillation input pin. |
| 28 | X1 | | Oscillation output pin. |
| 29 to 32 | P27 to P24 | G | General-purpose I/O port.<br>The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | IN3 to IN0 | | Event input pin for input capture 0 to 3. |
| 33, 34 | P23, P22 | J | General-purpose I/O port.<br>The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.<br>High current output port. |
| | PPGF (E) ,<br>PPGD (C) | | Output pin for PPG. |
| 35, 36 | P21, P20 | J | General-purpose I/O port.<br>The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.<br>High current output port. |
| 37 | P85 | K | General-purpose I/O port. |
| | SIN1 | | Serial data input pin for UART1. |
| 38 | P87 | F | General-purpose I/O port. |
| | SCK1 | | Clock I/O pin for UART1. |
| 39 | P86 | F | General-purpose I/O port. |
| | SOT1 | | Serial data output pin for UART1. |
| 40 | P43 | F | General-purpose I/O port. |
| | TX1 | | TX output pin for CAN1 interface. |
| 41 | P42 | F | General-purpose I/O port. |
| | RX1 | | RX input pin for CAN1 interface. |
| | INT9R | | External interrupt request input pin for INT9 (Sub) . |
| 42 | P83 | F | General-purpose I/O port. |
| | SOT0 | | Serial data output pin for UART0. |
| | TOT2 | | Output pin for reload timer 2 |
| 43 | P84 | F | General-purpose I/O port. |
| | SCK0 | | Clock I/O pin for UART0. |
| | INT15R | | External interrupt request input pin for INT15. |

* : FPT-48P-M26

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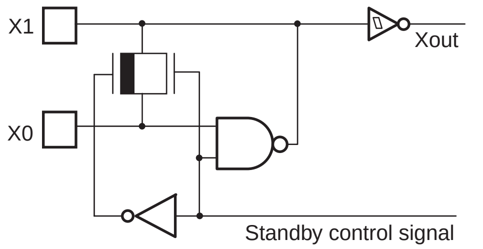
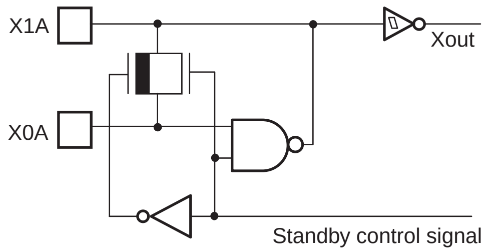
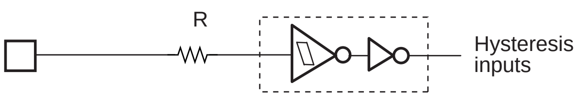
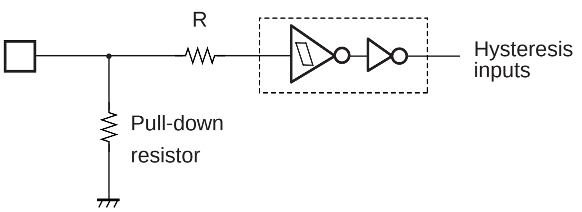
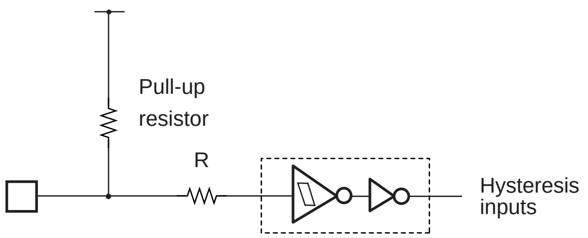
| Pin No. LQFP-48P* | Pin name | Circuit type | Function |
|---|---|---|---|
| 44 | P82 | K | General-purpose I/O port. |
| | SIN0 | | Serial data input pin for UART0. |
| | INT14R | | External interrupt request input pin for INT14. |
| | TIN2 | | Event input pin for reload timer 2. |
| 45 | P44 | F | General-purpose I/O port. (Different I/O circuit type from MB90V340A.) |
| | FRCK0 | | Free-run timer 0 clock pin. |
| 46, 47 | P40, P41 | F | General-purpose I/O port. (Devices with S-suffix and MB90V340A-101/103 only.) |
| | X0A, X1A | B | Oscillation input pin for sub-clock. (Devices without S-suffix and MB90V340A-102/104 only.) |
| 48 | $AV_{SS}$ | I | $V_{SS}$ power input pin for analog circuit. |

* : FPT-48P-M26

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>• High-speed oscillation feedback resistor = approx. 1 MΩ |
| B |  | Oscillation circuit<br>• Low-speed oscillation feedback resistor = approx. 10 MΩ |
| C |  | Mask ROM device :<br>• CMOS hysteresis input pin<br><br>Flash device :<br>• CMOS input pin |
| D |  | Mask ROM device :<br>• CMOS hysteresis input pin<br>• Pull-down resistor value : approx. 50 kΩ<br><br>Flash device :<br>• CMOS input pin<br>• No Pull-down |
| E |  | CMOS hysteresis input pin<br>• Pull-up resistor value : approx. 50 kΩ |

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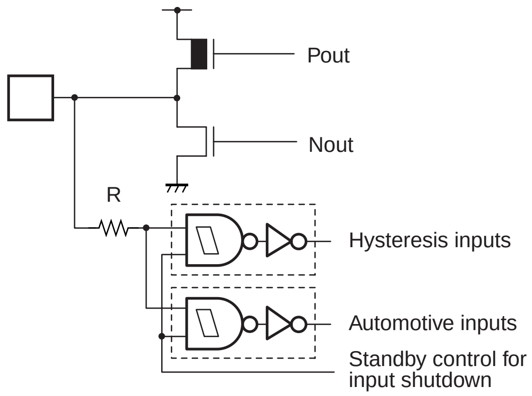
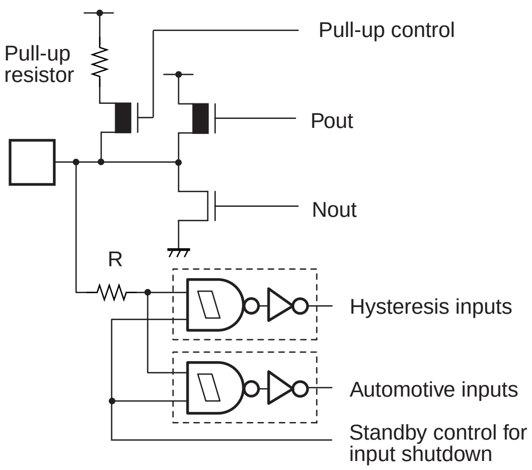
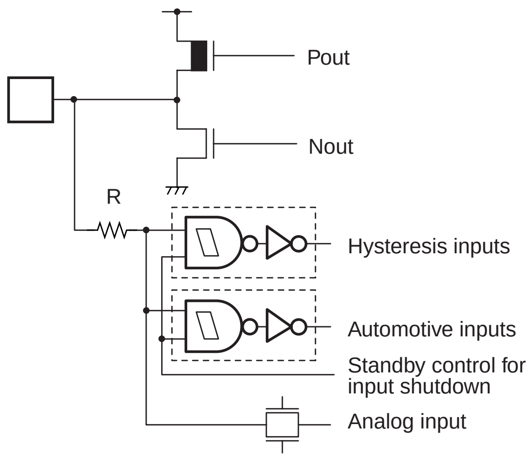
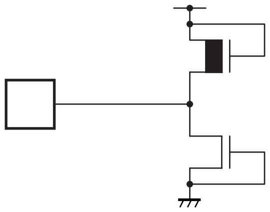
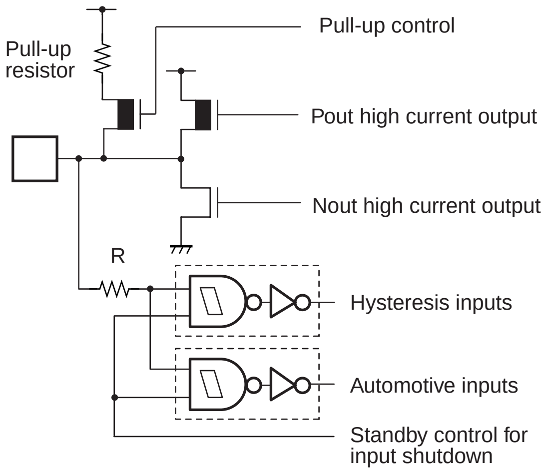
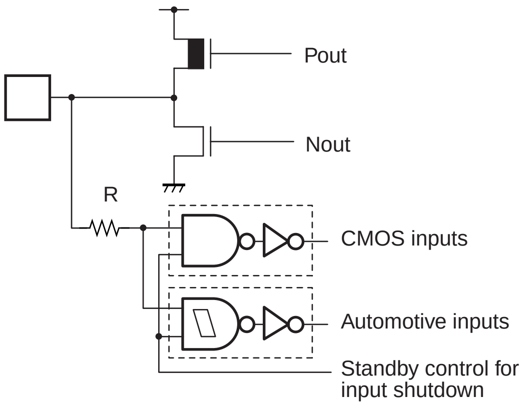
| Type | Circuit | Remarks |
|---|---|---|
| F |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function) |
| G |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• Settable pull-up resistor : approx. 50 kΩ |
| H |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• A/D analog input |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| I |  | • Power supply input protection circuit |
| J |  | • CMOS level output ($I_{OL}$ = 20 mA, $I_{OH}$ = –14 mA)<br>• CMOS hysteresis inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• Settable pull-up resistor : approx. 50 kΩ |
| K |  | • CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS input (With standby-time input shutdown function)<br>• Automotive input (With standby-time input shutdown function) |

## ■ HANDLING DEVICES

**Special care is required for the following when handling the device :**

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Precautions for when not using a sub-clock signal
- Notes on during operation of PLL clock mode
- Power supply pins ($V_{CC}/V_{SS}$)
- Pull-up/down resistors
- Crystal oscillator circuit
- Turning-on sequence of power supply to A/D converter and analog inputs
- Connection of unused pins of A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Initialization
- Notes on using CAN Function
- Flash security function
- Correspondence with +105 °C or more

### 1. Preventing latch-up

**CMOS IC chips may suffer latch-up under the following conditions** :

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ and $V_{SS}$.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Use meticulous care not to exceed the rating.

For the same reason, also be careful not to let the analog power-supply voltage ($AV_{CC}$, AVR) exceed the digital power-supply voltage.

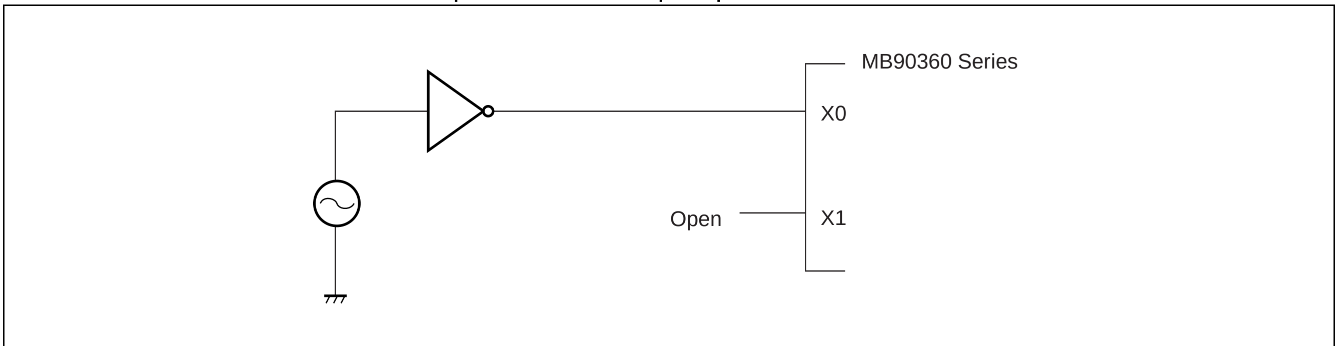
### 2. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore, they must be pulled up or pulled down through resistors. In this case, those resistors should be more than 2 kΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### 3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



4. **Precautions for when not using a sub-clock signal**

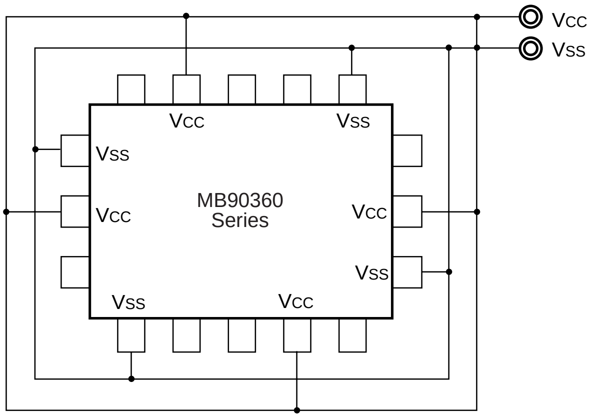
If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin and leave the X1A pin open.

5. **Notes on during operation of PLL clock mode**

If the PLL clock mode is selected, the microcontroller attempts to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

6. **Power supply pins ($V_{CC}$/$V_{SS}$)**

- If there are multiple $V_{CC}$ and $V_{SS}$ pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the $V_{CC}$ and $V_{SS}$ pins to the power supply and ground externally.
- Connect $V_{CC}$ and $V_{SS}$ to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between $V_{CC}$ and $V_{SS}$ in the vicinity of $V_{CC}$ and $V_{SS}$ pins of the device.




7. **Pull-up/down resistors**

The MB90360 Series does not support internal pull-up/down resistors (Port 2 : built-in pull-up resistors) . Use external components where needed.

8. **Crystal oscillator circuit**

Noises around X0 or X1 pin may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

9. **Turning-on sequence of power supply to A/D converter and analog inputs**

Make sure to turn on the A/D converter power supply ($AV_{CC}$ and AVR) and analog inputs (AN0 to AN15) after turning-on the digital power supply ($V_{CC}$) .

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable) .

### 10. Connection of unused pins of A/D converter if A/D converter is used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$.

### 11. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V)

### 12. Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified $V_{CC}$ power supply voltage operating guarantee range. Therefore, the $V_{CC}$ power supply voltage should be stabilized.

For reference, the power supply voltage should be controlled so that $V_{CC}$ ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard $V_{CC}$ power supply voltage and the coefficient of transient fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

### 13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

### 14. Notes on using CAN function

To use CAN function, please set '1' to DIRECT bit of CAN direct mode register (CDMR) .
If DIRECT bit is set to '0' (initial value) , wait states will be performed when accessing CAN registers.

Note : Please refer to Hardware Manual of MB90360 series for detail of CAN Direct Mode Register.

### 15. Flash security function

The security bit is located in the area of the flash memory.
If protection code $01_H$ is written in the security bit, the flash memory is in the protected state by security.
Therefore, please do not write $01_H$ in this address if you do not use the security function.
Please refer to following table for the address of the security bit.

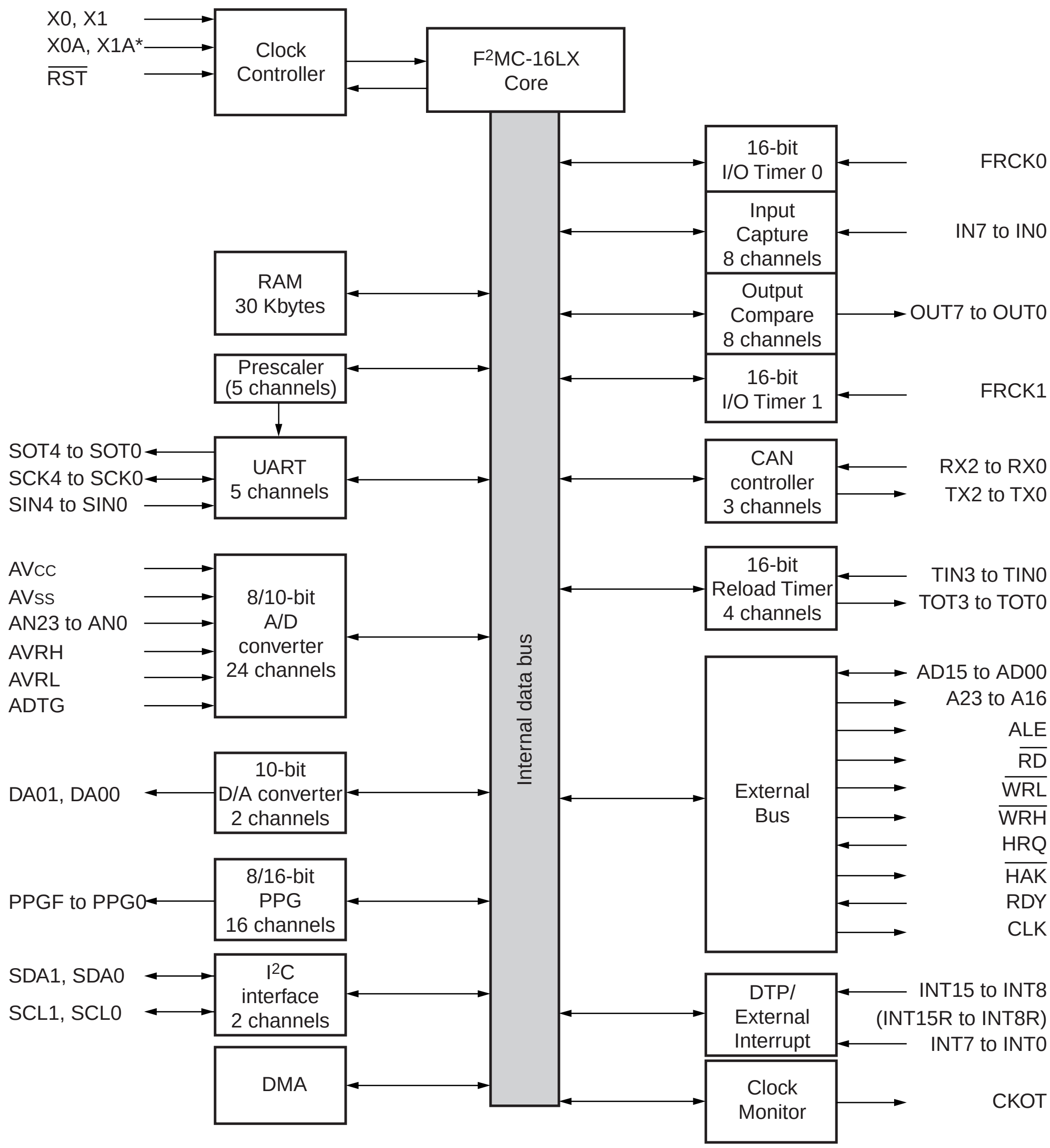
| | Flash memory size | Address for security bit |
|---|---|---|
| MB90F362<br>MB90F362S<br>MB90F362T<br>MB90F362TS<br>MB90F367<br>MB90F367S<br>MB90F367T<br>MB90F367TS | Embedded 512 Kbit Flash Memory | $FF0001_H$ |

### 16. Correspondence with +105 °C or more

If used exceeding $T_A = +105$ °C, please contact Fujitsu for reliability limitations.

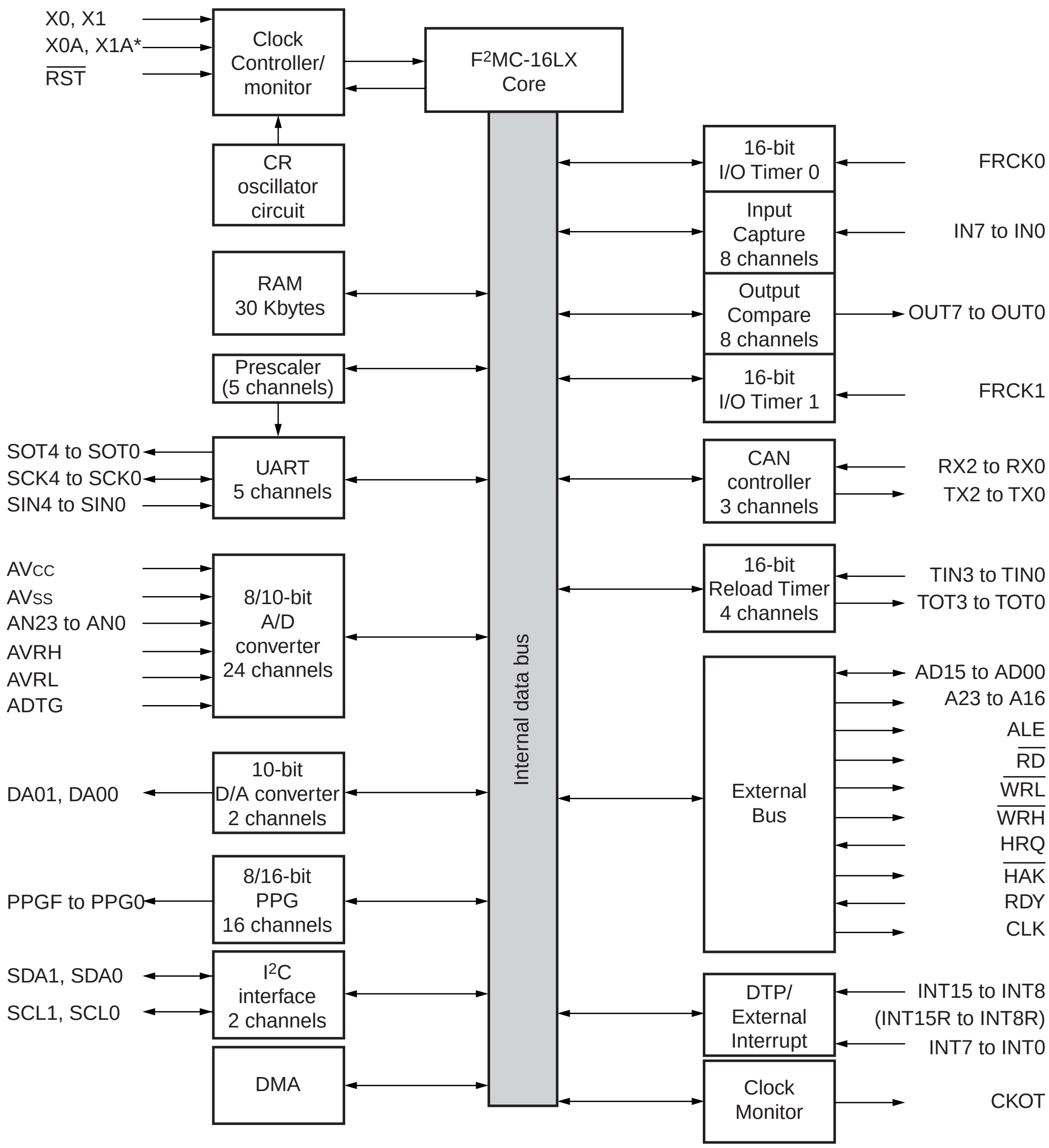
## ■ BLOCK DIAGRAMS

• **MB90V340A-101/102**



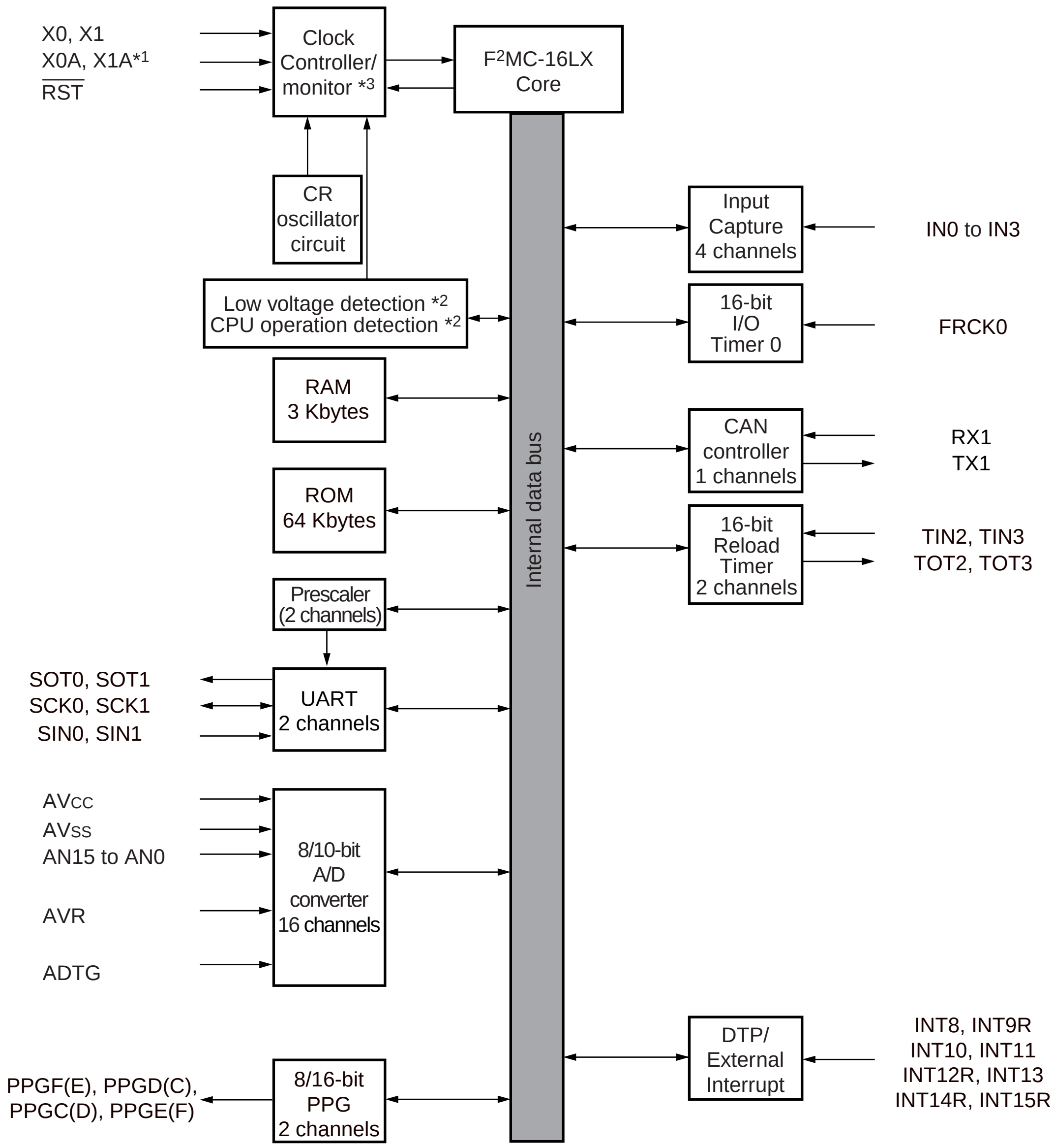

* : Only for MB90V340A-102

• **MB90V340A-103/104**



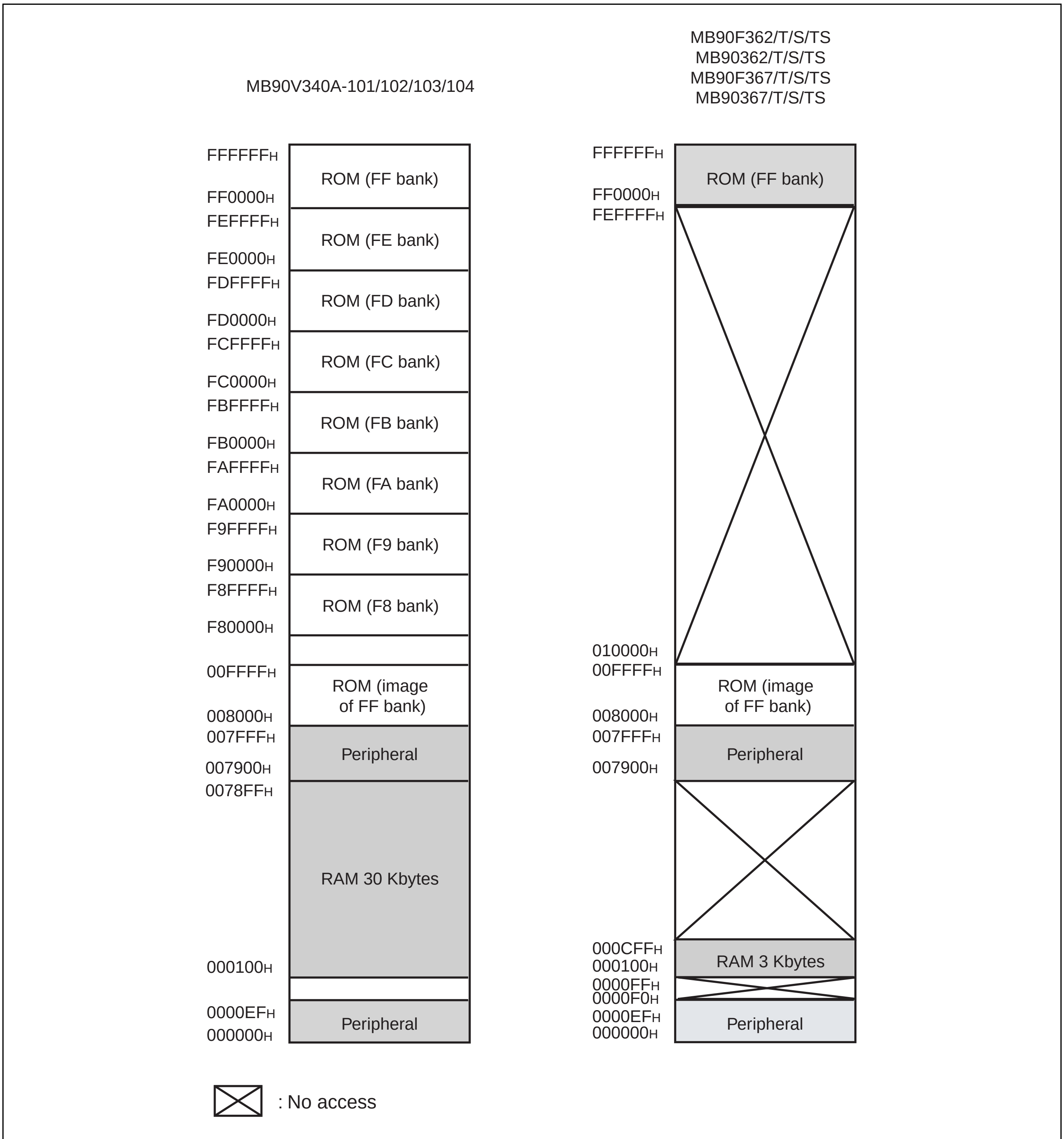

* : Only for MB90V340A-104

• **MB90F362/T/S/TS, MB90362/T/S/TS, MB90F367/T/S/TS, MB90367/T/S/TS**




*1 : Only for devices without S-suffix
*2 : Only for devices with T-suffix
*3 : CR oscillation circuit/clock monitor correspond to MB90F367/T/S/TS and MB90367/T/S/TS only.

## ■ MEMORY MAP




Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referred without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

## ■ I/O MAP

**(Address : 000000H-0000FFH)**

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000000H, 000001H | Reserved | | | | |
| 000002H | Port 2 Data Register | PDR2 | R/W | Port 2 | XXXXXXXXB |
| 000003H | Reserved | | | | |
| 000004H | Port 4 Data Register | PDR4 | R/W | Port 4 | XXXXXXXXB |
| 000005H | Port 5 Data Register | PDR5 | R/W | Port 5 | XXXXXXXXB |
| 000006H | Port 6 Data Register | PDR6 | R/W | Port 6 | XXXXXXXXB |
| 000007H | Reserved | | | | |
| 000008H | Port 8 Data Register | PDR8 | R/W | Port 8 | XXXXXXXXB |
| 000009H, 00000AH | Reserved | | | | |
| 00000BH | Port 5 Analog Input Enable Register | ADER5 | R/W | Port 5, A/D | 11111111B |
| 00000CH | Port 6 Analog Input Enable Register | ADER6 | R/W | Port 6, A/D | 11111111B |
| 00000DH | Reserved | | | | |
| 00000EH | Input Level Select Register | ILSR0 | R/W | Ports | XXXX0XXXB |
| 00000FH | Input Level Select Register | ILSR1 | R/W | Ports | XXXXXXXXB |
| 000010H, 000011H | Reserved | | | | |
| 000012H | Port 2 Direction Register | DDR2 | R/W | Port 2 | 00000000B |
| 000013H | Reserved | | | | |
| 000014H | Port 4 Direction Register | DDR4 | R/W | Port 4 | XXX00000B |
| 000015H | Port 5 Direction Register | DDR5 | R/W | Port 5 | 00000000B |
| 000016H | Port 6 Direction Register | DDR6 | R/W | Port 6 | 00000000B |
| 000017H | Reserved | | | | |
| 000018H | Port 8 Direction Register | DDR8 | R/W | Port 8 | 000000X0B |
| 000019H | Reserved | | | | |
| 00001AH | Port A Direction Register | DDRA | W | Port A | XXX00XXXB |
| 00001BH to 00001DH | Reserved | | | | |
| 00001EH | Port 2 Pull-up Control Register | PUCR2 | R/W | Port 2 | 00000000B |
| 00001FH | Reserved | | | | |

*(Continued)*

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000020H | Serial Mode Register 0 | SMR0 | W, R/W | UART0 | 00000000B |
| 000021H | Serial Control Register 0 | SCR0 | W, R/W | | 00000000B |
| 000022H | Reception/Transmission Data Register 0 | RDR0/ TDR0 | R/W | | 00000000B |
| 000023H | Serial Status Register 0 | SSR0 | R, R/W | | 00001000B |
| 000024H | Extended Communication Control Register 0 | ECCR0 | R, W, R/W | | 000000XXB |
| 000025H | Extended Status/Control Register 0 | ESCR0 | R/W | | 00000100B |
| 000026H | Baud Rate Generator Register 00 | BGR00 | R/W, R | | 00000000B |
| 000027H | Baud Rate Generator Register 01 | BGR01 | R/W, R | | 00000000B |
| 000028H | Serial Mode Register 1 | SMR1 | W, R/W | UART1 | 00000000B |
| 000029H | Serial Control Register 1 | SCR1 | W, R/W | | 00000000B |
| 00002AH | Reception/Transmission Data Register 1 | RDR1/ TDR1 | R/W | | 00000000B |
| 00002BH | Serial Status Register 1 | SSR1 | R, R/W | | 00001000B |
| 00002CH | Extended Communication Control Register 1 | ECCR1 | R, W, R/W | | 000000XXB |
| 00002DH | Extended Status/Control Register 1 | ESCR1 | R/W | | 00000100B |
| 00002EH | Baud Rate Generator Register 10 | BGR10 | R/W, R | | 00000000B |
| 00002FH | Baud Rate Generator Register 11 | BGR11 | R/W, R | | 00000000B |
| 000030H to 00003AH | Reserved | | | | |
| 00003BH | Address Detect Control Register 1 | PACSR1 | R/W | Address Match Detection 1 | 00000000B |
| 00003CH to 000047H | Reserved | | | | |
| 000048H | PPG C Operation Mode Control Register | PPGCC | W, R/W | 16-bit PPG C/D | 0X000XX1B |
| 000049H | PPG D Operation Mode Control Register | PPGCD | W, R/W | | 0X000001B |
| 00004AH | PPG C/PPG D Count Clock Select Register | PPGCD | R/W | | 000000X0B |
| 00004BH | Reserved | | | | |
| 00004CH | PPG E Operation Mode Control Register | PPGCE | W, R/W | 16-bit PPG E/F | 0X000XX1B |
| 00004DH | PPG F Operation Mode Control Register | PPGCF | W, R/W | | 0X000001B |
| 00004EH | PPG E/PPG F Count Clock Select Register | PPGEF | R/W | | 000000X0B |
| 00004FH | Reserved | | | | |

*(Continued)*

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 000050H | Input Capture Control Status 0/1 | ICS01 | R/W | Input Capture 0/1 | 00000000B |
| 000051H | Input Capture Edge 0/1 | ICE01 | R/W, R | | XXX0X0XXB |
| 000052H | Input Capture Control Status 2/3 | ICS23 | R/W | Input Capture 2/3 | 00000000B |
| 000053H | Input Capture Edge 2/3 | ICE23 | R | | XXXXXXXXB |
| 000054H to 000063H | Reserved | | | | |
| 000064H | Timer Control Status 2 | TMCSR2 | R/W | 16-bit Reload Timer 2 | 00000000B |
| 000065H | Timer Control Status 2 | TMCSR2 | R/W | | XXXX0000B |
| 000066H | Timer Control Status 3 | TMCSR3 | R/W | 16-bit Reload Timer 3 | 00000000B |
| 000067H | Timer Control Status 3 | TMCSR3 | R/W | | XXXX0000B |
| 000068H | A/D Control Status 0 | ADCS0 | R/W | A/D Converter | 000XXXX0B |
| 000069H | A/D Control Status 1 | ADCS1 | R/W, W | | 0000000XB |
| 00006AH | A/D Data 0 | ADCR0 | R | | 00000000B |
| 00006BH | A/D Data 1 | ADCR1 | R | | XXXXXX00B |
| 00006CH | ADC Setting 0 | ADSR0 | R/W | | 00000000B |
| 00006DH | ADC Setting 1 | ADSR1 | R/W | | 00000000B |
| 00006EH | Low Voltage/CPU Operation Detection Reset Control Register | LVRC | R/W, W | Low voltage/CPU operation detection reset | 00111000B |
| 00006FH | ROM Mirror Function Select | ROMM | W | ROM Mirror | XXXXXXX1B |
| 000070H to 00007FH | Reserved | | | | |
| 000080H to 00008FH | Reserved for CAN Interface 1. Refer to "■ CAN CONTROLLERS" | | | | |
| 000090H to 00009DH | Reserved | | | | |
| 00009EH | Address Detect Control Register 0 | PACSR0 | R/W | Address Match Detection 0 | 00000000B |
| 00009FH | Delayed Interrupt/Release Register | DIRR | R/W | Delayed Interrupt generation module | XXXXXXX0B |
| 0000A0H | Low-power Consumption Mode Control Register | LPMCR | W, R/W | Low-Power consumption Control Circuit | 00011000B |
| 0000A1H | Clock Selection Register | CKSCR | R, R/W | Low-Power consumption Control Circuit | 11111100B |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000A2H to 0000A7H | Reserved | | | | |
| 0000A8H | Watchdog Control Register | WDTC | R, W | Watchdog Timer | XXXXX111B |
| 0000A9H | Timebase Timer Control Register | TBTC | W, R/W | Timebase Timer | 1XX00100B |
| 0000AAH | Watch Timer Control register | WTC | R, R/W | Watch Timer | 1X001000B |
| 0000ABH to 0000ADH | Reserved | | | | |
| 0000AEH | Flash Control Status (Flash Devices only. Otherwise reserved) | FMCS | R, R/W | Flash Memory | 000X0000B |
| 0000AFH | Reserved | | | | |
| 0000B0H | Interrupt Control Register 00 | ICR00 | W, R/W | Interrupt Control | 00000111B |
| 0000B1H | Interrupt Control Register 01 | ICR01 | W, R/W | | 00000111B |
| 0000B2H | Interrupt Control Register 02 | ICR02 | W, R/W | | 00000111B |
| 0000B3H | Interrupt Control Register 03 | ICR03 | W, R/W | | 00000111B |
| 0000B4H | Interrupt Control Register 04 | ICR04 | W, R/W | | 00000111B |
| 0000B5H | Interrupt Control Register 05 | ICR05 | W, R/W | | 00000111B |
| 0000B6H | Interrupt Control Register 06 | ICR06 | W, R/W | | 00000111B |
| 0000B7H | Interrupt Control Register 07 | ICR07 | W, R/W | | 00000111B |
| 0000B8H | Interrupt Control Register 08 | ICR08 | W, R/W | | 00000111B |
| 0000B9H | Interrupt Control Register 09 | ICR09 | W, R/W | | 00000111B |
| 0000BAH | Interrupt Control Register 10 | ICR10 | W, R/W | | 00000111B |
| 0000BBH | Interrupt Control Register 11 | ICR11 | W, R/W | | 00000111B |
| 0000BCH | Interrupt Control Register 12 | ICR12 | W, R/W | | 00000111B |
| 0000BDH | Interrupt Control Register 13 | ICR13 | W, R/W | | 00000111B |
| 0000BEH | Interrupt Control Register 14 | ICR14 | W, R/W | | 00000111B |
| 0000BFH | Interrupt Control Register 15 | ICR15 | W, R/W | | 00000111B |
| 0000C0H to 0000C9H | Reserved | | | | |
| 0000CAH | External Interrupt Enable 1 | ENIR1 | R/W | External Interrupt 1 | 00000000B |
| 0000CBH | External Interrupt Source 1 | EIRR1 | R/W | | XXXXXXXXB |
| 0000CCH | Detection Level Setting 1 | ELVR1 | R/W | | 00000000B |
| 0000CDH | | | | | 00000000B |
| 0000CEH | External Interrupt Source Select | EISSR | R/W | | 00000000B |

*(Continued)*

*(Continued)*

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $0000CF_H$ | PLL/Subclock Control Register | PSCCR | W | PLL | $XXXX0000_B$ |
| $0000D0_H$ to $0000FF_H$ | Reserved | | | | |

**(Address : 7900H-7FFFH)**

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7900H to 7917H | Reserved | | | | |
| 7918H | Reload Register LC | PRLLC | R/W | 16-bit PPG C/D | XXXXXXXXB |
| 7919H | Reload Register HC | PRLHC | R/W | | XXXXXXXXB |
| 791AH | Reload Register LD | PRLLD | R/W | | XXXXXXXXB |
| 791BH | Reload Register HD | PRLHD | R/W | | XXXXXXXXB |
| 791CH | Reload Register LE | PRLLE | R/W | 16-bit PPG E/F | XXXXXXXXB |
| 791DH | Reload Register HE | PRLHE | R/W | | XXXXXXXXB |
| 791EH | Reload Register LF | PRLLF | R/W | | XXXXXXXXB |
| 791FH | Reload Register HF | PRLHF | R/W | | XXXXXXXXB |
| 7920H | Input Capture 0 | IPCP0 | R | Input Capture 0/1 | XXXXXXXXB |
| 7921H | Input Capture 0 | IPCP0 | R | | XXXXXXXXB |
| 7922H | Input Capture 1 | IPCP1 | R | | XXXXXXXXB |
| 7923H | Input Capture 1 | IPCP1 | R | | XXXXXXXXB |
| 7924H | Input Capture 2 | IPCP2 | R | Input Capture 2/3 | XXXXXXXXB |
| 7925H | Input Capture 2 | IPCP2 | R | | XXXXXXXXB |
| 7926H | Input Capture 3 | IPCP3 | R | | XXXXXXXXB |
| 7927H | Input Capture 3 | IPCP3 | R | | XXXXXXXXB |
| 7928H to 793FH | Reserved | | | | |
| 7940H | Timer Data 0 | TCDT0 | R/W | I/O Timer 0 | 00000000B |
| 7941H | Timer Data 0 | TCDT0 | R/W | | 00000000B |
| 7942H | Timer Control Status 0 | TCCSL0 | R/W | | 00000000B |
| 7943H | Timer Control Status 0 | TCCSH0 | R/W | | 0XXXXXXXB |
| 7944H to 794BH | Reserved | | | | |
| 794CH | Timer 2/Reload 2 | TMR2/ TMRLR2 | R/W | 16-bit Reload Timer 2 | XXXXXXXXB |
| 794DH | | | R/W | | XXXXXXXXB |
| 794EH | Timer 3/Reload 3 | TMR3/ TMRLR3 | R/W | 16-bit Reload Timer 3 | XXXXXXXXB |
| 794FH | | | R/W | | XXXXXXXXB |
| 7950H to 795FH | Reserved | | | | |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7960H | Clock Monitor Function Control Register | CSVCR | R, R/W | Clock monitor | 00011100B |
| 7961H to 796DH | Reserved | | | | |
| 796EH | CAN Direct Mode Register (MB90V340 only) | CDMR | R/W | CAN clock sync | XXXXXXX0B |
| 796FH to 79DFH | Reserved | | | | |
| 79E0H | Detect Address Setting 0 | PADR0 | R/W | Address Match Detection 0 | XXXXXXXXB |
| 79E1H | Detect Address Setting 0 | PADR0 | R/W | | XXXXXXXXB |
| 79E2H | Detect Address Setting 0 | PADR0 | R/W | | XXXXXXXXB |
| 79E3H | Detect Address Setting 1 | PADR1 | R/W | | XXXXXXXXB |
| 79E4H | Detect Address Setting 1 | PADR1 | R/W | | XXXXXXXXB |
| 79E5H | Detect Address Setting 1 | PADR1 | R/W | | XXXXXXXXB |
| 79E6H | Detect Address Setting 2 | PADR2 | R/W | | XXXXXXXXB |
| 79E7H | Detect Address Setting 2 | PADR2 | R/W | | XXXXXXXXB |
| 79E8H | Detect Address Setting 2 | PADR2 | R/W | | XXXXXXXXB |
| 79E9H to 79EFH | Reserved | | | | |
| 79F0H | Detect Address Setting 3 | PADR3 | R/W | Address Match Detection 1 | XXXXXXXXB |
| 79F1H | Detect Address Setting 3 | PADR3 | R/W | | XXXXXXXXB |
| 79F2H | Detect Address Setting 3 | PADR3 | R/W | | XXXXXXXXB |
| 79F3H | Detect Address Setting 4 | PADR4 | R/W | | XXXXXXXXB |
| 79F4H | Detect Address Setting 4 | PADR4 | R/W | | XXXXXXXXB |
| 79F5H | Detect Address Setting 4 | PADR4 | R/W | | XXXXXXXXB |
| 79F6H | Detect Address Setting 5 | PADR5 | R/W | | XXXXXXXXB |
| 79F7H | Detect Address Setting 5 | PADR5 | R/W | | XXXXXXXXB |
| 79F8H | Detect Address Setting 5 | PADR5 | R/W | | XXXXXXXXB |
| 79F9H to 7BFFH | Reserved | | | | |
| 7C00H to 7CFFH | Reserved for CAN Interface 1. Refer to "■ CAN CONTROLLERS" | | | | |

*(Continued)*

*(Continued)*

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7D00H to 7DFFH | Reserved for CAN Interface 1. Refer to "■ CAN CONTROLLERS" | | | | |
| 7E00H to 7FFFH | Reserved | | | | |

Notes :
- Initial value of "X" represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

## ■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps/s to 2 Mbps/s (when input clock is at 16 MHz)

**List of Control Registers (1)**

| Address CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 000080H | Message buffer valid register | BVALR | R/W | 00000000B |
| 000081H | | | | 00000000B |
| 000082H | Transmit request register | TREQR | R/W | 00000000B |
| 000083H | | | | 00000000B |
| 000084H | Transmit cancel register | TCANR | W | 00000000B |
| 000085H | | | | 00000000B |
| 000086H | Transmission complete register | TCR | R/W | 00000000B |
| 000087H | | | | 00000000B |
| 000088H | Receive complete register | RCR | R/W | 00000000B |
| 000089H | | | | 00000000B |
| 00008AH | Remote request receiving register | RRTRR | R/W | 00000000B |
| 00008BH | | | | 00000000B |
| 00008CH | Receive overrun register | ROVRR | R/W | 00000000B |
| 00008DH | | | | 00000000B |
| 00008EH | Reception interrupt enable register | RIER | R/W | 00000000B |
| 00008FH | | | | 00000000B |

**List of Control Registers (2)**

| Address CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 007D00H<br>007D01H | Control status register | CSR | R/W, W<br>R/W, R | 0XXXX0X1B<br>00XXX000B |
| 007D02H<br>007D03H | Last event indicator register | LEIR | R/W | 000X0000B<br>XXXXXXXXB |
| 007D04H<br>007D05H | Receive and transmit error counter | RTEC | R | 00000000B<br>00000000B |
| 007D06H<br>007D07H | Bit timing register | BTR | R/W | 11111111B<br>X1111111B |
| 007D08H<br>007D09H | IDE register | IDER | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007D0AH<br>007D0BH | Transmit RTR register | TRTRR | R/W | 00000000B<br>00000000B |
| 007D0CH<br>007D0DH | Remote frame receive waiting register | RFWTR | R/W | XXXXXXXXB<br>XXXXXXXXB |
| 007D0EH<br>007D0FH | Transmit interrupt enable register | TIER | R/W | 00000000B<br>00000000B |
| 007D10H<br>007D11H<br>007D12H<br>007D13H | Acceptance mask select register | AMSR | R/W | XXXXXXXXB<br>XXXXXXXXB<br>XXXXXXXXB<br>XXXXXXXXB |
| 007D14H<br>007D15H<br>007D16H<br>007D17H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXXB<br>XXXXXXXXB<br>XXXXXXXXB<br>XXXXXXXXB |
| 007D18H<br>007D19H<br>007D1AH<br>007D1BH | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXXB<br>XXXXXXXXB<br>XXXXXXXXB<br>XXXXXXXXB |

**List of Message Buffers (ID Registers) (1)**

| Address CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 007C00$_H$ to 007C1F$_H$ | General-purpose RAM | — | R/W | XXXXXXXX$_B$ to XXXXXXXX$_B$ |
| 007C20$_H$ | ID register 0 | IDR0 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C21$_H$ | | | | |
| 007C22$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C23$_H$ | | | | |
| 007C24$_H$ | ID register 1 | IDR1 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C25$_H$ | | | | |
| 007C26$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C27$_H$ | | | | |
| 007C28$_H$ | ID register 2 | IDR2 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C29$_H$ | | | | |
| 007C2A$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C2B$_H$ | | | | |
| 007C2C$_H$ | ID register 3 | IDR3 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C2D$_H$ | | | | |
| 007C2E$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C2F$_H$ | | | | |
| 007C30$_H$ | ID register 4 | IDR4 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C31$_H$ | | | | |
| 007C32$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C33$_H$ | | | | |
| 007C34$_H$ | ID register 5 | IDR5 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C35$_H$ | | | | |
| 007C36$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C37$_H$ | | | | |
| 007C38$_H$ | ID register 6 | IDR6 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C39$_H$ | | | | |
| 007C3A$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C3B$_H$ | | | | |
| 007C3C$_H$ | ID register 7 | IDR7 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C3D$_H$ | | | | |
| 007C3E$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C3F$_H$ | | | | |

**List of Message Buffers (ID Registers) (2)**

| Address CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 007C40$_H$ | ID register 8 | IDR8 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C41$_H$ | | | | |
| 007C42$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C43$_H$ | | | | |
| 007C44$_H$ | ID register 9 | IDR9 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C45$_H$ | | | | |
| 007C46$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C47$_H$ | | | | |
| 007C48$_H$ | ID register 10 | IDR10 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C49$_H$ | | | | |
| 007C4A$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C4B$_H$ | | | | |
| 007C4C$_H$ | ID register 11 | IDR11 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C4D$_H$ | | | | |
| 007C4E$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C4F$_H$ | | | | |
| 007C50$_H$ | ID register 12 | IDR12 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C51$_H$ | | | | |
| 007C52$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C53$_H$ | | | | |
| 007C54$_H$ | ID register 13 | IDR13 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C55$_H$ | | | | |
| 007C56$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C57$_H$ | | | | |
| 007C58$_H$ | ID register 14 | IDR14 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C59$_H$ | | | | |
| 007C5A$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C5B$_H$ | | | | |
| 007C5C$_H$ | ID register 15 | IDR15 | R/W | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C5D$_H$ | | | | |
| 007C5E$_H$ | | | | XXXXXXXX$_B$<br>XXXXXXXX$_B$ |
| 007C5F$_H$ | | | | |

**List of Message Buffers (DLC Registers and Data Registers) (1)**

| Address CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 007C60H<br>007C61H | DLC register 0 | DLCR0 | R/W | XXXXXXXXB |
| 007C62H<br>007C63H | DLC register 1 | DLCR1 | R/W | XXXXXXXXB |
| 007C64H<br>007C65H | DLC register 2 | DLCR2 | R/W | XXXXXXXXB |
| 007C66H<br>007C67H | DLC register 3 | DLCR3 | R/W | XXXXXXXXB |
| 007C68H<br>007C69H | DLC register 4 | DLCR4 | R/W | XXXXXXXXB |
| 007C6AH<br>007C6BH | DLC register 5 | DLCR5 | R/W | XXXXXXXXB |
| 007C6CH<br>007C6DH | DLC register 6 | DLCR6 | R/W | XXXXXXXXB |
| 007C6EH<br>007C6FH | DLC register 7 | DLCR7 | R/W | XXXXXXXXB |
| 007C70H<br>007C71H | DLC register 8 | DLCR8 | R/W | XXXXXXXXB |
| 007C72H<br>007C73H | DLC register 9 | DLCR9 | R/W | XXXXXXXXB |
| 007C74H<br>007C75H | DLC register 10 | DLCR10 | R/W | XXXXXXXXB |
| 007C76H<br>007C77H | DLC register 11 | DLCR11 | R/W | XXXXXXXXB |
| 007C78H<br>007C79H | DLC register 12 | DLCR12 | R/W | XXXXXXXXB |
| 007C7AH<br>007C7BH | DLC register 13 | DLCR13 | R/W | XXXXXXXXB |
| 007C7CH<br>007C7DH | DLC register 14 | DLCR14 | R/W | XXXXXXXXB |
| 007C7EH<br>007C7FH | DLC register 15 | DLCR15 | R/W | XXXXXXXXB |

**List of Message Buffers (DLC Registers and Data Registers) (2)**

| Address CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 007C80H to 007C87H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007C88H to 007C8FH | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007C90H to 007C97H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007C98H to 007C9FH | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CA0H to 007CA7H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CA8H to 007CAFH | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CB0H to 007CB7H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CB8H to 007CBFH | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CC0H to 007CC7H | Data register 8 (8 bytes) | DTR8 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CC8H to 007CCFH | Data register 9 (8 bytes) | DTR9 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CD0H to 007CD7H | Data register 10 (8 bytes) | DTR10 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CD8H to 007CDFH | Data register 11 (8 bytes) | DTR11 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CE0H to 007CE7H | Data register 12 (8 bytes) | DTR12 | R/W | XXXXXXXXB to XXXXXXXXB |
| 007CE8H to 007CEFH | Data register 13 (8 bytes) | DTR13 | R/W | XXXXXXXXB to XXXXXXXXB |

**List of Message Buffers (DLC Registers and Data Registers) (3)**

| Address<br>CAN1 | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| $007CF0_H$<br>to<br>$007CF7_H$ | Data register 14<br>(8 bytes) | DTR14 | R/W | $XXXXXXXX_B$<br>to<br>$XXXXXXXX_B$ |
| $007CF8_H$<br>to<br>$007CFF_H$ | Data register 15<br>(8 bytes) | DTR15 | R/W | $XXXXXXXX_B$<br>to<br>$XXXXXXXX_B$ |

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

| Interrupt cause | EI²OS corresponding | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|
| | | Number | Address | Number | Address |
| Reset | N | #08 | FFFFDCH | — | — |
| INT9 instruction | N | #09 | FFFFD8H | — | — |
| Exception | N | #10 | FFFFD4H | — | — |
| Reserved | N | #11 | FFFFD0H | ICR00 | 0000B0H |
| Reserved | N | #12 | FFFFCCH | | |
| CAN 1 reception | N | #13 | FFFFC8H | ICR01 | 0000B1H |
| CAN 1 transmission/node status | N | #14 | FFFFC4H | | |
| Reserved | N | #15 | FFFFC0H | ICR02 | 0000B2H |
| Reserved | N | #16 | FFFFBCH | | |
| Reserved | N | #17 | FFFFB8H | ICR03 | 0000B3H |
| Reserved | N | #18 | FFFFB4H | | |
| 16-bit reload timer 2 | Y1 | #19 | FFFFB0H | ICR04 | 0000B4H |
| 16-bit reload timer 3 | Y1 | #20 | FFFFACH | | |
| Reserved | N | #21 | FFFFA8H | ICR05 | 0000B5H |
| Reserved | N | #22 | FFFFA4H | | |
| PPG C/D | N | #23 | FFFFA0H | ICR06 | 0000B6H |
| PPG E/F | N | #24 | FFFF9CH | | |
| Timebase timer | N | #25 | FFFF98H | ICR07 | 0000B7H |
| External interrupt 8 to 11 | Y1 | #26 | FFFF94H | | |
| Watch timer | N | #27 | FFFF90H | ICR08 | 0000B8H |
| External interrupt 12 to 15 | Y1 | #28 | FFFF8CH | | |
| A/D converter | Y1 | #29 | FFFF88H | ICR09 | 0000B9H |
| I/O timer 0 | N | #30 | FFFF84H | | |
| Reserved | N | #31 | FFFF80H | ICR10 | 0000BAH |
| Reserved | N | #32 | FFFF7CH | | |
| Input capture 0 to 3 | Y1 | #33 | FFFF78H | ICR11 | 0000BBH |
| Reserved | N | #34 | FFFF74H | | |
| UART 0 reception | Y2 | #35 | FFFF70H | ICR12 | 0000BCH |
| UART 0 transmission | Y1 | #36 | FFFF6CH | | |
| UART 1 reception | Y2 | #37 | FFFF68H | ICR13 | 0000BDH |
| UART 1 transmission | Y1 | #38 | FFFF64H | | |

*(Continued)*

*(Continued)*

| Interrupt cause | $EI^2OS$ corresponding | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|
| | | Number | Address | Number | Address |
| Reserved | N | #39 | $FFFF60_H$ | ICR14 | $0000BE_H$ |
| Reserved | N | #40 | $FFFF5C_H$ | | |
| Flash memory | N | #41 | $FFFF58_H$ | ICR15 | $0000BF_H$ |
| Delayed interrupt generation module | N | #42 | $FFFF54_H$ | | |

Y1 : Usable

Y2 : Usable, with $EI^2OS$ stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When 2 peripheral resources share the ICR register, only one can use extended intelligent I/O service at a time.
- When either of the 2 peripheral resources sharing the ICR register specifies extended intelligent I/O service, the other one cannot use interrupts.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating Min | Rating Max | Unit | Remarks |
|---|---|---|---|---|---|
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC} = AV_{CC}$*2 |
| | AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq AVR$*2 |
| Input voltage*1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Maximum clamp current | $I_{CLAMP}$ | –2.0 | +2.0 | mA | *6 |
| Total Maximum clamp current | $\Sigma\|I_{CLAMP}\|$ | — | 40 | mA | *6 |
| “L” level maximum output current | $I_{OL1}$ | — | 15 | mA | *4 |
| | $I_{OL2}$ | — | 40 | mA | *5 |
| “L” level average output current | $I_{OLAV1}$ | — | 4 | mA | *4 |
| | $I_{OLAV2}$ | — | 30 | mA | *5 |
| “L” level maximum overall output current | $\Sigma I_{OL1}$ | — | 125 | mA | *4 |
| | $\Sigma I_{OL2}$ | — | 160 | mA | *5 |
| “L” level average overall output current | $\Sigma I_{OLAV1}$ | — | 40 | mA | *4 +105 °C < $T_A$ ≤ +125 °C |
| | $\Sigma I_{OLAV2}$ | | | | *5 +105 °C < $T_A$ ≤ +125 °C |
| | $\Sigma I_{OLAV1}$ | — | 40 | mA | *4 –40 °C ≤ $T_A$ ≤ +105 °C |
| | $\Sigma I_{OLAV2}$ | | | | *5 –40 °C ≤ $T_A$ ≤ +105 °C |
| “H” level maximum output current | $I_{OH1}$ | — | –15 | mA | *4 |
| | $I_{OH2}$ | — | –40 | mA | *5 |
| “H” level average output current | $I_{OHAV1}$ | — | –4 | mA | *4 |
| | $I_{OHAV2}$ | — | –30 | mA | *5 |
| “H” level maximum overall output current | $\Sigma I_{OH1}$ | — | –125 | mA | *4 |
| | $\Sigma I_{OH2}$ | — | –160 | mA | *5 |
| “H” level average overall output current | $\Sigma I_{OHAV1}$ | — | –40 | mA | *4 +105 °C < $T_A$ ≤ +125 °C |
| | $\Sigma I_{OHAV2}$ | | | | *5 +105 °C < $T_A$ ≤ +125 °C |
| | $\Sigma I_{OHAV1}$ | — | –40 | mA | *4 –40 °C ≤ $T_A$ ≤ +105 °C |
| | $\Sigma I_{OHAV2}$ | | | | *5 –40 °C ≤ $T_A$ ≤ +105 °C |
| Power consumption | $P_D$ | — | 300 | mW | MB90F362/T/S/TS, MB90F367/T/S/TS |
| Operating temperature | $T_A$ | –40 | +105 | °C | |
| | | –40 | +125 | °C | *7 |
| Storage temperature | $T_{STG}$ | –55 | +150 | °C | |

*(Continued)*

*(Continued)*

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0$ V.

*2 : Set $AV_{CC}$ and $V_{CC}$ to the same voltage. Make sure that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ when the power is switched on.

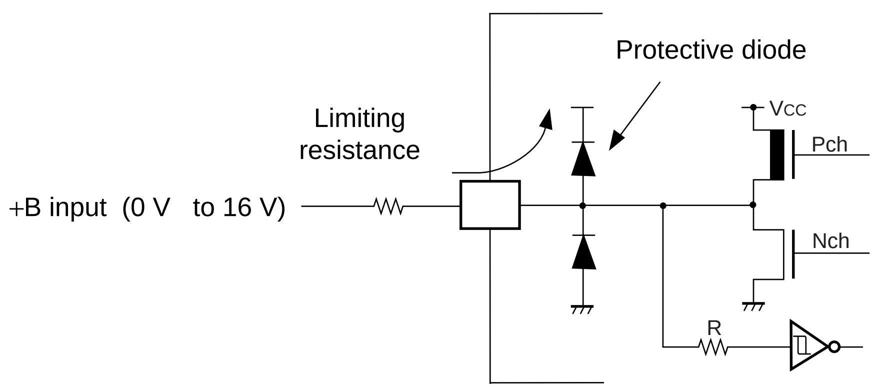
*3 : $V_I$ and $V_O$ should not exceed $V_{CC}$ + 0.3 V. $V_I$ should not exceed the specified ratings. However, if the maximun current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*4 : Applicable to pins : P24 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87

*5 : Applicable to pins : P20 to P23

*6 : Applicable to pins : P20 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is inputted when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits :

**• Input/output equivalent circuits**




*7 : If used exceeding $T_A$ = +105 °C, please contact Fujitsu for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

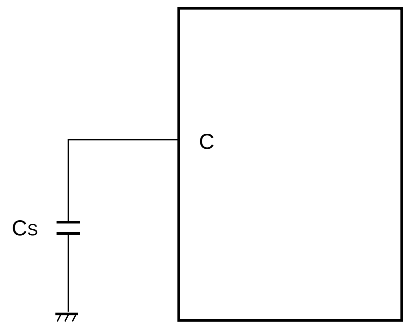
## 2. Recommended Conditions

($V_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 4.0 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.5 | 5.0 | 5.5 | V | Under normal operation when not using the A/D converter and not Flash programming. |
| | | 3.0 | — | 5.5 | V | Maintains RAM data in stop mode |
| Smooth capacitor | $C_S$ | 0.1 | — | 1.0 | µF | Use a ceramic capacitor or capacitor of better AC characteristics. Bypass capacitor at the $V_{CC}$ pin should be greater than this capacitor. |
| Operating temperature | $T_A$ | –40 | — | +105 | °C | |
| | | –40 | — | +125 | °C | * |

* : If used exceeding $T_A$ = +105 °C, please contact Fujitsu for reliability limitations.

• **C Pin Connection Diagram**




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value Min | Value Typ | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Input “H” voltage | $V_{IHS}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Pin inputs if CMOS hysteresis input levels are selected (except P82, P85) |
| | $V_{IHA}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Pin inputs if Automotive input levels are selected |
| | $V_{IHS}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | P82, P85 inputs if CMOS input levels are selected |
| | $V_{IHR}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | $\overline{\text{RST}}$ input pin (CMOS hysteresis) |
| | $V_{IHM}$ | — | — | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | MD input pin |
| Input “L” voltage | $V_{ILS}$ | — | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Pin inputs if CMOS hysteresis input levels are selected (except P82, P85) |
| | $V_{ILA}$ | — | — | $V_{SS}$ – 0.3 | — | 0.5 $V_{CC}$ | V | Pin inputs if Automotive input levels are selected |
| | $V_{ILS}$ | — | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | P82, P85 inputs if CMOS input levels are selected |
| | $V_{ILR}$ | — | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | $\overline{\text{RST}}$ input pin (CMOS hysteresis) |
| | $V_{ILM}$ | — | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | MD input pin |
| Output “H” voltage | $V_{OH}$ | Other than P20 to P23 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output “H” voltage | $V_{OHI}$ | P20 to P23 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –14.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output “L” voltage | $V_{OL}$ | Other than P20 to P23 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |
| Output “L” voltage | $V_{OLI}$ | P20 to P23 | $V_{CC}$ = 4.5 V, $I_{OL}$ = 20.0 mA | — | — | 0.4 | V | |
| Input leak current | $I_{IL}$ | — | $V_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | –1 | — | 1 | µA | |
| Pull-up resistance | $R_{UP}$ | P20 to P27, $\overline{\text{RST}}$ | — | 25 | 50 | 100 | kΩ | |
| Pull-down resistance | $R_{DOWN}$ | MD2 | — | 25 | 50 | 100 | kΩ | Except Flash devices |

*(Continued)*

($T_A = -40$ °C to $+125$ °C, $V_{CC} = 5.0$ V ± 10%, $f_{CP} \leq 24$ MHz, $V_{SS} = AV_{SS} = 0$ V)

| Parameter | Symbol | Pin | Condition | | Value Min | Value Typ | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| Power supply current* | $I_{CC}$ | $V_{CC}$ | $V_{CC} = 5.0$ V, Internal frequency : 24 MHz, At normal operation. | | — | 35 | 45 | mA | |
| | | | $V_{CC} = 5.0$ V, Internal frequency : 24 MHz, At writing FLASH memory. | | — | 50 | 60 | mA | Flash devices |
| | | | $V_{CC} = 5.0$ V, Internal frequency : 24 MHz, At erasing FLASH memory. | | — | 50 | 60 | mA | Flash devices |
| | $I_{CCS}$ | | $V_{CC} = 5.0$ V, Internal frequency : 24 MHz, At sleep mode. | | — | 12 | 20 | mA | |
| | $I_{CTS}$ | | $V_{CC} = 5.0$ V, Internal frequency : 2 MHz, At main timer mode | | — | 0.3 | 0.8 | mA | Without T model |
| | | | | | — | 0.4 | 1.0 | | With T model |
| | $I_{CTSPLL6}$ | | $V_{CC} = 5.0$ V, Internal frequency : 24 MHz, At PLL timer mode, External frequency = 4 MHz | | — | 4 | 7 | mA | |
| | $I_{CCL}$ | | $V_{CC} = 5.0$ V Internal frequency : 8 kHz, At sub operation, $T_A = +25$°C | Stopping clock monitor function | — | 40 | 100 | µA | MB90F362, MB90F367, MB90362, MB90367 |
| | | | | Operating clock monitor function | — | 60 | 150 | | MB90F367, MB90367 |
| | | | | Stopping clock monitor function | — | 90 | 200 | | MB90F362T, MB90F367T, MB90362T, MB90367T |
| | | | | Operating clock monitor function | — | 110 | 250 | | MB90F367T, MB90367T |
| | $I_{CCLS}$ | | $V_{CC} = 5.0$ V Internal frequency : 8 kHz, At sub sleep, $T_A = +25$°C | Stopping clock monitor function | — | 10 | 50 | µA | MB90F362, MB90F367, MB90362, MB90367 |
| | | | | Operating clock monitor function | — | 30 | 100 | | MB90F367, MB90367 |
| | | | | Stopping clock monitor function | — | 60 | 150 | | MB90F362T, MB90F367T, MB90362T, MB90367T |
| | | | | Operating clock monitor function | — | 80 | 200 | | MB90F367T, MB90367T |
| | $I_{CCT}$ | | $V_{CC} = 5.0$ V Internal frequency : 8 kHz, At watch mode, $T_A = +25$°C | Stopping clock monitor function | — | 8 | 30 | µA | MB90F362, MB90F367, MB90362, MB90367 |
| | | | | Operating clock monitor function | — | 30 | 70 | | MB90F367, MB90367 |
| | | | | Stopping clock monitor function | — | 60 | 130 | | MB90F362T, MB90F367T, MB90362T, MB90367T |
| | | | | Operating clock monitor function | — | 80 | 170 | | MB90F367T, MB90367T |
| | $I_{CCH}$ | | $V_{CC} = 5.0$ V, At stop mode, $T_A = +25$°C | | — | 5 | 25 | µA | Without T model |
| | | | | | — | 50 | 130 | µA | With T model |

* : The power supply current is measured with an external clock.

*(Continued)*

*(Continued)*

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Sym-bol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, $V_{CC}$, $V_{SS}$, C | — | — | 5 | 15 | pF | |

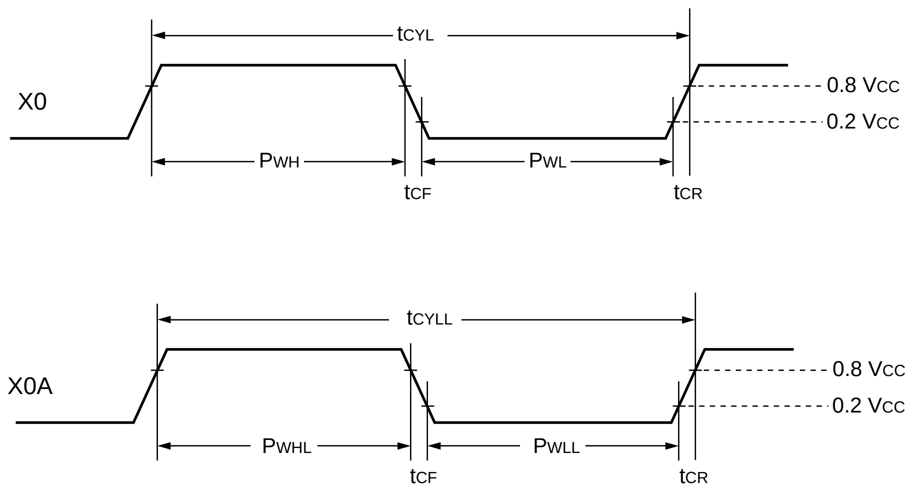
## 4. AC Characteristics

### (1) Clock Timing

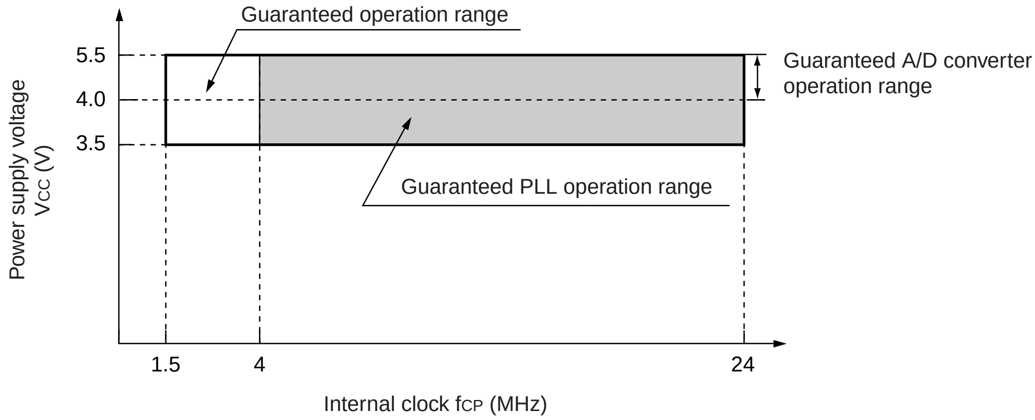
($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Value Min | Value Typ | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | 1/2 when PLL stops, When using an oscillation circuit |
| | | | 4 | — | 16 | MHz | PLL × 1, When using an oscillation circuit |
| | | | 4 | — | 12 | MHz | PLL × 2, When using an oscillation circuit |
| | | | 4 | — | 8 | MHz | PLL × 3, When using an oscillation circuit |
| | | | 4 | — | 6 | MHz | PLL × 4, When using an oscillation circuit |
| | | | 4 | — | 4 | MHz | PLL × 6, When using an oscillation circuit |
| | | X0, X1 | 3 | — | 24 | MHz | 1/2 when PLL stops, When using an external clock |
| | | | 4 | — | 24 | MHz | PLL × 1, When using an external clock |
| | | | 4 | — | 12 | MHz | PLL × 2, When using an external clock |
| | | | 4 | — | 8 | MHz | PLL × 3, When using an external clock |
| | | | 4 | — | 6 | MHz | PLL × 4, When using an external clock |
| | | | 4 | — | 4 | MHz | PLL × 6, When using an external clock |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | 100 | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | 62.5 | — | 333 | ns | When using an oscillation circuit |
| | | X0, X1 | 41.67 | — | 333 | ns | When using an external clock |
| | $t_{CYLL}$ | X0A, X1A | 10 | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio is about 30% to 70%. |
| | $P_{WHL}$, $P_{WLL}$ | X0A | 5 | 15.2 | — | µs | |
| Input clock rise and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When using external clock |
| Internal operating clock frequency (machine clock) | $f_{CP}$ | — | 1.5 | — | 24 | MHz | When using main clock |
| | $f_{CPL}$ | — | — | 8.192 | 50 | kHz | When using sub clock |
| Internal operating clock cycle time (machine clock) | $t_{CP}$ | — | 41.67 | — | 666 | ns | When using main clock |
| | $t_{CPL}$ | — | 20 | 122.1 | — | µs | When using sub clock |

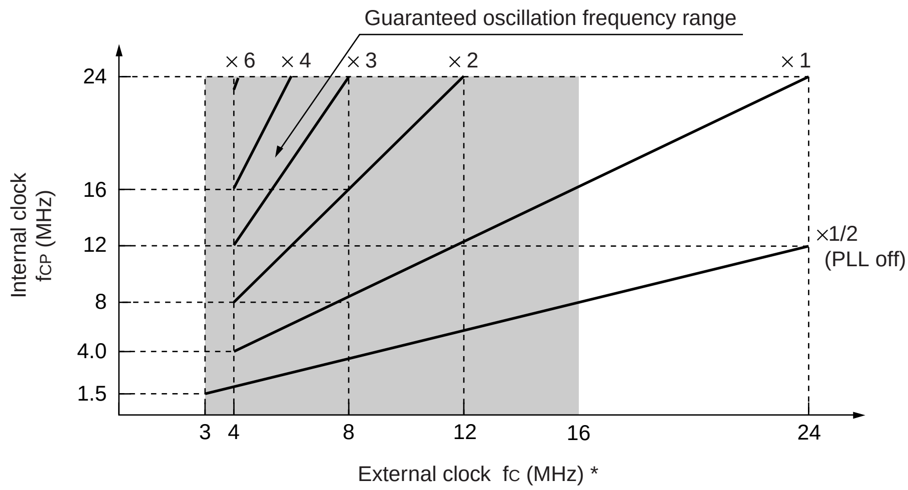
• **Clock Timing**



• Guaranteed PLL Operation Range




**Guaranteed operation range of MB90360 series**



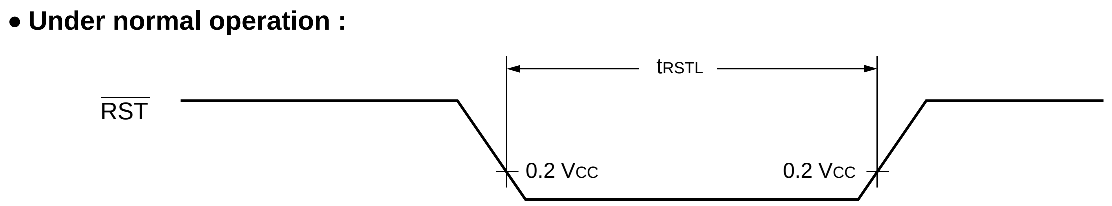

* : When using the oscillation circuit, the maximum oscillation clock frequency is 16 MHz.

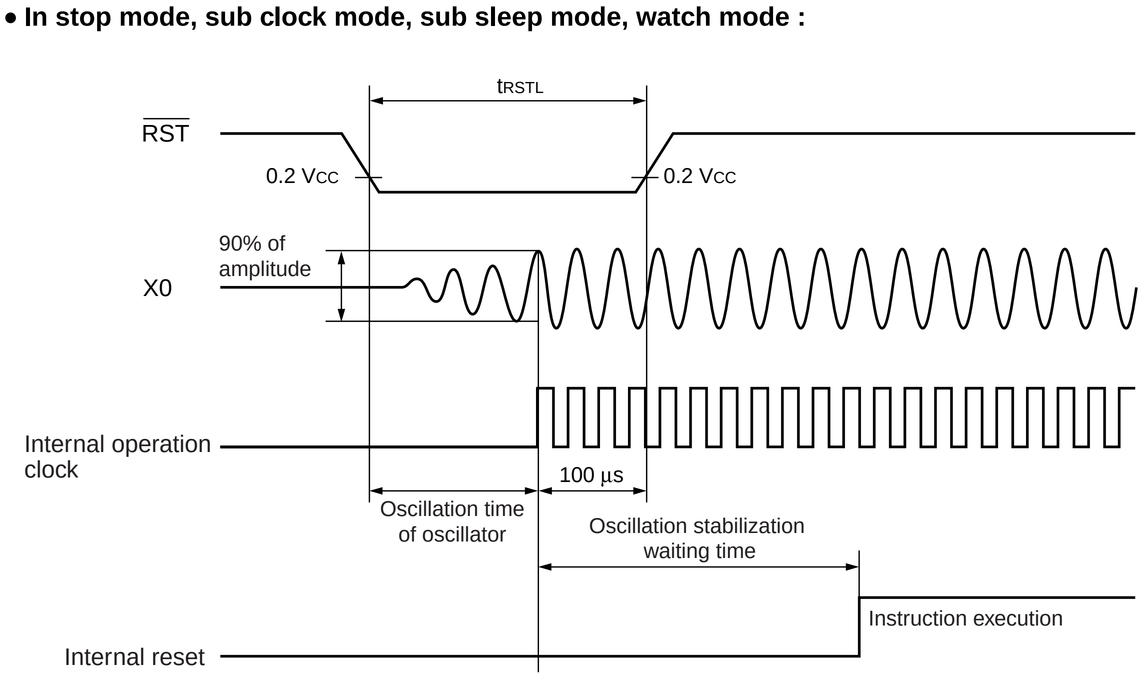
### (2) Reset Standby Input

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 500 | — | ns | Under normal operation |
| | | | Oscillation time of oscillator* + 100 µs | — | ns | In stop mode, sub clock mode, sub sleep mode and watch mode |
| | | | 100 | — | µs | In timebase timer mode |

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms and tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs and several ms. With an external clock, the oscillation time is 0 ms.

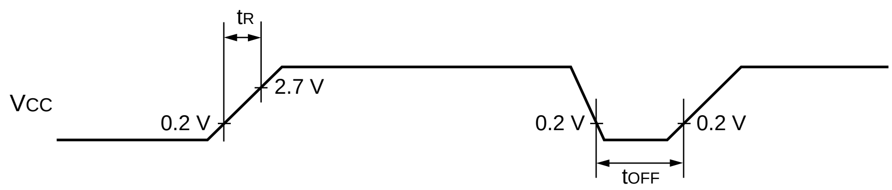


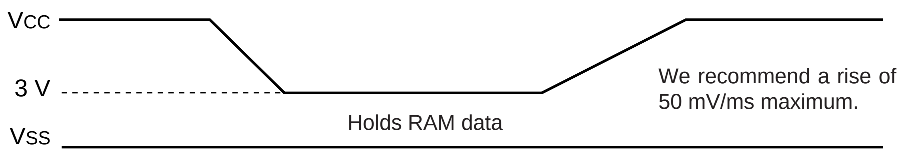
### (3) Power-on Reset

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power on rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | |
| Power off time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | Due to repetitive operation |




If you change the power supply voltage too rapidly, a power-on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



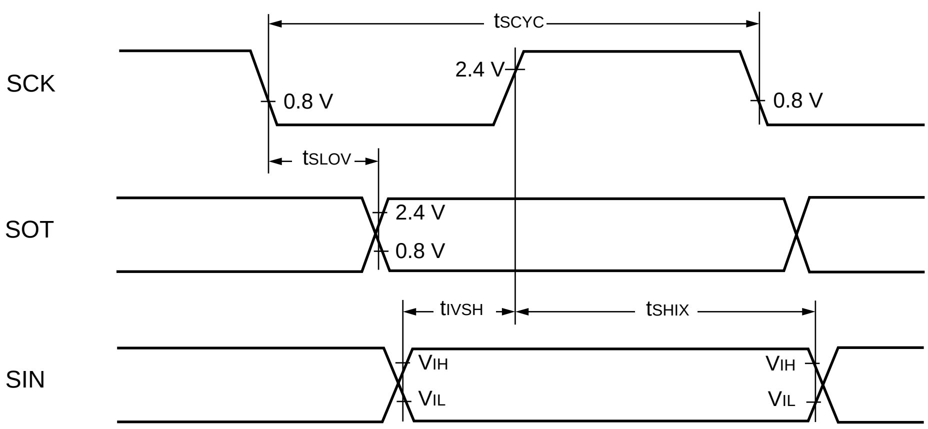
(4) UART0/1

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

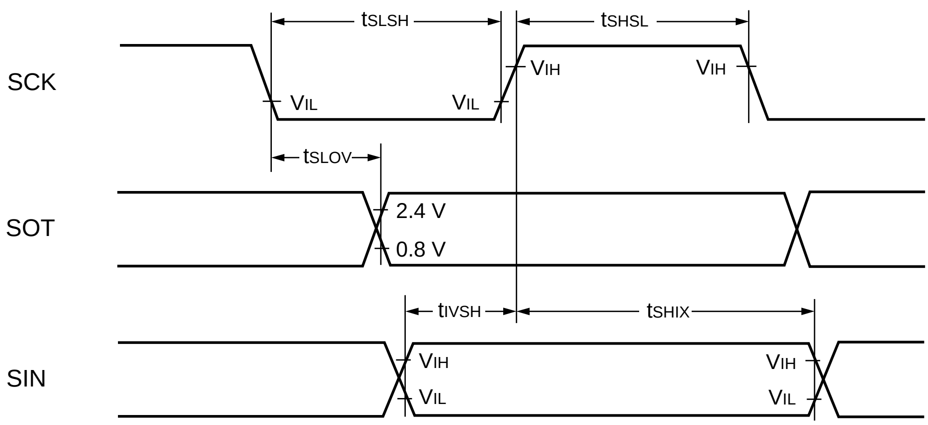
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0, SCK1 | Internal shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 8 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0, SCK1, SOT0, SOT1 | | –80 | +80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0, SCK1, SIN0, SIN1 | | 100 | — | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIX}$ | SCK0, SCK1, SIN0, SIN1 | | 60 | — | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0, SCK1 | External shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 4 $t_{CP}$ | — | ns | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0, SCK1 | | 4 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0, SCK1, SOT0, SOT1 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0, SCK1, SIN0, SIN1 | | 60 | — | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIX}$ | SCK0, SCK1, SIN0, SIN1 | | 60 | — | ns | |

Notes :
- AC characteristic in CLK synchronized mode.
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to " (1) Clock Timing".

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**

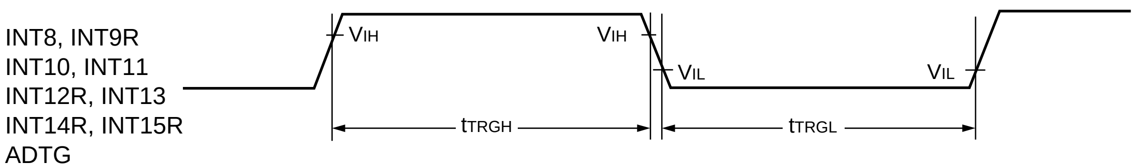



### (5) Trigger Input Timing

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT8, INT9R<br>INT10, INT11<br>INT12R, INT13<br>INT14R, INT15R<br>ADTG | — | 5 $t_{CP}$ | — | ns | |

Note : $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

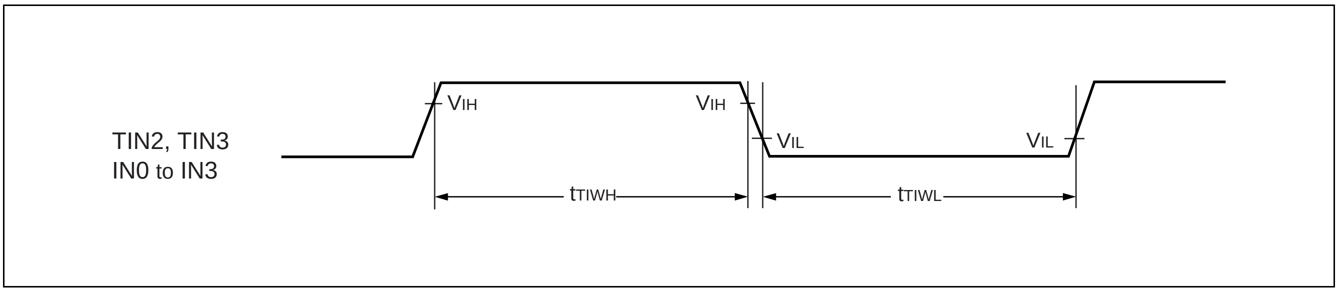


### (6) Timer Related Resource Input Timing

($T_A$ = –40 °C to +125 °C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIN2, TIN3<br>IN0 to IN3 | — | 4 $t_{CP}$ | — | ns | |

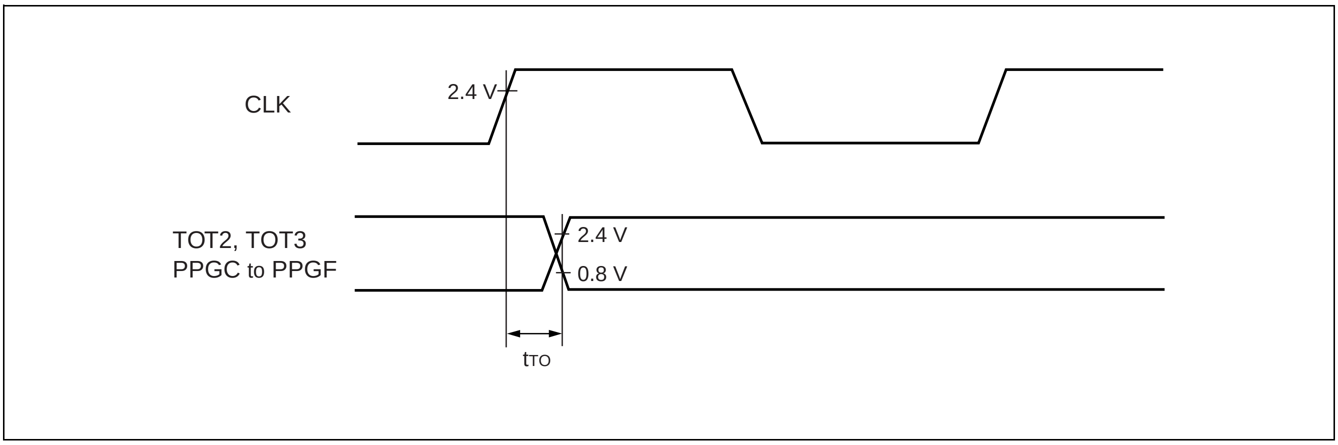
Note : $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to " (1) Clock Timing".




### (7) Timer Related Resource Output Timing

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK ↑ → $T_{OUT}$ change time | $t_{TO}$ | TOT2, TOT3<br>PPGC to PPGF | — | 30 | — | ns | |



## 5. A/D Converter

($T_A$ = –40 °C to +125 °C, 3.0 V ≤ AVR – $AV_{SS}$, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | — | — | ±3.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential nonlinearity error | — | — | — | — | ±1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | AN0 to AN15 | $AV_{SS}$ – 1.5 | $AV_{SS}$ + 0.5 | $AV_{SS}$ + 2.5 | LSB | |
| Full scale reading voltage | $V_{FST}$ | AN0 to AN15 | AVR – 3.5 | AVR – 1.5 | AVR + 0.5 | LSB | |
| Compare time | — | — | 1.0 | — | 16,500 | µs | 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V |
| | | | 2.0 | | | | 4.0 V ≤ $AV_{CC}$ < 4.5 V |
| Sampling time | — | — | 0.5 | — | ∞ | µs | 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V |
| | | | 1.2 | | | | 4.0 V ≤ $AV_{CC}$ < 4.5 V |
| Analog port input current | $I_{AIN}$ | AN0 to AN15 | –0.3 | — | +0.3 | µA | |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN15 | $AV_{SS}$ | — | AVR | V | |
| Reference voltage range | — | AVR | $AV_{SS}$ + 2.7 | — | $AV_{CC}$ | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 3.5 | 7.5 | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage supply current | $I_R$ | AVR | — | 600 | 900 | µA | |
| | $I_{RH}$ | AVR | — | — | 5 | µA | * |
| Offset between input channels | — | AN0 to AN15 | — | — | 4 | LSB | |

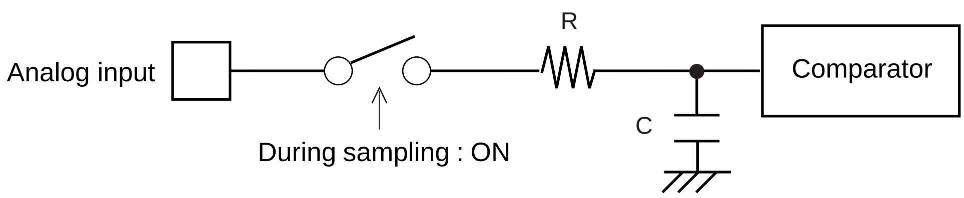
* : If A/D converter is not operating, a current when CPU is stopped is applicable ($V_{CC}$ = $AV_{CC}$ = AVR = 5.0 V) .

*(Continued)*

**• About the external impedance of analog input and its sampling time**

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage changed to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

• Analog input circuit model




MB90F362/T/S/TS, MB90F367/T/S/TS

| | R | C |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V | 2.0 kΩ (Max) | 16.0 pF (Max) |
| 4.0 V ≤ AVcc < 4.5 V | 8.2 kΩ (Max) | 16.0 pF (Max) |

MB90362/T/S/TS, MB90367/T/S/TS, MB90V340A-101/102/103/104

| | R | C |
|---|---|---|
| 4.5 V ≤ AVcc ≤ 5.5 V | 2.0 kΩ (Max) | 14.4 pF (Max) |
| 4.0 V ≤ AVcc < 4.5 V | 8.2 kΩ (Max) | 14.4 pF (Max) |

Note : The values are reference values.

*(Continued)*

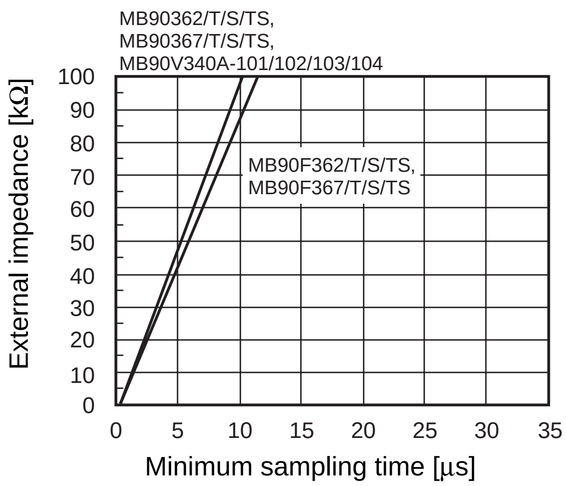
*(Continued)*

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

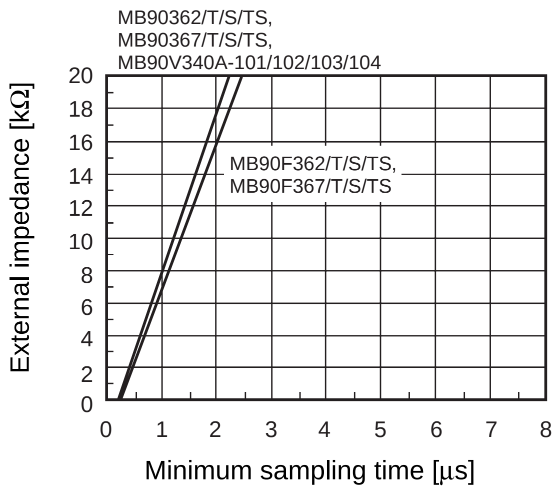
• The relationship between external impedance and minimum sampling time

• At 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

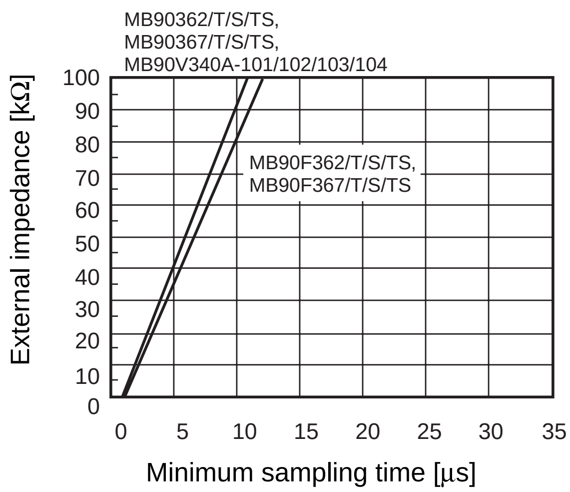



(External impedance = 0 kΩ to 20 kΩ)

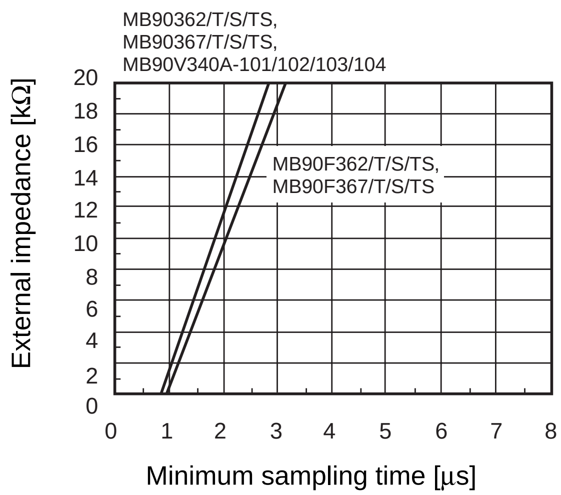



• At 4.0 V ≤ $AV_{CC}$ < 4.5 V

(External impedance = 0 kΩ to 100 kΩ)




(External impedance = 0 kΩ to 20 kΩ)




- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

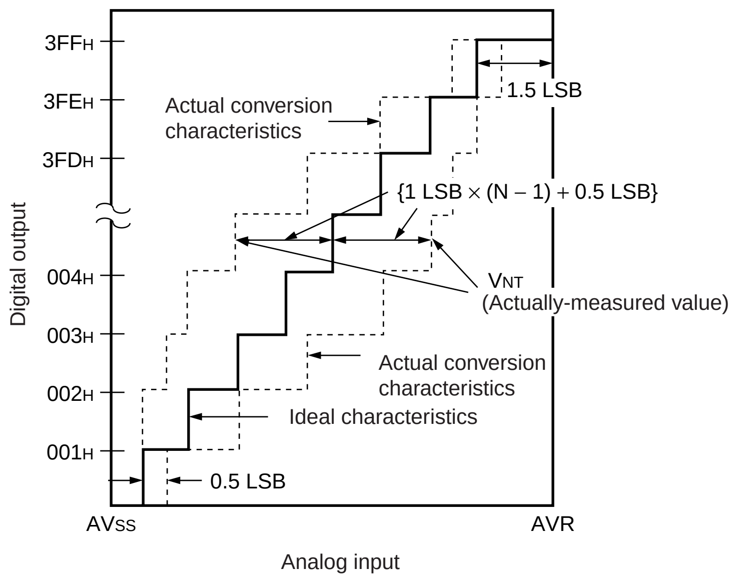
**• About errors**

As | AVR – $AV_{SS}$ | becomes smaller, values of relative errors grow larger.

### 6. Definition of A/D Converter Terms

| | | |
|---|---|---|
| Resolution | : | Analog variation that is recognized by an A/D converter. |
| Non linearity error | : | Deviation between a line across zero-transition line ( "00 0000 0000$_B$" ← → "00 0000 0001$_B$" ) and full-scale transition line ( "11 1111 1110$_B$" ← → "11 1111 1111$_B$" ) and actual conversion characteristics. |
| Differential linearity error | : | Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value. |
| Total error | : | Difference between an actual value and an theoretical value. A total error includes zero transition error, full-scale transition error, and linear error. |

Total error




$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

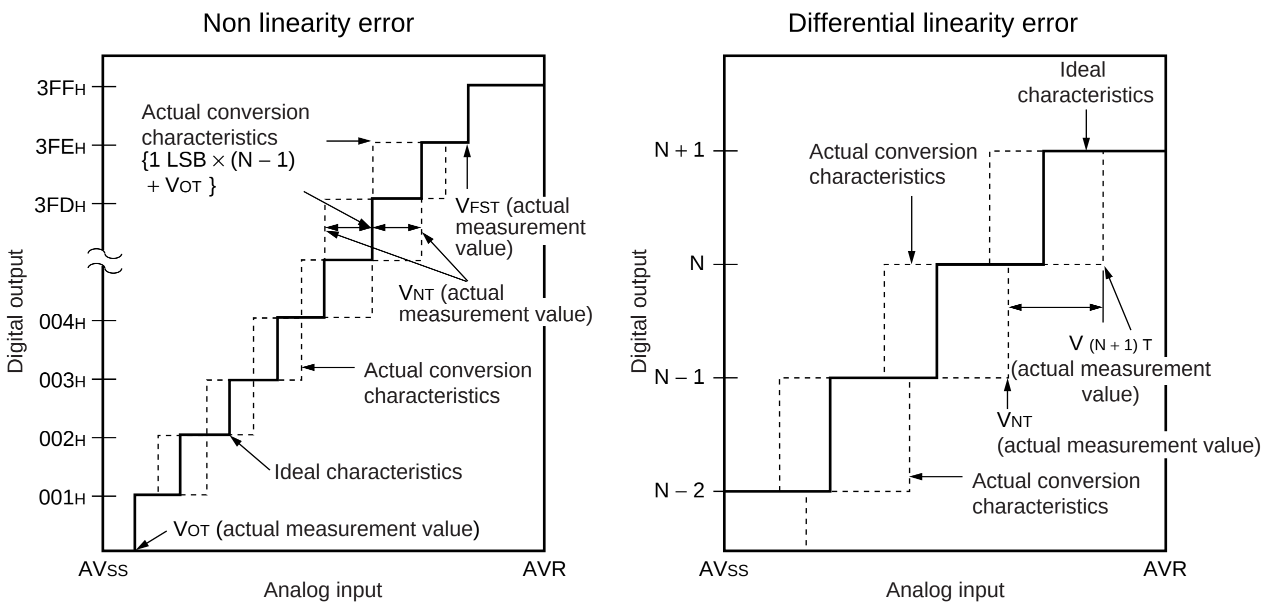
$V_{OT}$ (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

$V_{FST}$ (Ideal value) $= AVR - 1.5$ LSB [V]

$V_{NT}$ : A voltage at which digital output transits from (N – 1) to N.

*(Continued)*

*(Continued)*




$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

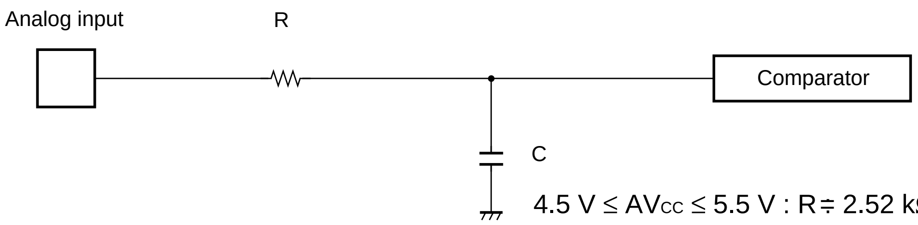
$V_{OT}$ : Voltage at which digital output transits from “$000_H$” to “$001_H$.”
$V_{FST}$ : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

### 7. Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs :

- Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ $AV_{CC}$ ≤ 5.5 V, sampling period = 0.5 µs)
- If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.
- If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

**• Analog input circuit model**




4.5 V ≤ $AV_{CC}$ ≤ 5.5 V : R ≒ 2.52 kΩ, C ≒ 10.7 pF
4.0 V ≤ $AV_{CC}$ < 4.5 V : R ≒ 13.6 kΩ, C ≒ 10.7 pF

Note : Use the values in the figure only as a guideline.

### 8. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Chip erase time | $T_A$ = +25 °C<br>$V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes programming prior to erasure |
| Word (16-bit width) programming time | | — | 16 | 3,600 | µs | Except for the overhead time of the system level |
| Program/Erase cycle | — | 10,000 | — | — | cycle | |
| Flash memory data retention time | Average<br>$T_A$ = +85 °C | 20 | — | — | Year | * |

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

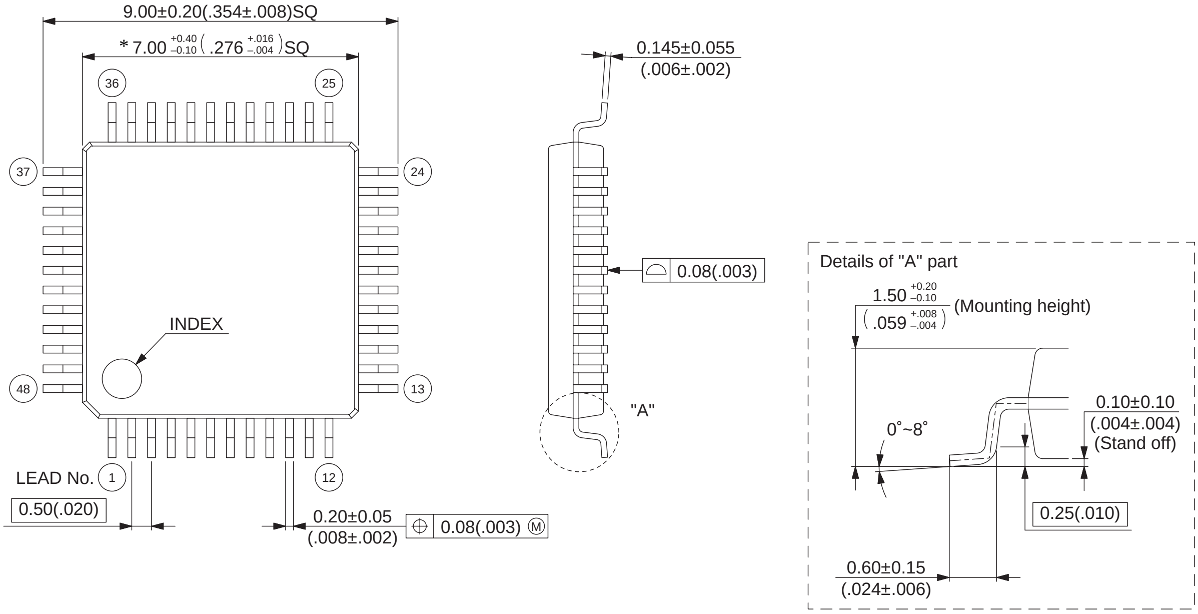
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90F362PMT | 48-pin Plastic LQFP (FPT-48P-M26) | |
| MB90F362TPMT | | |
| MB90F362SPMT | | |
| MB90F362TSPMT | | |
| MB90F367PMT | | |
| MB90F367TPMT | | |
| MB90F367SPMT | | |
| MB90F367TSPMT | | |
| MB90362PMT | | |
| MB90362TPMT | | |
| MB90362SPMT | | |
| MB90362TSPMT | | |
| MB90367PMT | | |
| MB90367TPMT | | |
| MB90367SPMT | | |
| MB90367TSPMT | | |
| MB90V340A-101 | 299-pin Ceramic PGA (PGA-299C-A01) | For evaluation |
| MB90V340A-102 | | |
| MB90V340A-103 | | |
| MB90V340A-104 | | |

## ■ PACKAGE DIMENSION

48-pin Plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

# MB90360 Series

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