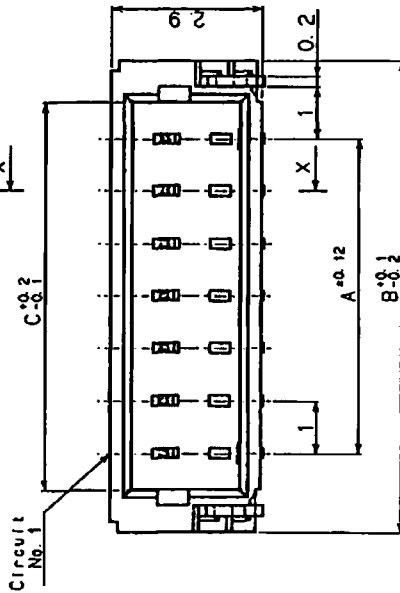
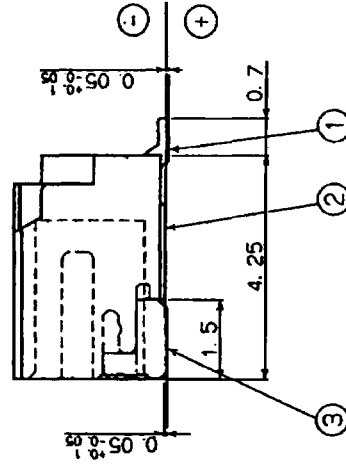
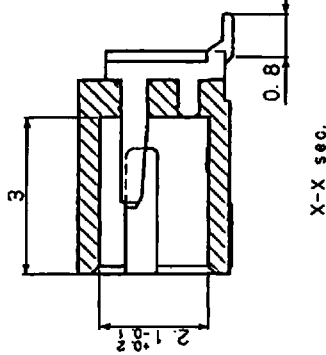


P.C. Board layout



Circuit No.	Dimensions		
	A	B	C
2	1.0	4.0	2.4
3	2.0	5.0	3.4
4	3.0	6.0	4.4
5	4.0	7.0	5.4
6	5.0	8.0	6.4
7	6.0	9.0	7.4
8	7.0	10.0	8.4
9	8.0	11.0	9.4
10	9.0	12.0	10.4
11	10.0	13.0	11.4
12	11.0	14.0	12.4
13	12.0	15.0	13.4
14	13.0	16.0	14.4
15	14.0	17.0	15.4



REVISIONS		PART NAME	
No.	REMARKS	PART No.	DRAWING No.
3	SOLDER TAB BRASS 10.2 COPPER-UNDERPLATED TIN/LEAD ALLOY-PLATED		
2	WAFER POLYAMIDE UL94V-0. NATURAL		
1	BASE CONTACT COPPER ALLOY COPPER-UNDERPLATED TIN/LEAD ALLOY-PLATED		
APPROVED BY: J. S. T. DATE: JUL. 15 1997			
CHECKED BY: M. Y. SCALE: 1:1		SR CONNECTOR	
DRAWN BY: S.S. MATERIAL: J. S. T.		SM(B)-SRSS	
PROJECTION: 1st ANGLE		KRD-20271	

NOTE

1. Unless otherwise specified, tolerances are:
 $0 < L < 1.0: \pm 0.15$ $1.0 < L < 3.0: \pm 0.2$ $3.0 < L: \pm 0.3$
2. Dispersion of solder tail length should be 0.1mm MAX.

THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO JST AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION.