High Density FLASH Memory Card
16, 32, 48, 64, 80 MEGABYTE

FEATURES

- Low cost High Density Linear Flash Card
- Single 5V Supply
  - (3V/5V operation is available as an option)
- Based on Intel 28F640J5 (MLC) Components
- Fast Read Performance
  - 250ns Maximum Access Time
  - (200ns optional)
- PCMCIA compatible
  - x8/ x16 Data Interface
- 32-Byte Write Buffer
  - 6µs per Byte Effective Write Time
- Cross-Compatible Command Support
  - Intel Basic Command Set
  - Common Flash Interface (CFI)
  - Scaleable Command Set
- Power-Down Mode
  - Reset, Power Down Registers
- 10,000 Erase Cycles per Block
- 128K word symmetrical Block Architecture
- PC Card Standard Type II Form Factor

GENERAL DESCRIPTION

WEDC's Flash memory cards – FLF0 Series - offer high density linear Flash memory for code and data storage, high performance disk emulation, mobile PC and embedded applications.

The WEDC FLF0 series is based on Intel's Multi Level Cell (MLC) Flash memory technology, providing high density Flash components at significantly lower cost per megabyte. MLC technology allows for two bits of information to be stored in a single cell. This leads to reduced die size and reduced cost per megabyte.

WEDC's FLF0 series cards are built with Intel's 64Mb components, 28F640J5, with manufacturer/device ID of 89/15H. The FLF0 series is available in standard densities of 16, 32, 48 and 64MB.

Additionally, WEDC's FLF0 series provides densities beyond the 64MB density, supported by PCMCIA standard.

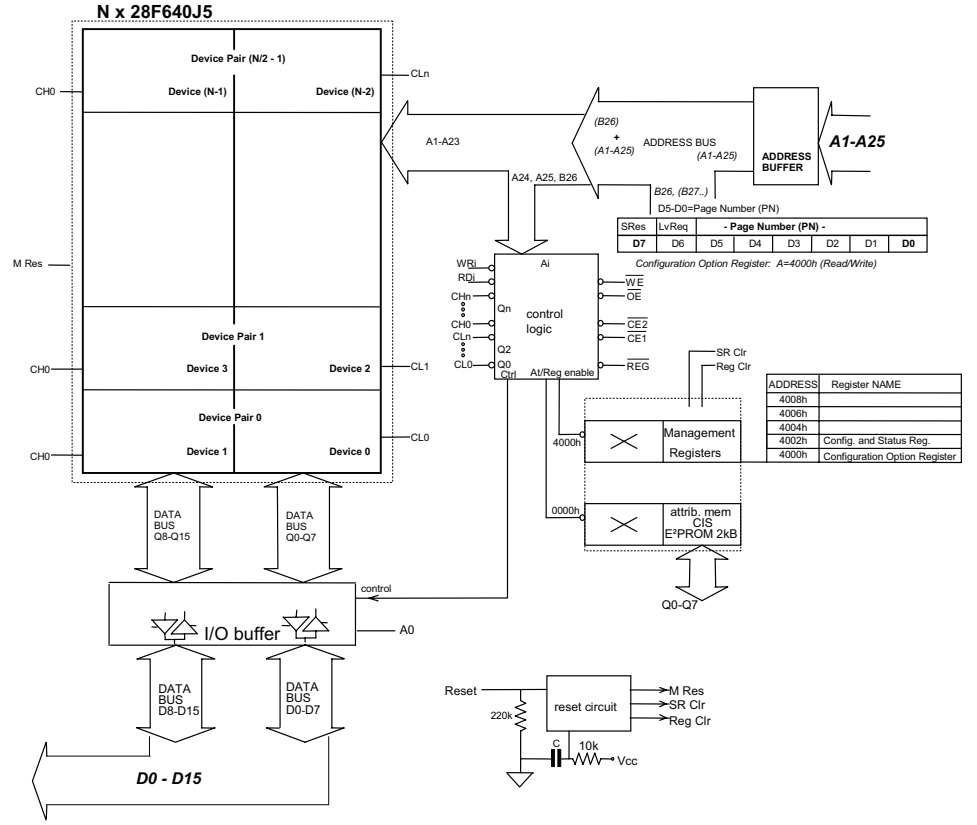
These higher densities are based on a "paging scheme". By writing a page address to the Configuration Option Register (address 4000H), an additional page of memory could be access. The current FLF0 series supports densities to 80MB: total of 2 pages: page 0 := 64MB, page 1 := 16MB.

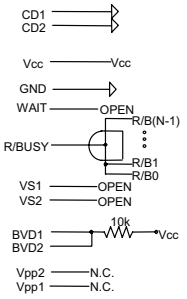
To provide a 16 bit word wide access and to support PCMCIA standard, devices are paired on the card. Therefore, the Flash array is structured in 128K word (256kB) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation.

The FLF0 series cards conform with the PC Card 95 Standard supported by PCMCIA and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Flash Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both, a recessed (for label) or flat housing. Please contact WEDC sales representative for further information on Custom artwork.

BLOCK DIAGRAM





$\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$, $\overline{Reg}$: pull up typ 100k
A0, A25, Reset: pull down typ 100k
R/Busy - Open Drain output (require pull up on host)

Configuration Option Register: ADRS=4000h

Read/Write

SRes	LvReq	- Page Number (PN) -					
D7	D6	D5	D4	D3	D2	D1	**D0**

D7 Soft Reset, active High
1=Reset State
0=End Reset State

D6 LevelReq (not supported)

D5-D0 *Configuration index*
D5-D1 reserved
D0 Page Number Config. (PN) *Power On default =0*

Configuration Status Register: ADRS=4002h

Read/Write

reserved					PwrDwn	*reserved*	
D7	D6	D5	D4	D3	**D2**	D1	D0

D2 Power Down; active High
1 = Place all memory devices in power down mode
0 = normal operation *Power On default=0*

Manufacturer ID	Intel	89_H
Device ID	28F640J5	15_H

FLF0 Flash Card
based on Strata Flash 28F640J5

PINOUT

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ_3	I/O	Data bit 3	
3	DQ_4	I/O	Data bit 4	
4	DQ_5	I/O	Data bit 5	
5	DQ_6	I/O	Data bit 6	
6	DQ_7	I/O	Data bit 7	
7	$\overline{CE}_1$	I	Card enable 1	LOW
8	A_{10}	I	Address bit 10	
9	$\overline{OE}$	I	Output enable	LOW
10	A_{11}	I	Address bit 11	
11	A_9	I	Address bit 9	
12	A_8	I	Address bit 8	
13	A_{13}	I	Address bit 13	
14	A_{14}	I	Address bit 14	
15	$\overline{WE}$	I	Write Enable	LOW
16	$\overline{RDY/BSY}$	O	Ready/Busy	LOW (1)
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Prog. Voltage	NC
19	A_{16}	I	Address bit 16	
20	A_{15}	I	Address bit 15	
21	A_{12}	I	Address bit 12	
22	A_7	I	Address bit 7	
23	A_6	I	Address bit 6	
24	A_5	I	Address bit 5	
25	A_4	I	Address bit 4	
26	A_3	I	Address bit 3	
27	A_2	I	Address bit 2	
28	A_1	I	Address bit 1	
29	A_0	I	Address bit 0	
30	DQ_0	I/O	Data bit 0	
31	DQ_1	I/O	Data bit 1	
32	DQ_2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	$\overline{CD}_1$	O	Card Detect 1	LOW
37	DQ_{11}	I/O	Data bit 11	
38	DQ_{12}	I/O	Data bit 12	
39	DQ_{13}	I/O	Data bit 13	
40	DQ_{14}	I/O	Data bit 14	
41	DQ_{15}	I	Data bit 15	
42	$\overline{CE}_2$	I	Card Enable 2	LOW
43	VS_1	O	Voltage Sense 1	NC (2)
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address bit 17	
47	A_{18}	I	Address bit 18	
48	A_{19}	I	Address bit 19	
49	A_{20}	I	Address bit 20	
50	A_{21}	I	Address bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Prog. Voltage	NC
53	A_{22}	I	Address bit 22	
54	A_{23}	I	Address bit 23	
55	A_{24}	I	Address bit 24	
56	A_{25}	I	Address bit 25	
57	VS_2	O	Voltage Sense 2	NC
58	$\overline{RST}$	I	Card Reset	HIGH
59	$\overline{Wait}$	O	Extended Bus cycle	Low (3)
60	RFU		Reserved	
61	$\overline{REG}$	I	Attrib Mem Select	
62	BVD_2	O	Bat. Volt. Detect 2	(3)
63	BVD_1	O	Bat. Volt. Detect 1	(3)
64	DQ_8	I/O	Data bit 8	
65	DQ_9	I/O	Data bit 9	
66	DQ_{10}	O	Data bit 10	
67	$\overline{CD}_2$	O	Card Detect 2	LOW
68	GND		Ground	

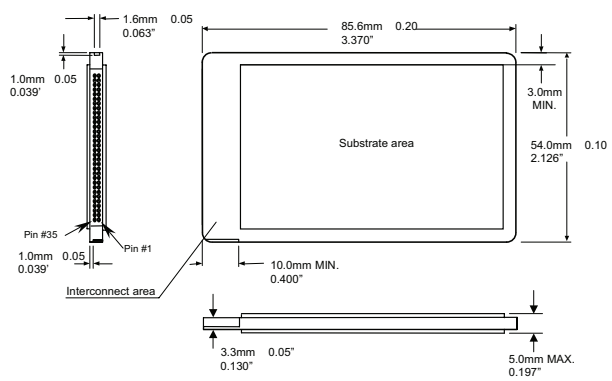
Notes:

1. RDY/BSY signal is an "Open drain" type output, pull-up resistors are required on the host side.

2. VS_1 is connected to GND for 3.3V/5V cards and N.C. for 5V only cards.

3. $\overline{Wait}$, BVD_1 and BVD_2 are internally connected to V_{CC} by resistors for compatibility.

MECHANICAL



CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A_0 - A_{25}	INPUT	**ADDRESS INPUTS:** A_0 through A_{25} enable direct addressing of up to 64MB of memory on the card. Signal A_0 is not used in word access mode. A_{25} is the most significant bit
DQ_0 - DQ_{15}	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 THROUGH DQ_{15} constitute the bi-directional databus. DQ_{15} is the MSB.
$\overline{CE_1}$, $\overline{CE_2}$	INPUT	**CARD ENABLE 1 AND 2:** $\overline{CE_1}$ enables even byte accesses, $\overline{CE_2}$ enables odd byte accesses. Multiplexing A_0, $\overline{CE_1}$ and $\overline{CE_2}$ allows 8-bit hosts to access all data on DQ_0 - DQ_7 (see truth table).
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
$\overline{RDY/BSY}$	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
$\overline{CD_1}$, $\overline{CD_2}$	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
V_{PP1}, V_{PP2}	N.C.	**PROGRAMMING VOLTAGES:** Not connected for 5V only card.
V_{CC}		**CARD POWER SUPPLY:** 5.0V for all internal circuitry
GND		**CARD GROUND**
$\overline{REG}$	INPUT	**ATTRIBUTE MEMORY SELECT :** Active low signal, enables access to attribute memory space, occupied by the Card Information Structure (CIS) and Card Registers.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down control for the memory array.
$\overline{WAIT}$	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 and VS_2 are open to indicate a 5V card .
RFU		**RESERVED FOR FUTURE USE**
NC		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

FUNCTIONAL TRUTH TABLE

READ function						Common Memory			Attribute Memory		
Function Mode	$\overline{CE_2}$	$\overline{CE_1}$	A_0	$\overline{OE}$	$\overline{WE}$	$\overline{REG}$	D_{15}-D_8	D_7-D_0	$\overline{REG}$	D_{15}-D_8	D_7-D_0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

CARD INTERFACE

The FLF0 series flash card complies with PC Card standard (PCMCIA, March 1997). While maintaining PCMCIA compatibility, the FLF0 series card has integrated special features to extend functionality.

Card has built in 2 control registers:

- Configuration Option Register (COR)
  Address = 4000_h
- Configuration and Status Register (CSR)
  Address = 4002_h

COR register: provide a soft reset function (bit D7) and additional page register (bit D0) to extend card capacity beyond 64MB.

SReset

As defined by PCMCIA, setting the SReset bit to 1, places the card in the reset state. During this state all memory devices are place in power down mode, minimizing power consumption. Returning this bit to 0 leaves the reset cycle and place the card in the same condition as following a power up or hardware reset. This bit must be cleared to 0, to access any device on the card.

Complete soft reset cycle must consist of a 2 step write sequence to the SReset bit:

1. Initialization: write 1 to SReset
   - reset cycle begin
   - memory devices enters Power-Down mode aborting all operations and clearing all registers.
2. Write 0 to SReset
   - Reset cycle ends
   - memory devices and registers enters power on default state

Card can be place in Power Down mode by activating Reset signal (pin58) or by controlling the bit D2 in CSR register.

LevlRequest

Not supported

Configuration Index

Configuration Index bits (D0 - D5) are defined to provide address extension bits -page address, to extend card capacity beyond 64MB.

Only bit D0 is supported:

- D0 set to 0 selects **page 0**
- D0 set to 1 selects: **page 1**

D0 is set to the value of 0, during power on or any reset.

CSR register: provide a power control of memory array. Only bit D2 is supported; all other bits are “don’t care”

PwrDwn

Writing 1 to PwrDwn bit (D2) forces each memory device on the card into a reset/power down mode by asserting all the devices RP# pins. Writing 0 to the bit returns the array to stand by mode.

Card Information Structure (CIS) contains information about Registers addressing and Memory structure.

Cards with memory capacity < 64MB do not support Configuration Index bits.

Notes:

1. *Reading from undefined address location or unsupported bits will return random data.*
2. *Writing to undefined address location may result in card malfunctioning due to limited address decoding.*
3. *See block diagram for more details about control registers.*

ABSOLUTE MAXIMUM RATINGS (2)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Storage Temperature	-10°C to +70 °C
Voltage on any pin relative to V_{SS}	-0.5V to V_{CC}+0.5V
V_{CC} supply Voltage relative to V_{SS}	-0.5V to +7.0V

Note:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (1)

Symbol	Parameter	Density (Mbytes)	Notes	Typ(3)	Max	Units	Test Conditions
I_{CCR}	V_{CC} Read Current	16,32,48,64,80		70	110	mA	V_{CC} = V_{CC} max tcycle = 200ns
I_{CCW}	V_{CC} Program Current	16,32,48,64,80		70	120	mA	2 memory devices
I_{CCE}	V_{CC} Erase Current	16,32,48,64,80		70	140	mA	2 memory devices
I_{CCD}	V_{PP} Power-down Current	16	2	160	250	µA	V_{CC} = V_{CC} max Control Signals = V_{CC} Reset = V_{CC} (active)
		32		320	500		
		48		480	750		
		64		650	1000		
		80		800	1250		
I_{CCS} (CMOS)	V_{CC} Standby Current	16	2	0.2	0.4	mA	V_{CC} = V_{CC} max Control Signals = V_{CC}
		32		0.4	0.7		
		48		0.6	1.0		
		64		0.8	1.3		
		80		1.0	1.6		Reset = 0V (not active)

CMOS Test Conditions: V_{CC} = 5V ± 5%, V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V

Notes:
1. *All currents are RMS values unless otherwise specified. I_{CCR}, I_{CCW} and I_{CCE} are based on Word wide operations (2 memory devices activated).*
2. *Control Signals: $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$, $\overline{WE}$.*
3. *Typical: V_{CC} = 5V, T = +25°C.*

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1, 2		±20	µA	V_{CC} = V_{CC}MAX V_{IN} =V_{CC} or GND
I_{LO}	Output Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX V_{IN} =V_{CC} or GND
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7xV_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	1	V_{CC}-0.4	V_{CC}	V	I_{OH} = -2.0mA
V_{LKO}	V_{CC} Erase/Program Lock Voltage	1	3.25		V	

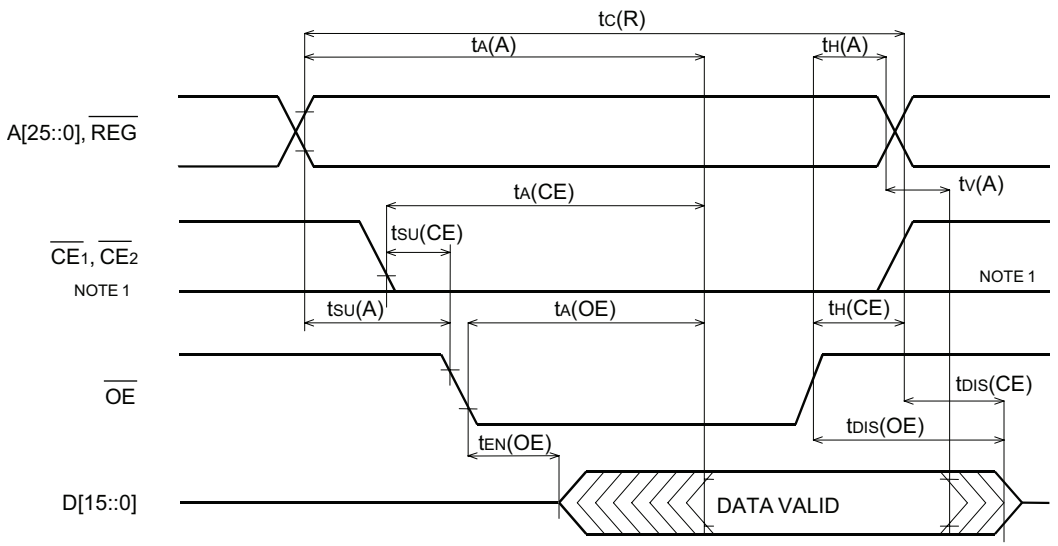
Notes:
1. *Values are the same for byte and word wide modes for all card densities.*
2. *Exception: Leakage current on control signals with internal pull up resistors (see block diag) will be < 500 µA when V_{IN} = GND.*

AC CHARACTERISTICS - READ TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
t_{C}(R)	Read Cycle Time	200		250		ns
t_{A}(A)	Address Access Time		200		250	ns
t_{A}(CE)	Card Enable Access Time		200		250	ns
t_{A}(OE)	Output Enable Access Time		90		100	ns
t_{SU}(A)	Address Setup Time		20		30	ns
t_{SU}(CE)	Card Enable Setup Time		0		0	ns
t_{H}(A)	Address Hold Time		20		20	ns
t_{H}(CE)	Card Enable Hold Time		20		20	ns
t_{V}(A)	Output Hold from Address Change		0		0	ns
t_{DIS}(CE)	Output Disable Time from $\overline{CE}$		90		100	ns
t_{DIS}(OE)	Output Disable Time from $\overline{OE}$		90		100	ns
t_{EN}(CE)	Output Enable Time from $\overline{CE}$	5		5		ns
t_{EN}(OE)	Output Enable Time from $\overline{OE}$	5		5		ns
t_{REC}(RST)	Power Down recovery to Output Delay. V_{CC} = 5V		500		500	ns

Note: *AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.*

READ TIMING DIAGRAM

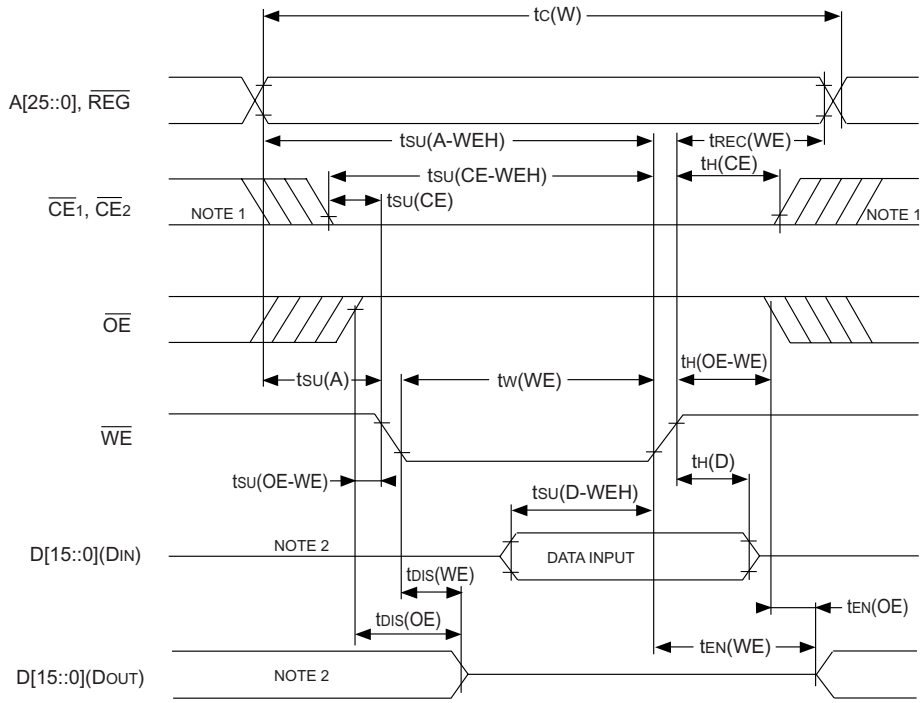


AC CHARACTERISTICS - WRITE TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
tcW	Write Cycle Time	200		250		ns
tw(WE)	Write Pulse Width	120		150		ns
tsu(A)	Address Setup Time	20		30		ns
tsu(A-WEH)	Address Setup Time for $\overline{WE}$	140		180		ns
tsu(CE-WEH)	Card Enable Setup Time for $\overline{WE}$	140		180		ns
tsu(D-WEH)	Data Setup Time for $\overline{WE}$	60		80		ns
tH(D)	Data Hold Time	30		30		ns
trec(WE)	Write Recover Time	30		30		ns
tdis(WE)	Output Disable Time from $\overline{WE}$		90		100	ns
tdis(OE)	Output Disable Time from $\overline{OE}$		90		100	ns
ten(WE)	Output Enable Time from $\overline{WE}$	5		5		ns
ten(OE)	Output Enable Time from $\overline{OE}$	5		5		ns
tsu(OE-WE)	Output Enable Setup from $\overline{WE}$	10		10		ns
tH(OE-WE)	Output Enable Hold from $\overline{WE}$	50		50		ns
tsu(CE)	Card Enable Setup Time from $\overline{OE}$	0		0		ns
tH(CE)	Card Enable Hold Time	20		20		ns
trec(WEL)	Reset recovery to WE going low	1		1		µs

Note: *AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.*

WRITE TIMING DIAGRAM

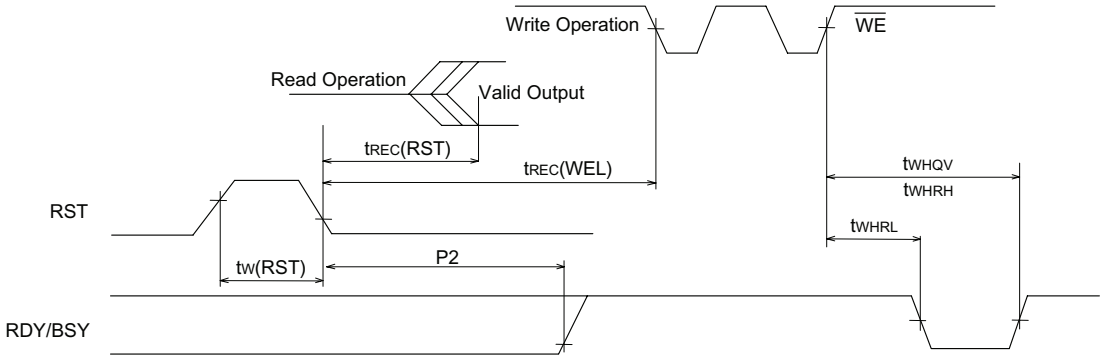


DATA WRITE AND ERASE PERFORMANCE (1,3)
VCC = 5V ± 5%, TA = 0C TO + 70C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
tWHQV1	Word/Byte Program time	2,4		6		µs	Effective time per Byte (using Write Buffer)
tWHQV3	Block Program Time (using Byte program command)			120		µs	
	Block Program Time (using write to buffer command)	2		0.8		sec	Word Program Mode
tWHQV4	Block Erase Time	2		1.0		sec	
tWHRH	Erase Suspend Latency Time to Read			25	35	µs	

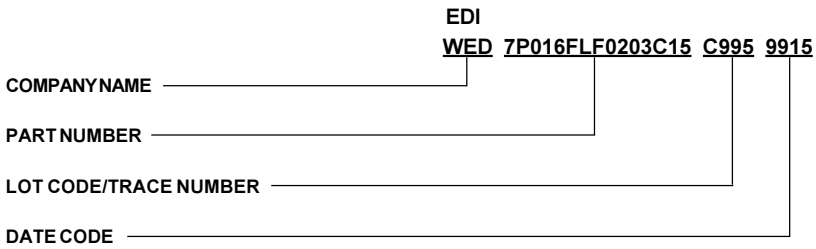
Notes:
1. *Typical: Nominal voltages and TA = 25C.*
2. *Excludes system overhead.*
3. *Valid for all speed options.*
4. *To maximize system performance RDY/BSY signal should be polled.*

WAVEFORMS FOR RESET OPERATION



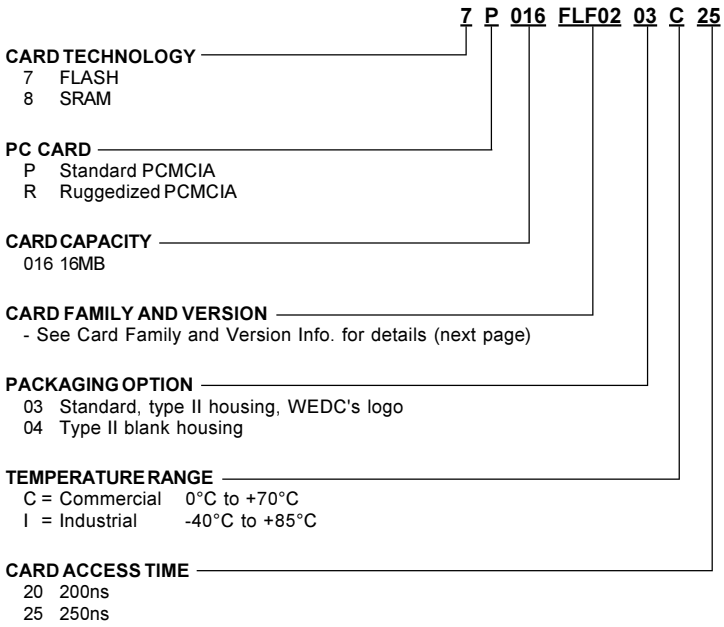
SYMBOL	Parameter	Min	Max	Unit
tw(RST)	Reset pulse High time	35		µs
P2	RST Low to reset during Erase/Program/Lock-bit		100	ns
tREC(RST)	Reset Low to output delay		500	ns
tREC(WEL)	Reset Recovery to WE going Low	1		µs
tWHRL	WE High to RDY/BSY going low		100	ns

PRODUCT MARKING



Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING



ORDERING INFORMATION

7P XXX FLF YY SS T ZZ

XXX

016	16MB
032	32MB
048	48MB
064	64MB
080	80MB

YY

02	Based on 28F640J5 with Attribute Memory
04	Based on 28F640J5 with Attribute Memory and Write Protect Switch (optional)

SS

03	Type II, WEDC Logo
04	Blank Housing Type II
05	Blank Housing Type II Recessed

T

C	Commercial

ZZ

20	200ns
25	250ns

3V/5V operation is available as an option, but the FLF1 series is suggested in such case as a better solution.

WEDC's standard cards are shipped with WEDC's logo. Cards are also available with blank housings (no logo). The blank housings are available in both recessed (for label) and flat housing.
Please contact your WEDC sales representative for further information on custom artwork.

CIS DATA FOR 16MB-64MB CARDS BASED ON INTEL 28F640J5

Sample for 48MB

ADDRESS	VALUE	DESCRIPTION
00H	01H	CISTPL_DEVICE
02H	03H	TPL_LINK
04H	51H	FLASH = 250ns (device writable)
06H	3EH	CARD SIZE: 16MB
	7EH	32MB
	BEH	48MB
	FEH	64MB
08H	FFH	END OF TUPLE
0AH	18H	CISTPL_JEDEC_C
0CH	03H	TPL_LINK
0EH	89H	INTEL - ID
10H	15H	INTEL 28F640J5 - ID
12H	FFH	END OF TUPLE
14H	17H	CISTPL_DEVICE_A
16H	03H	TPL_LINK
18H	42H	EEPROM - 200ns
1AH	01H	Device Size = 2KBytes
1CH	FFH	END OF TUPLE
1EH	1EH	CISTPL_DEVICEGEO
20H	07H	TPL_LINK
22H	02H	DGTPL_BUS
24H	12H	DGTPL_EBS
26H	01H	DGTPL_RBS
28H	01H	DGTPL_WBS
2AH	01H	DGTPL_PART
2CH	01H	FLASH DEVICE NON-INTERLEAVED
2EH	FFH	END OF TUPLE
30H	20H	CISTPL_MANFID
32H	05H	TPL_LINK(04H)
34H	F6H	EDI TPLMID_MANF: LSB
36H	01H	EDI TPLMID_MANF: MSB
38H	00H	*LSB: Number Not Assigned*
3AH	00H	*MSB: Number Not Assigned*
3CH	FFH	END OF TUPLE
3EH	1AH	CISTPL_CONF
40H	06H	TPL_LINK
42H	01H	TPCC_SZ
44H	45H	TPCC_LAST
46H	37H	TPCC_RADR
48H	50H	TPCC_RADR
4AH	30H	TPCC_RMSK
4EH	**1BH**	**CISTPL_CFTABLE_ENTRY**
50H	**03H**	TPL_LINK
52H	**00H**	TPCE_INDEX
54H	**00H**	TPCE_FS (no selection)
56H	**FFH**	END OF TUPLE
58H	**15H**	**CISTPL_VERS1**
5AH	**47H**	TPL_LINK
5CH	**05H**	TPLLV1_MAJOR

ADDRESS	VALUE	DESCRIPTION
5EH	**00H**	TPLLV1_MINOR
60H	**45H**	E
62H	**44H**	D
64H	**49H**	I
66H	**37H**	7
68H	**50H**	P
6AH	**30H**	0
6CH	**34H**	4
6EH	**38H**	8
70H	**46H**	F
72H	**4CH**	L
74H	**46H**	F
76H	**30H**	0
78H	**32H**	2
7AH	**2DH**	-
7CH	**2DH**	-
7EH	**2DH**	-
80H	**32H**	2
82H	**35H**	5
84H	**20H**	SPACE
86H	**00H**	END TEXT
88H	**43H**	C
8AH	**4FH**	O
8CH	**50H**	P
8EH	**59H**	Y
90H	**52H**	R
92H	**49H**	I
94H	**47H**	G
96H	**48H**	H
98H	**54H**	T
9AH	**20H**	SPACE
9CH	**45H**	E
9EH	**4CH**	L
A0H	**45H**	E
A4H	**54H**	T
A6H	**52H**	R
A8H	**4FH**	O
AAH	**4EH**	N
ACH	**49H**	I
AEH	**43H**	C
B0H	**20H**	SPACE
B2H	**44H**	D
B4H	**45H**	E
B6H	**53H**	S
B8H	**49H**	I
BAH	**47H**	G
BCH	**4EH**	N
BEH	**53H**	S
C0H	**20H**	SPACE
C2H	**49H**	I

CIS DATA FOR 16MB-64MB CARDS (CONT.)

ADDRESS	VALUE	DESCRIPTION
C4H	**4EH**	N
C6H	**43H**	C
C8H	**4FH**	O
CAH	**52H**	R
CCH	**50H**	P
CEH	**4FH**	O
D0H	**52H**	R
D2H	**41H**	A
D4H	**54H**	T
D6H	**45H**	E

ADDRESS	VALUE	DESCRIPTION
D8H	**44H**	D
DAH	**20H**	SPACE
DCH	**00H**	END TEXT
DEH	**31H**	1
E0H	**39H**	9
E2H	**39H**	9
E4H	**38H**	8
E6H	**00H**	END TEXT
E8H	**FFH**	END OF LIST
EAH	**FFH**	

CIS DATA FOR 80MB CARD BASED ON INTEL 28F640J5

ADDRESS	VALUE	DESCRIPTION
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**51H**	FLASH = 250ns (device writable)
06H	**FEH**	CARD SIZE: 64MB(1st page)
08H	**FFH**	END OF TUPLE
0AH	**09H**	**CISTPL_EXTDEVICE**
0CH	**06H**	TPL_LINK
0EH	**04H**	Mem Paging Info: 1bit/COR/64M
10H	**51H**	FLASH = 250ns
12H	**07H**	Device Size Extender
14H	**01H**	1x64MB
16H	**3EH**	+16MB
18H	**FFH**	END OF TUPLE
1AH	**1AH**	**CISTPL_CONF**
1CH	**06H**	TPL_LINK
1EH	**01H**	TPCC_SZ
20H	**00H**	TPCC_LAST(no index descript)
22H	**00H**	TPCC_RADR: LSByte
24H	**40H**	TPCC_RADR: MSByte
26H	**03H**	TPCC_RMSK: 2 Reg
28H	**FFH**	END OF TUPLE
2AH	**18H**	**CISTPL_JEDEC_C**
2CH	**03H**	TPL_LINK
2EH	**89H**	INTEL - ID
30H	**15H**	INTEL 28F640J5 - ID
32H	**FFH**	END OF TUPLE
34H	**17H**	**CISTPL_DEVICE_A**
36H	**03H**	TPL_LINK
38H	**42H**	EEPROM - 200ns
3AH	**01H**	Device Size = 2KBytes
3CH	**FFH**	END OF TUPLE
3EH	**1EH**	**CISTPL_DEVICEGEO**
40H	**07H**	TPL_LINK
42H	**02H**	DGTPL_BUS

ADDRESS	VALUE	DESCRIPTION
44H	**12H**	DGTPL_EBS
46H	**01H**	DGTPL_RBS
48H	**01H**	DGTPL_WBS
4AH	**01H**	DGTPL_PART
4CH	**01H**	FLASH DEVICE NON-INTERLEAVED
4EH	**FFH**	END OF TUPLE
50H	**20H**	**CISTPL_MANFID**
52H	**04H**	TPL_LINK(04H)
54H	**F6H**	**EDI** TPLMID_MANF: LSB
56H	**01H**	**EDI** TPLMID_MANF: MSB
58H	**00H**	*LSB: Number Not Assigned*
5AH	**00H**	*MSB: Number Not Assigned*
5CH	**15H**	**CISTPL_VERS1**
5EH	**47H**	TPL_LINK
60H	**05H**	TPLLV1_MAJOR
62H	**00H**	TPLLV1_MINOR
64H	**45H**	*E*
66H	**44H**	*D*
68H	**49H**	*I*
6AH	**37H**	*7*
6CH	**50H**	*P*
6EH	**30H**	*0*
70H	**38H**	*8*
72H	**30H**	*0*
74H	**46H**	*F*
76H	**4CH**	*L*
78H	**46H**	*F*
7AH	**30H**	*0*
7CH	**32H**	*2*
7EH	**2DH**	-
80H	**2DH**	-
82H	**2DH**	-
84H	**32H**	*2*

CIS DATA FOR 80MB CARD (CONT.)

ADDRESS	VALUE	DESCRIPTION
86H	**35H**	*5*
88H	**20H**	*SPACE*
8AH	**00H**	END TEXT
8CH	**43H**	*C*
8EH	**4FH**	*O*
90H	**50H**	*P*
92H	**59H**	*Y*
94H	**52H**	*R*
96H	**49H**	*I*
98H	**47H**	*G*
9AH	**48H**	*H*
9CH	**54H**	*T*
9EH	**20H**	*SPACE*
A0H	**45H**	*E*
A2H	**4CH**	*L*
A4H	**45H**	*E*
A6H	**43H**	*C*
A8H	**54H**	*T*
AAH	**52H**	*R*
ACH	**4FH**	*O*
AEH	**4EH**	*N*
B0H	**49H**	*I*
B2H	**43H**	*C*
B4H	**20H**	*SPACE*
B6H	**44H**	*D*
B8H	**45H**	*E*
BAH	**53H**	*S*
BCH	**49H**	*I*
BEH	**47H**	*G*
C0H	**4EH**	*N*
C2H	**53H**	*S*
C4H	**20H**	*SPACE*
C6H	**49H**	*I*
C8H	**4EH**	*N*
CAH	**43H**	*C*
CCH	**4FH**	*O*
CEH	**52H**	*R*
D0H	**50H**	*P*
D2H	**4FH**	*O*
D4H	**52H**	*R*
D6H	**41H**	*A*
D8H	**54H**	*T*
DAH	**45H**	*E*
DCH	**44H**	*D*
DEH	**20H**	*SPACE*
E0H	**00H**	*END TEXT*
E2H	**31H**	*1*
E4H	**39H**	*9*
E6H	**39H**	*9*

ADDRESS	VALUE	DESCRIPTION
E8H	**38H**	*8*
EAH	**00H**	END TEXT
ECH	**FFH**	END OF LIST
EEH	**FFH**	**CISTPL_END**
D2H	**FFH**	

Document Title

PCMCIA Flash Memory Card - FL0 Series

Revision History

Rev level	Description	Date
Rev 1	Initial release	March 20, 1998
Rev 2	Logo change	May 27, 1999
Rev 3	Added Page 10, changed page header	June 5, 2000
Rev 4	Corrected timing errors on pgs. 7&8	August 1, 2000
Rev 5	Change to FLF0. Ordering info changed and moved to page 11	March 18, 2003