

MSC23S132B/BL-xxBS8/DS8

1,048,576-Word by 32-Bit DRAM Module: Fast Page Mode

DESCRIPTION

The OKI MSC23S132B/BL-xxBS8/DS8 is a fully decoded 1,048,576-word x 32-bit CMOS Dynamic Random Access Memory Module composed of eight 4-Mb DRAMs in SOJ (MSM514400B/BL) packages mounted with four 0.2 μ F decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for non-parity memory expansion applications such as fax machines, printers and personal computers. The low-power version (BL) offers reduced power consumption for mobile computing applications like laptops and palmtops.

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FEATURES

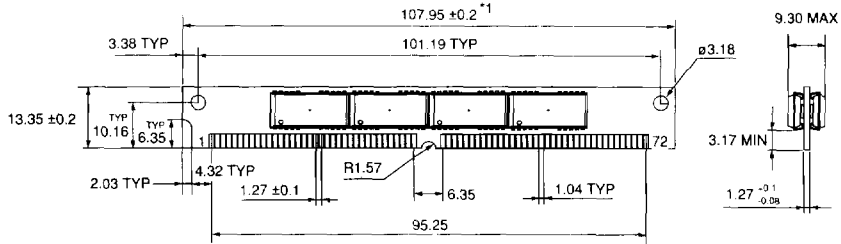
- 1-Meg x 32-bit organization
- 72-pin socket insertable module
 - MSC23S132B/BL-xxBS8: Gold tab
 - MSC23S132B/BL-xxDS8: Solder tab
- Single +5 V supply ± 10 % tolerance
- Access times: 60, 70, 80, 100 ns
- Input: TTL compatible
- Output: TTL compatible, three-state
- Refresh: 1024 cycles/16 ms (128 ms: L-version)
- $\overline{\text{CAS}}$ -before-RAS refresh, $\overline{\text{CAS}}$ -before-RAS hidden refresh, RAS-only refresh capability
- Multibit test mode capability

Family Organization

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSC23S132B/BL-60BS8/DS8	60 ns	30 ns	15 ns	110 ns	4400 mW	44 mW
MSC23S132B/BL-70BS8/DS8	70 ns	35 ns	20 ns	130 ns	3960 mW	
MSC23S132B/BL-80BS8/DS8	80 ns	40 ns	20 ns	150 ns	3520 mW	8.8 mW (L-version)
MSC23S132B/BL-10BS8/DS8	100 ns	50 ns	25 ns	180 ns	3080 mW	

PIN CONFIGURATION

MSC23S132B/BL-xxBS8/DS8



*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

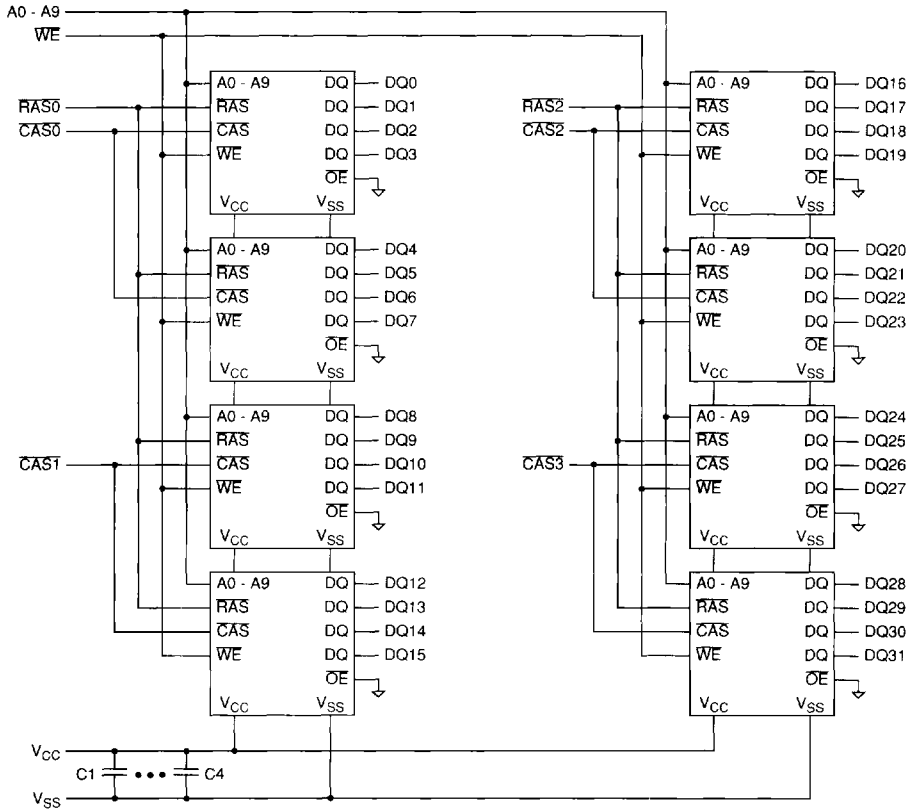
Pin Configuration

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V _{SS}	16	A4	31	A8	46	N.C.	61	DQ13
2	DQ0	17	A5	32	A9	47	WE	62	DQ30
3	DQ16	18	A6	33	N.C.	48	N.C.	63	DQ14
4	DQ1	19	N.C.	34	RAS2	49	DQ8	64	DQ31
5	DQ17	20	DQ4	35	N.C.	50	DQ24	65	DQ15
6	DQ2	21	DQ20	36	N.C.	51	DQ9	66	N.C.
7	DQ18	22	DQ5	37	N.C.	52	DQ25	67	PD0
8	DQ3	23	DQ21	38	N.C.	53	DQ10	68	PD1
9	DQ19	24	DQ6	39	V _{SS}	54	DQ26	69	PD2
10	V _{CC}	25	DQ22	40	CAS0	55	DQ11	70	PD3
11	N.C.	26	DQ7	41	CAS2	56	DQ27	71	N.C.
12	A0	27	DQ23	42	CAS3	57	DQ12	72	V _{SS}
13	A1	28	A7	43	CAS1	58	DQ28		
14	A2	29	N.C.	44	RAS0	59	V _{CC}		
15	A3	30	V _{CC}	45	N.C.	60	DQ29		

Presence Detect Pins

Pin Number	Pin Name	60 ns	70 ns	80 ns	100 ns
67	PD0	V _{SS}	V _{SS}	V _{SS}	V _{SS}
68	PD1	V _{SS}	V _{SS}	V _{SS}	V _{SS}
69	PD2	N.C.	V _{SS}	N.C.	V _{SS}
70	PD3	N.C.	N.C.	V _{SS}	V _{SS}

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ^[1]

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 ~ +7.0	V
Voltage V _{CC} supply relative to V _{SS}	V _{CC}	-1.0 ~ +7.0	V
Short circuit output current	I _{OS}	50	mA
Power dissipation	P _D	8	W
Operating temperature	T _{OPR}	0 ~ +70	°C
Storage temperature	T _{STG}	-40 ~ +125	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~ +70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.4	-	6.5	V
Input low voltage	V _{IL}	-1.0	-	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz) ^[1]

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A0 ~ A9)	C _{IN1}	-	74	pF
Input capacitance (WE)	C _{IN2}	-	76	pF
Input capacitance (RAS0, RAS2)	C _{IN3}	-	48	pF
Input capacitance (CAS0 ~ CAS3)	C _{IN4}	-	34	pF
I/O capacitance (DQ0 ~ DQ31)	C _{DQ}	-	17	pF

1. Capacitance measured with Boonton Meter.

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C} \sim +70^\circ\text{C}$)

Parameter	Symbol	Condition	60 ns		70 ns		80 ns		100 ns		Unit	Note	
			Min	Max	Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	$0\text{ V} \leq V_I \leq 6.5\text{ V}$; All other pins not under test = 0 V	-80	80	-80	80	-80	80	-80	80	μA		
Output leakage current	I_{LO}	D_{OUT} disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-10	10	-10	10	-10	10	-10	10	μA		
Output high voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V		
Output low voltage	V_{OL}	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	0	0.4	V		
Average power supply current (Operating)	I_{CC1}	RAS, CAS cycling, $t_{RC} = \text{min.}$	-	800	-	720	-	640	-	560	mA	[1] [2]	
Power supply current (Standby)	I_{CC2}	RAS = V_{IH} , CAS = V_{IH} , $D_{OUT} = \text{Hi-Z}$	TTL	-	16	-	16	-	16	-	16	mA	
			MOS	-	8	-	8	-	8	-	8	mA	
				-	1.6	-	1.6	-	1.6	-	1.6	mA	[3]
Average power supply current (RAS-only refresh)	I_{CC3}	RAS cycling, CAS = V_{IH} , $t_{RC} = \text{min.}$	-	800	-	720	-	640	-	560	mA	[1] [2]	
Average power supply current (CAS-before-RAS refresh)	I_{CC6}	RAS cycling, CAS-before-RAS, $t_{RC} = \text{min.}$	-	800	-	720	-	640	-	560	mA	[1]	
Average power supply current (Fast Page Mode)	I_{CC7}	RAS = V_{IL} , CAS cycling, $t_{PC} = \text{min.}$	-	640	-	560	-	480	-	400	mA	[1] [4]	
Average power supply current (Battery Backup)	I_{CC10}	$t_{RC} = 125\ \mu\text{s}$, CAS-before-RAS cycling	-	2.4	-	2.4	-	2.4	-	2.4	mA	[1] [3]	

- I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.
- Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
- L-version only $t_{\text{RAS}}=t_{\text{RAS}}$ (min.) to $1\ \mu\text{s}$. Input voltage: All pins $V_{IH} \geq V_{CC} - 0.2\text{ V}$ or $V_{IL} \leq 0.2\text{ V}$.
- Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

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AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C} \sim +70^\circ\text{C}$) [1] [2] [3]

Parameter	Symbol	60 ns		70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	-	130	-	150	-	180	-	ns	
Fast Page Mode cycle time	t_{PC}	40	-	45	-	50	-	60	-	ns	
Access time from RAS	t_{RAC}	-	60	-	70	-	80	-	100	ns	[4] [5] [6]
Access time for CAS	t_{CAC}	-	15	-	20	-	20	-	25	ns	[4] [5]
Access time from column address	t_{AA}	-	30	-	35	-	40	-	50	ns	[4] [6]
Access time from CAS precharge	t_{CPA}	-	35	-	40	-	45	-	55	ns	[4]
Output low impedance time from CAS	t_{CLZ}	0	-	0	-	0	-	0	-	ns	
Output buffer turn-off delay time	t_{OFF}	0	15	0	20	0	20	0	25	ns	[7]
Transition time	t_T	3	50	3	50	3	50	3	50	ns	[3]
Refresh period	t_{REF}	-	16	-	16	-	16	-	16	ms	
Refresh period (L-version)	t_{REF}	-	128	-	128	-	128	-	128	ms	
RAS precharge time	t_{RP}	40	-	50	-	60	-	70	-	ns	
RAS pulse width	t_{RAS}	60	10K	70	10K	80	10K	100	10K	ns	
RAS pulse width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	100	100K	ns	
RAS hold time	t_{RSH}	15	-	20	-	20	-	25	-	ns	
CAS precharge time (Fast Page Mode)	t_{CP}	10	-	10	-	10	-	10	-	ns	
CAS pulse width	t_{CAS}	15	10K	20	10K	20	10K	25	10K	ns	
CAS hold time	t_{CSH}	60	-	70	-	80	-	100	-	ns	
CAS to RAS precharge time	t_{CRP}	5	-	5	-	5	-	5	-	ns	
RAS to CAS delay time	t_{RCD}	20	45	20	50	20	60	25	75	ns	[5]
RAS to column address delay time	t_{RAD}	15	30	15	35	15	40	20	50	ns	[6]
Row address set-up time	t_{ASR}	0	-	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	15	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	15	-	20	-	ns	
Column address hold time from RAS	t_{AR}	50	-	55	-	60	-	75	-	ns	
Column address to RAS lead time	t_{RAL}	30	-	35	-	40	-	50	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	0	-	ns	[8]
Read command hold time reference to RAS	t_{RRH}	0	-	0	-	0	-	0	-	ns	[8]
Write command set-up time	t_{WCS}	0	-	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	10	-	10	-	10	-	15	-	ns	
Write command hold time from RAS	t_{WCR}	45	-	50	-	60	-	75	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	10	-	15	-	ns	
Write command to RAS lead time	t_{RWL}	15	-	20	-	20	-	25	-	ns	
Write command to CAS lead time	t_{CWL}	15	-	20	-	20	-	25	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	0	-	ns	

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C} \sim +70^\circ\text{C}$) [1] [2] [3] (Continued)

Parameter	Symbol	60 ns		70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15	-	15	-	15	-	20	-	ns	
Data-in hold time from RAS	t_{DHR}	50	-	55	-	60	-	75	-	ns	
CAS active delay from RAS precharge	t_{RPC}	5	-	5	-	5	-	5	-	ns	
RAS to CAS set-up time (CAS-before-RAS)	t_{CSR}	5	-	5	-	5	-	5	-	ns	
RAS to CAS hold time (CAS-before-RAS)	t_{CHR}	10	-	10	-	10	-	10	-	ns	
CAS precharge time (Refresh counter test)	t_{CPT}	30	-	35	-	40	-	50	-	ns	
WE to RAS precharge time (CAS-before-RAS)	t_{WRP}	10	-	10	-	10	-	10	-	ns	
WE hold time from RAS (CAS-before-RAS)	t_{WRH}	10	-	10	-	10	-	10	-	ns	
RAS to WE set-up time (Test Mode)	t_{WSR}	10	-	10	-	10	-	10	-	ns	[9] [10]
RAS to WE hold time (Test Mode)	t_{WHR}	10	-	10	-	10	-	10	-	ns	[9] [10]

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1. A start-up delay of 200 μs is required after power-up followed by a minimum of eight initialization cycles (RAS-only refresh or CAS-before-RAS refresh) before proper device operation is achieved. When using the internal refresh counter, a minimum of eight CAS-before-RAS initialization cycles is required.
2. AC measurements assume $t_T = 5\text{ ns}$.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL} .
4. Measured with a load circuit equivalent to 2 TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled by t_{CAC} .
6. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled by t_{AA} .
7. t_{OFF} (max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. The test mode is initiated by performing a WE and CAS-before-RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the data I/O pin will indicate a high level. If any internal bits are not equal, the data I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a RAS-only refresh cycle or a CAS-before-RAS refresh cycle.
10. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM F for AC Timing Waveforms