October 2001
Advanced Information

AS7C25512PFS32A
AS7C25512PFS36A

2.5V 512K × 32/36 pipeline burst synchronous SRAM

Features

- Organization: 524,288 words x 32/36 bits
- Fast clock speeds to 200MHz in LVTTL/LVCMOS
- Fast clock to data access: 3.0/3.5/4.0 ns
- Fast $\overline{OE}$ access time: 3.0/3.5/4.0 ns
- Fully synchronous register-to-register operation
- Single register "Flow-through" mode
- Single-cycle deselect
  - Dual-cycle deselect also available (AS7C25512PFD32A/ AS7C25512PFD36A)
- Pentium®* compatible architecture and timing
- Asynchronous output enable control
- 100-pin TQFP package
- 119-Ball BGA (7 x 17 Ball Grid Array Package)
- Byte write enables
- Multiple chip enables for easy expansion
- 2.5V core power supply
- 2.5V I/O operation
- NTD™* pipeline architecture available (AS7C25512NTD32A/ AS7C25512NTD36A)

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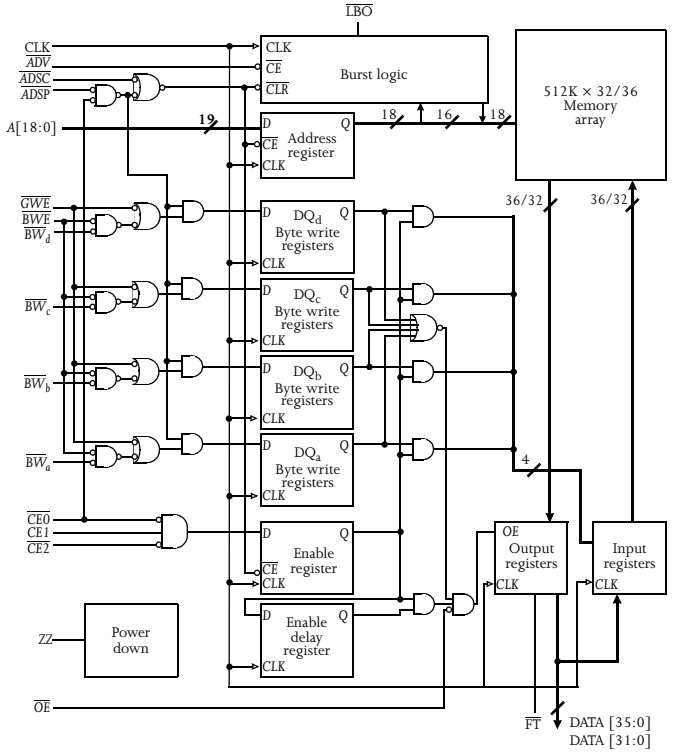
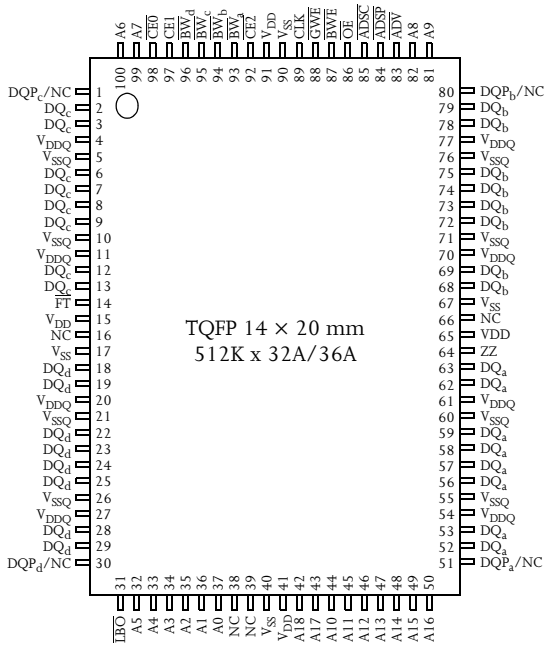
Logic Block Diagram:



Pin Arrangements:



Note: Pins 1,30,51,80 are NC for ×32

Selection guide	-200	-166	-100	Units
Minimum cycle time	5	6	10	ns
Maximum clock frequency	200	166	100	MHz
Maximum pipelined clock access time	3.0	3.5	4.0	ns
Maximum operating current	280	230	150	mA
Maximum standby current	100	70	50	mA
Maximum CMOS standby current (DC)	30	30	30	mA

Pin Configuration

119 BGA Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	$\overline{FT}$	A	A	V_{DD}	A	A	NC
D	DQC	DQPc	V_{SS}	NC	V_{SS}	DQpb	DQb
E	DQC	DQc	V_{SS}	$\overline{CE0}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQC	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQC	DQc	V_{SS}	$\overline{GWE}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	VDD	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BWE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DQpd	V_{SS}	A0	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	V_{DD}	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: For P/N AS7C25512PFS32A, 4 of the I/O Pins must be left open (N.C.)