



# Triple 4-3-3 Input NOR Gate

**ELECTRICALLY TESTED PER:  
5962-8756401**

The 10H506 is a Triple 4-3-3 input **NOR** gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply.

**2**

- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

**PIN ASSIGNMENTS**

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
V <sub>CC1</sub>	1	5	2	GND
B <sub>OUT</sub>	2	6	3	51 Ω to V <sub>TT</sub>
A <sub>OUT</sub>	3	7	4	51 Ω to V <sub>TT</sub>
A <sub>IN</sub>	4	8	5	51 Ω to V <sub>TT</sub>
A <sub>IN</sub>	5	9	7	OPEN
A <sub>IN</sub>	6	10	8	OPEN
A <sub>IN</sub>	7	11	9	OPEN
V <sub>EE</sub>	8	12	10	V <sub>EE</sub>
B <sub>IN</sub>	9	13	12	OPEN
B <sub>IN</sub>	10	14	13	51 Ω to V <sub>TT</sub>
B <sub>IN</sub>	11	15	14	OPEN
C <sub>IN</sub>	12	16	15	OPEN
C <sub>IN</sub>	13	1	17	OPEN
C <sub>IN</sub>	14	2	18	51 Ω to V <sub>TT</sub>
C <sub>OUT</sub>	15	3	19	51 Ω to V <sub>TT</sub>
V <sub>CC2</sub>	16	4	20	GND

**BURN - IN CONDITIONS:**  
**V<sub>TT</sub> = -2.0 V MAX/ -2.2 V MIN**  
**V<sub>EE</sub> = -5.7 V MAX/ -5.2 V MIN**

## Military 10H506

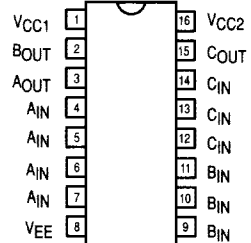


**AVAILABLE AS**

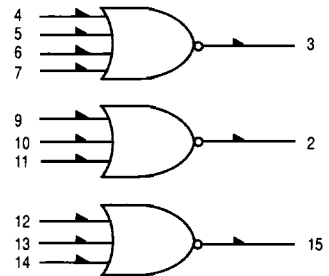
- 1) JAN: N/A
  - 2) SMD: 5962-8756401
  - 3) 883: 10H506/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

**PACKAGE: CERDIP: E**  
**CERFLAT: F**  
**LCC: 2**

The letter "M" appears before the slash on LCC.

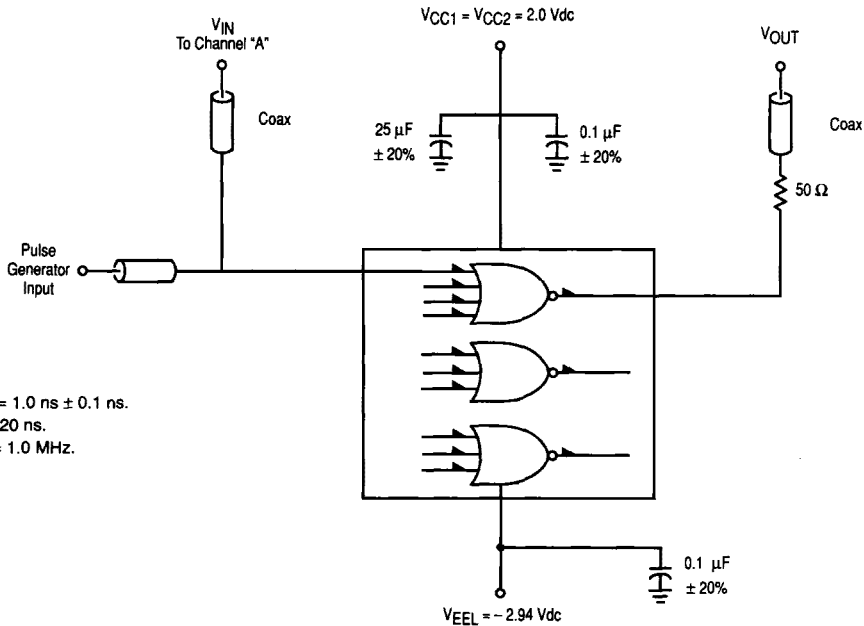


**LOGIC DIAGRAM**



# 10H506

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## NOTES

1.  $t_r = t_f = 1.0 \text{ ns} \pm 0.1 \text{ ns}$ .
2.  $P_W \geq 20 \text{ ns}$ .
3.  $P_{RF} = 1.0 \text{ MHz}$ .

## NOTES

1. All input and output cables to the scope are equal lengths of  $50 \Omega$  coaxial cable. Wire length should be  $\leq 0.250$  (6.35 mm) from  $TP_{IN}$  to input pin and  $TP_{OUT}$  to output pin.
2. Outputs not under test should be connected to a  $100 \Omega$  resistor to ground.

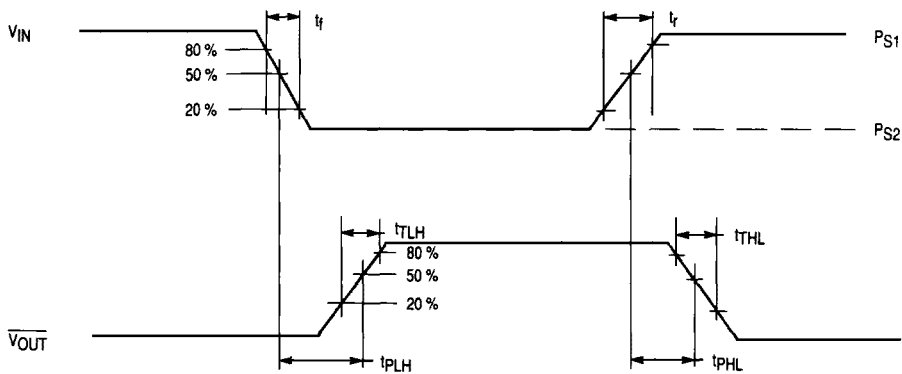


Figure 1. Switching Test Circuit and Waveforms

# 10H506 QUIESCENT LIMIT TABLE \*

## \* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	PS1	PS2	VEE1	VEE2	VEEL	
T <sub>A</sub> = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	
T <sub>A</sub> = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	
T <sub>A</sub> = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V									
	Functional Parameters:	Subgroup 1	Subgroup 2	Subgroup 3	Subgroup 1	Subgroup 2	Subgroup 3		V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	V <sub>EE1</sub>	V <sub>EE2</sub>	V <sub>CC</sub>	P.U.T.		
V <sub>OH</sub>	High Output Voltage	Min -1.01 Max -0.78	Min -0.86 Max -0.65	Min -1.06 Max -0.84	V	4-7 9-14	8	1, 16	2, 3, 15									
V <sub>OL</sub>	Low Output Voltage	Min -1.95 Max -1.58	Min -1.95 Max -1.363	Min -1.95 Max -1.61	V	4-7 9-14	8	1, 16	2, 3, 15									
V <sub>OH1</sub>	High Output Voltage	Min -1.01 Max -0.78	Min -0.86 Max -0.65	Min -1.06 Max -0.84	V	4-7 9-14	8	1, 16	2, 3, 15									
V <sub>OL1</sub>	Low Output Voltage	Min -1.95 Max -1.58	Min -1.95 Max -1.363	Min -1.95 Max -1.61	V	4-7 9-14	8	1, 16	2, 3, 15									
I <sub>EE</sub>	Power Supply Current	- 21	- 23	- 23	mA		8	1, 16	8									
I <sub>IH1</sub>	Input Current High	310	500	500	μA		8	1, 16	4-7 9-14									
I <sub>IL</sub>	Input Current Low	0.5	0.3	0.5	μA		8	1, 16	4-7 9-14									

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Test Temperature	Test Voltage Values (Volts)									
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	PS1	PS2	VEE1	VEE2	VEEL	VEEL
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T <sub>A</sub> = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V <sub>CC</sub> = 2.0 V, Output Load = 100 $\Omega$ to GND					
		Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 12	Subgroup 13	Subgroup 14							
t <sub>TLH</sub>	Rise Time	Min	Max	Min	Max	Min	Max	ns	V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>CC</sub>	VEEL	P.U.T.	
t <sub>THL</sub>	Fall time	0.6	1.8	0.55	1.9	0.5	1.7	ns	6	3	1, 16	8	2, 15	
t <sub>PHL</sub>	Propagation Delay High to Low	0.6	1.8	0.55	1.9	0.5	1.7	ns	10	2	1, 16	8	3, 15	
t <sub>PLH</sub>	Propagation Delay Low to High	0.5	1.75	0.55	1.8	0.5	1.7	ns	13	15	1, 16	8	2, 3	
		0.5	1.75	0.55	1.8	0.5	1.7	ns	13	15	1, 16	8	2, 3	