

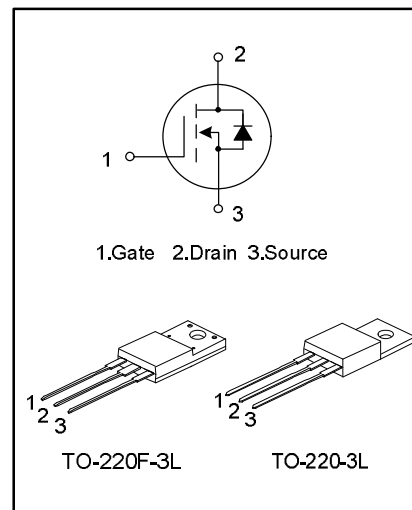
**5A, 600V N-CHANNEL MOSFET**
**GENERAL DESCRIPTION**

SVD5N60AT/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

**FEATURES**

- \* 5A,600V, $R_{DS(on)}$  (typ) =2.0 $\Omega$ @ $V_{GS}=10V$
- \* Low gate charge
- \* Low  $C_{rss}$
- \* Fast switching
- \* Improved dv/dt capability


**ORDERING SPECIFICATIONS**

| Part No.  | Package    | Marking   | Shipping    |
|-----------|------------|-----------|-------------|
| SVD5N60AT | TO-220-3L  | SVD5N60AT | 50Unit/Tube |
| SVD5N60AF | TO-220F-3L | SVD5N60AF | 50Unit/Tube |

**ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)**

| Parameter  | Symbol    | SVD5N60AT | SVD5N60AF | Unit |
|--|-----------|-----------|-----------|------|
| Drain-Source Voltage                             | $V_{DS}$  | 600       |           | V    |
| Gate-Source Voltage                              | $V_{GS}$  | $\pm 30$  |           | V    |
| Drain Current                                    | $I_D$     | 5.0       |           | A    |
| Power Dissipation(Tc=25°C)<br>-Derate above 25°C | $P_D$     | 100       | 33        | W    |
|  |           | 0.8       | 0.26      |      |
| Single Pulsed Avalanche Energy (Note 1)          | EAS       | 330       |           | mJ   |
| Repetitive Avalanche Energy (Note 2)             | EAR       | 7.3       |           | mJ   |
| Operation Junction Temperature                   | $T_J$     | -55~+150  |           | °C   |
| Storage Temperature                              | $T_{stg}$ | -55~+150  |           | °C   |

**THERMAL CHARACTERISTICS**

| Parameter                               | Symbol           | SVD5N60AT | SVD5N60AF | Unit |
|---|------------------|-----------|-----------|------|
| Thermal Resistance, Junction-to-Case    | R <sub>θJC</sub> | 1.25      | 3.79      | °C/W |
| Thermal Resistance, Junction-to-Ambient | R <sub>θJA</sub> | 62.5      | 62.5      | °C/W |

**ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)**

| Parameter                                | Symbol              | Test conditions  | Min. | Typ. | Max. | Unit |
|--|---------------------|--|------|------|------|------|
| Drain -Source Breakdown Voltage          | BVDSS               | V <sub>GS</sub> =0V, I <sub>D</sub> =250μA   | 600  | --   | --   | V    |
| Drain-Source Leakage Current             | I <sub>DSS</sub>    | V <sub>DS</sub> =600V, V <sub>GS</sub> =0V   | --   | --   | 10   | μA   |
| Gate-Source Leakage Current              | I <sub>GSS</sub>    | V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V   | --   | --   | ±100 | nA   |
| Gate Threshold Voltage                   | V <sub>GS(th)</sub> | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =250μA                              | 2.0  | --   | 4.0  | V    |
| Static Drain- Source On State Resistance | R <sub>DS(on)</sub> | V <sub>GS</sub> =10V, I <sub>D</sub> =2A   | --   | 2.0  | 2.4  | Ω    |
| Input Capacitance                        | C <sub>iss</sub>    | V <sub>DS</sub> =25V, V <sub>GS</sub> =0V,<br>f=1.0MHZ                                 | --   | 672  | --   | pF   |
| Output Capacitance                       | C <sub>oss</sub>    |  | --   | 66   | --   |      |
| Reverse Transfer Capacitance             | C <sub>rss</sub>    |  | --   | 4.7  | --   |      |
| Turn-on Delay Time                       | t <sub>d(on)</sub>  | V <sub>DD</sub> =300V, I <sub>D</sub> =4.4A,<br>R <sub>G</sub> =25Ω<br><br>(Note 3,4)  | --   | 27   | --   | ns   |
| Turn-on Rise Time                        | t <sub>r</sub>      |  | --   | 19   | --   |      |
| Turn-off Delay Time                      | t <sub>d(off)</sub> |  | --   | 160  | --   |      |
| Turn-off Fall Time                       | t <sub>f</sub>      |  | --   | 22   | --   |      |
| Total Gate Charge                        | Q <sub>g</sub>      | V <sub>DS</sub> =480V, I <sub>D</sub> =4.4A,<br>V <sub>GS</sub> =10V<br><br>(Note 3,4) | --   | 19.8 | --   | nC   |
| Gate-Source Charge                       | Q <sub>gs</sub>     |  | --   | 4    | --   |      |
| Gate-Drain Charge                        | Q <sub>gd</sub>     |  | --   | 7.2  | --   |      |

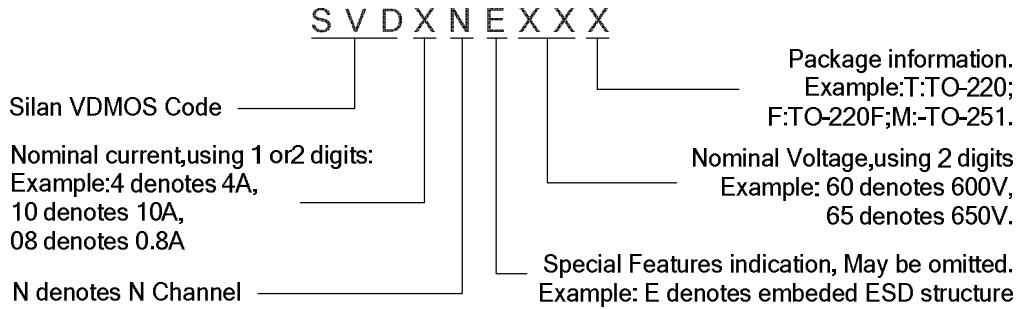
**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

| Parameter                 | Symbol          | Test conditions  | Min. | Typ. | Max. | Unit |
|---------------------------|-----------------|--|------|------|------|------|
| Continuous Source Current | I <sub>S</sub>  | Integral Reverse P-N<br>Junction Diode in the<br>MOSFET                            | --   | --   | 5.0  | A    |
| Pulsed Source Current     | I <sub>SM</sub> |  | --   | --   | 16   |      |
| Diode Forward Voltage     | V <sub>SD</sub> | I <sub>S</sub> =5.0A, V <sub>GS</sub> =0V  | --   | --   | 1.4  | V    |
| Reverse Recovery Time     | T <sub>rr</sub> | I <sub>S</sub> =5.0A, V <sub>GS</sub> =0V,<br>dI <sub>F</sub> /dt=100A/μs (Note 3) | --   | 300  | --   | ns   |
| Reverse Recovery Charge   | Q <sub>rr</sub> |  | --   | 2.2  | --   | μC   |

Notes:

- L=30mH, I<sub>AS</sub>=4.4A, V<sub>DD</sub>=85V, R<sub>G</sub>=25Ω, starting T<sub>J</sub>=25°C;
- Repetitive Rating: Pulse width limited by maximum junction temperature;
- Pulse Test: Pulse width ≤300μs, Duty cycle ≤2%;
- Essentially independent of operating temperature.

NOMENCLATURE



TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

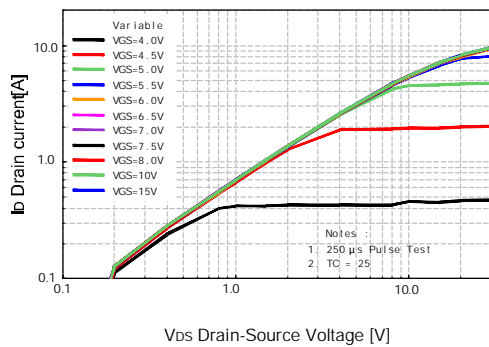


Figure 2. Transfer Characteristics

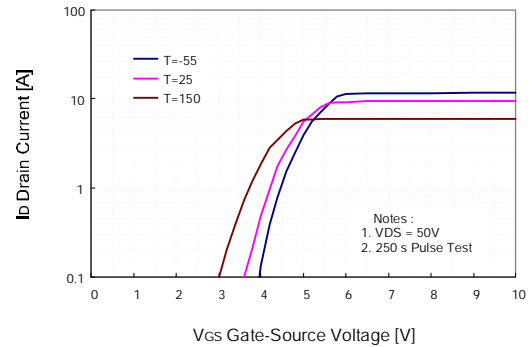


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

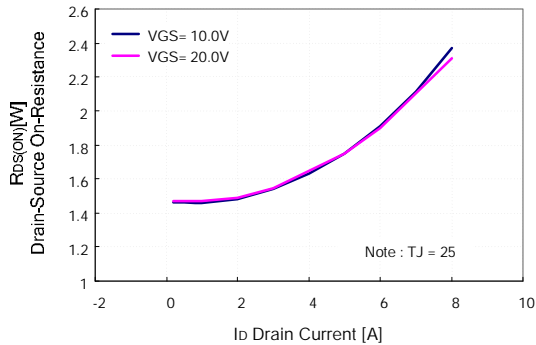
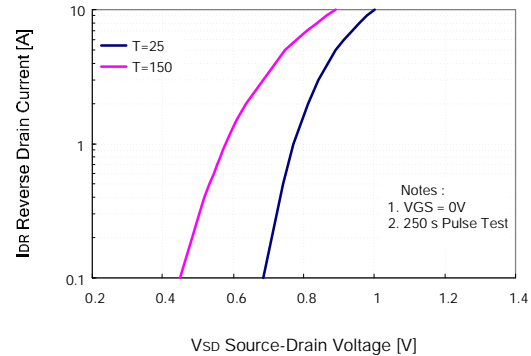


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS (continued)

Figure 5. Capacitance Characteristics

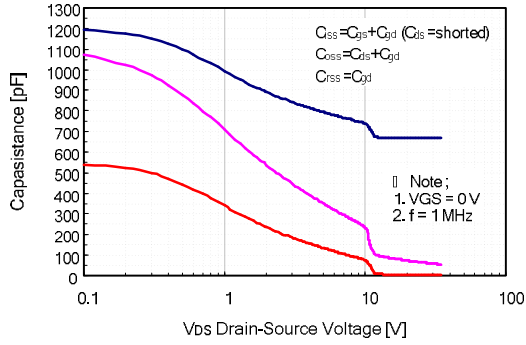


Figure 6. Gate Charge Characteristics

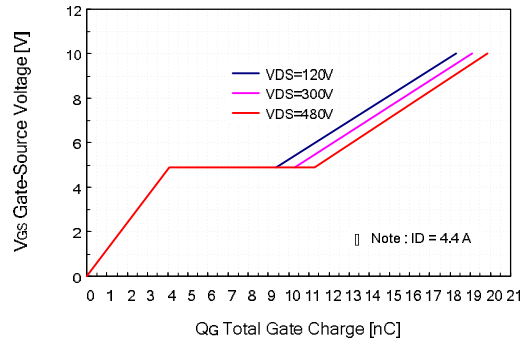


Figure 7. Breakdown Voltage Variation vs. Temperature

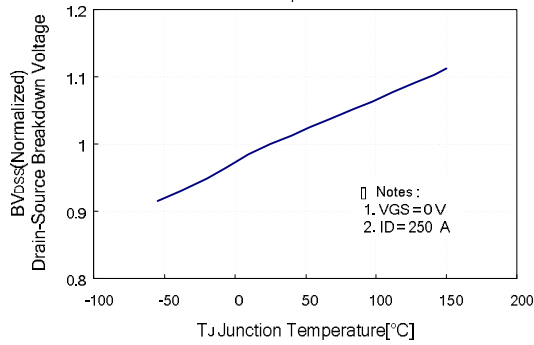
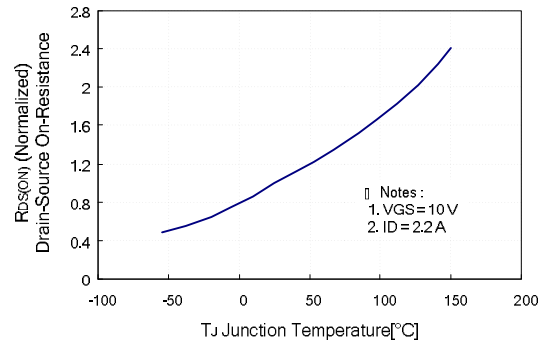
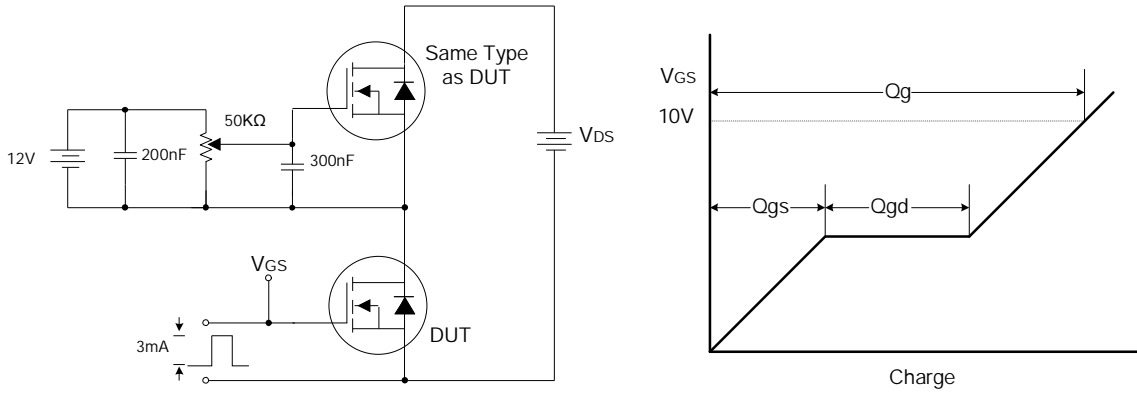


Figure 8. On-resistance Variation vs Temperature

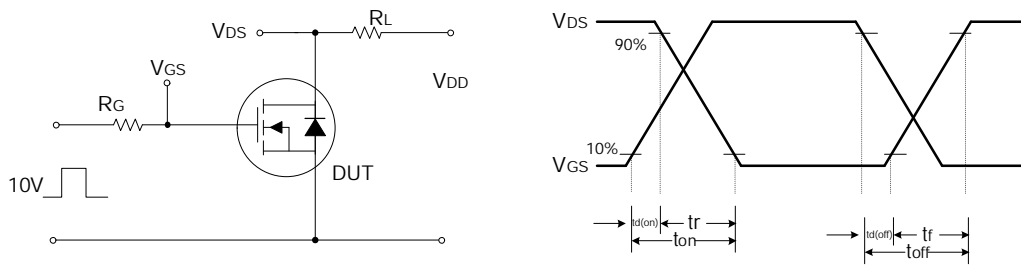


TYPICAL TEST CIRCUIT

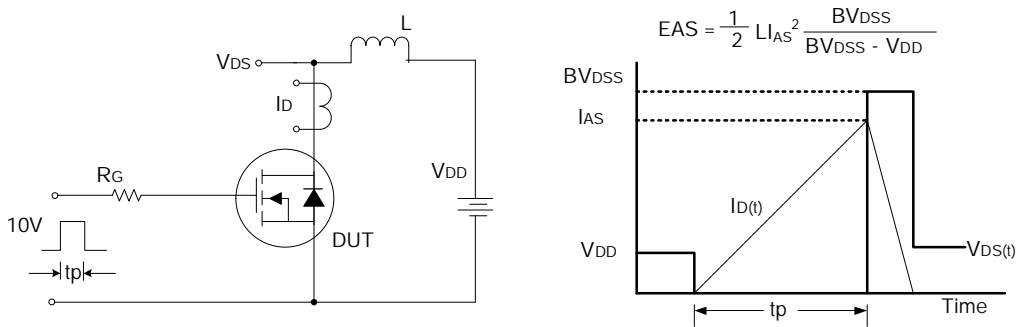
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



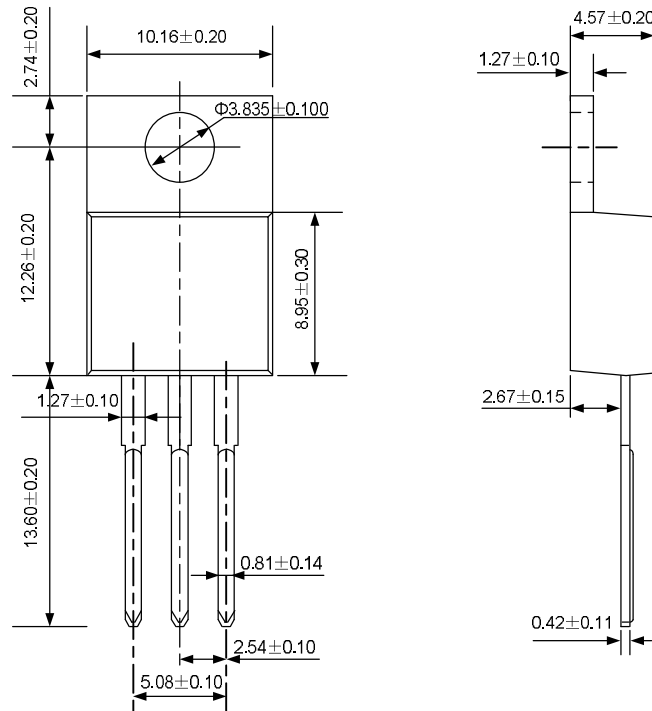
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

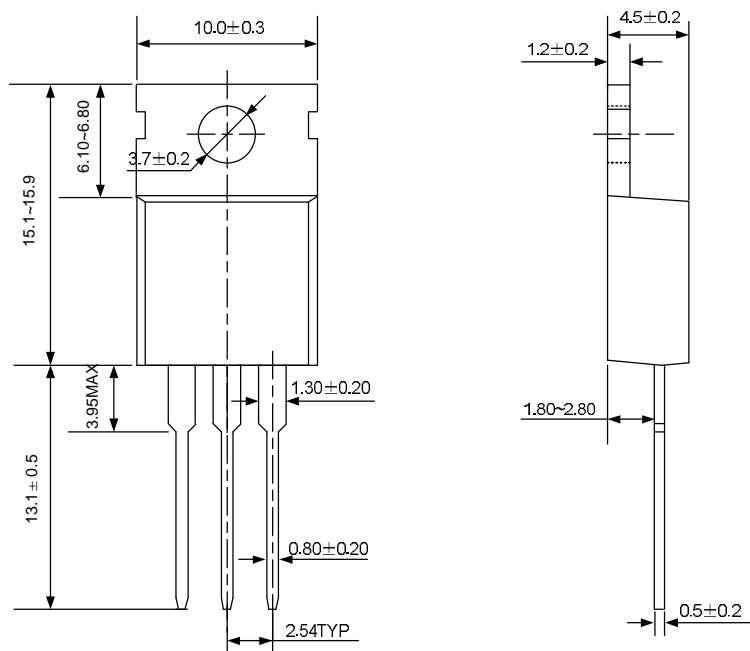
TO-220-3L(One)

UNIT: mm



TO-220-3L (Two)

UNIT: mm



PACKAGE OUTLINE (continued)

