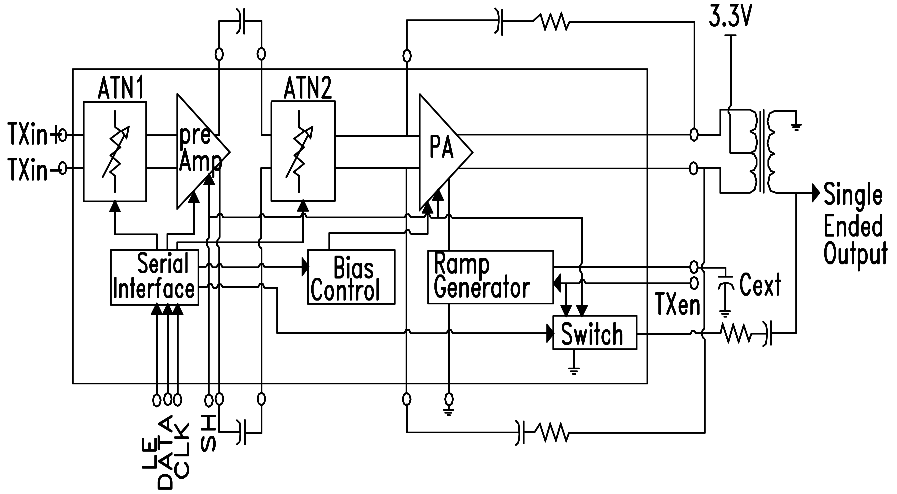
S510066

UPSTREAM CATV AMPLIFIER

FEATURES

- **SINGLE 3.3 V SUPPLY OPERATION**
- **LOW POWER CONSUMPTION:**
  135 mA typical @ 63 dBmV output
- **63 dB DYNAMIC RANGE:**
  -0.5 to 63 dBmV output
- **PROGRAMMABLE GAIN IN 0.5 dB STEPS**
- **ULTRA LOW ON/OFF TRANSIENTS**
- **DOCSIS 2.0 and RoHS compliant**

FUNCTIONAL DIAGRAM



DESCRIPTION

The S510066 is a high performance, low cost, low power programmable power amplifier designed for use in CATV upstream applications. The amplifier operates over a frequency range from 5 to 65 MHz and has a maximum output of 63 dBmV. A 3-wire serial interface controls the gain over a 63.5 dB range in 0.5 dB steps. The S510066 is available in both a thermally enhanced QFN28 5x5 quad package-55Z and in a TSSOP20 packge.The product is DOCSIS and RoHS compliant.

APPLICATIONS

- Set-Top Boxes
- Cable Telephony
- Cable Modems
- Catv infra structure

RF ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = 3.3 V, unless otherwise specified)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
RF Performance					
Av	Gain F_{IN} = 5 MHz, Gain Code = 127	dB	26	28	
Av	Gain F_{IN} = 65 MHz, Gain Code = 127	dB	25.2	29.2	
	Gain Flatness, V_{OUT} = 61 dBmV, F_{IN} = 5 to 42 MHz	dB		0.5	1
	Gain Flatness, V_{OUT} = 61 dBmV, F_{IN} = 5 to 65 MHz	dB		0.8	1.5
	Attenuation Range, Gain Code = 0 to 127	dB		63.5	
	Attenuation Step Size, Gain Code = 0 to 127	dB		0.5	
	Output Return Loss, 5 to 65 MHz	dB		15	10
	Isolation, 5 to 65 MHz, TXEN = 0 (Transmit Disable Mode)	dB		-69	
	Transmit Mode Noise, 5 to 65 MHz, BW = 160 KHz, Gain Code = 127 to 64	dBmV		-38	-35
	Transmit Mode Noise, 5 to 65 MHz, BW = 160 KHz, Gain Code = 63 to 31	dBmV		-50	-47
	Transmit Mode Noise, 5 to 65 MHz, BW = 160 KHz, Gain Code = 31 to 0	dBmV		-53	-50
	Transmit Disable Mode Noise, 5 to 65 MHz, BW = 160 KHz, TXEN = 0	dBmV		-70	
HD2	2nd Harmonic Distortion, V_{OUT} = 61 dBmV, 5 to 65 MHz	dBc	-55	-60	
HD3	3rd Harmonic Distortion, V_{OUT} = 61 dBmV, 5 to 65 MHz	dBc	-50	-53	
HD3	3rd Harmonic Distortion, V_{OUT} = 57 dBmV, 5 to 65 MHz(@ 3.4V)	dBc		-58	

DC ELECTRICAL CHARACTERISTICS

SYMBOLS	PARAMETERS		UNITS	MIN	TYP	MAX
DC Performance						
V_{DD}	Supply Voltage		V	3.2	3.3	3.5
I_{DD}	Supply Current,	Gain Code = 127	mA		138	145
	TXEN = 1, D7 = 0, SH = 1	Gain Code = 63 to 0	mA		68	
I_{DD}	Supply Current, TXEN = 0, D7 = 0, SH = 1		mA		35	
I_{DD}	Supply Current, D7 = 0, SH = 1			uA		10
Logic Inputs						
V_{INH}	Input High Voltage		V	V_{DD} -0.4		
V_{INL}	Input Low Voltage		V			0.4

ABSOLUTE MAXIMUM RATINGS

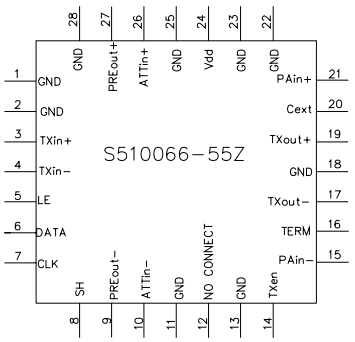
(T_C = 25°C unless otherwise noted)

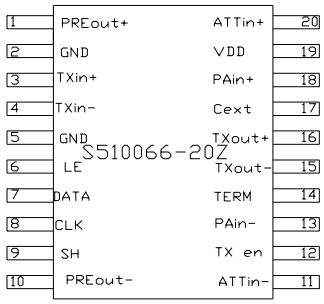
SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD} (GND)	Supply Voltage (GND)	V	-0.3 to +3.6
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-65 to 150
	Junction Temperature	°C	150
	Thermal Resistance (Ø ja)	°C/W	34

Note:

1. Operation in excess of any one of these parameters may result in permanent damage.

PIN ASSIGNMENTS



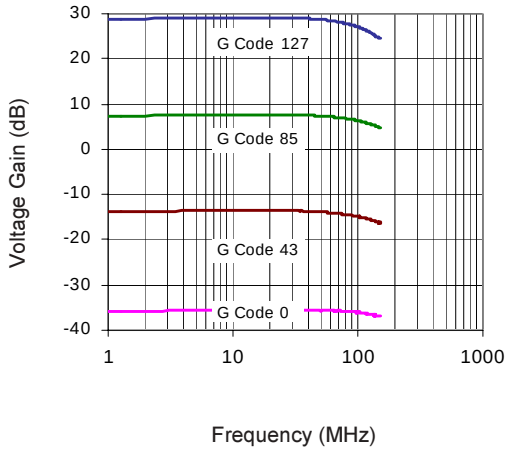


PIN FUNCTIONS

PIN NO. TSSOP 20	PIN NO. QFN28	PIN NAME	DESCRIPTION
5	1	GND	Ground.
2	2	GND	Ground.
3	3	TXin+	Positive input to the ATTN1 stage. Along with Txin-, the two ports form a differential impedance of 150 ohms.
4	4	TXin-	Negative input to the ATTN1 stage. Along with Txin+, the two ports form a differential impedance of 150 ohms.
6	5	LE	Serial Interface enable. TTL compatible input. See Serial Interface section.
7	6	DATA	Serial Interface data. TTL compatible input. See Serial Interface section.
8	7	CLK	Serial Interface clock. TTL compatible input. See Serial Interface section.
9	8	SH	Hardware shut down. Drive SH high to enable all chip functions given that D7=1.
10	9	PREout-	Negative output of the pre-amp. A DC blocking cap must be used to connect this pin to the input of ATTN2 stage.
11	10	ATTin-	Negative input of the ATTN2 stage.
	11	GND	Ground.
	12	No Connect	
	13	GND	Ground.
12	14	TXen	Transmit enable. Drive TXen high to turn on the output-amplifier stage.
13	15	PAin-	Negative input of the PA stage.
14	16	TERM	A resistor of 75 ohms and a bypass cap must be connected in series to the output of the transformer to ensure proper output impedance when output-amp is disabled.
15	17	TXout-	Negative output of the output-amp stage. Along with TXin+, the two ports form a differential impedance of 75 ohms.
	18	GND	Ground.
16	19	TXout+	Positive output of the output-amp stage. Along with TXin-, the two ports form a differential impedance of 75 ohms.
17	20	Cext	An external capacitor to ground is connected to control the ramp-up and ramp-down during Transmit enable and disable.
18	21	PAin+	Positive input of the PA stage.
	22	GND	PA ground.
	23	GND	Ground.
19	24	VDD	3.3 V supply for the pre-amp stage.
	25	GND	Pre-amp ground.
20	26	ATTin+	Positive input of the ATTN2 stage.
1	27	PREout+	Positive output of the pre-amp. A DC blocking cap must be used to connect this pin to the input of ATTN2 stage.
	28	GND	Ground.

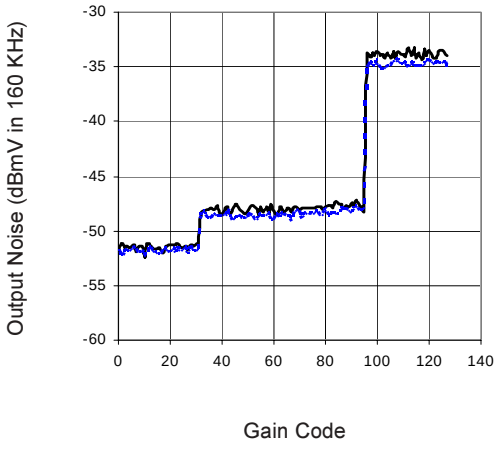
TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN vs. FREQUENCY

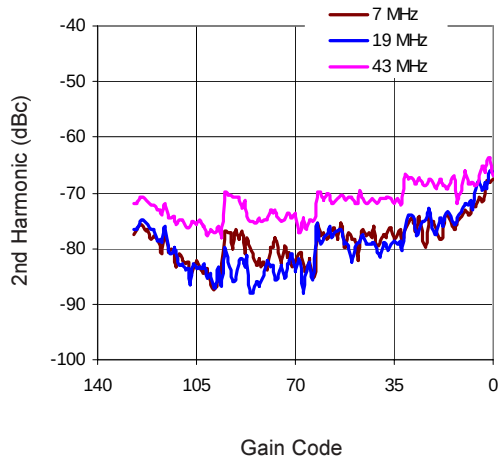


VOLTAGE GAIN vs. GAIN CODE

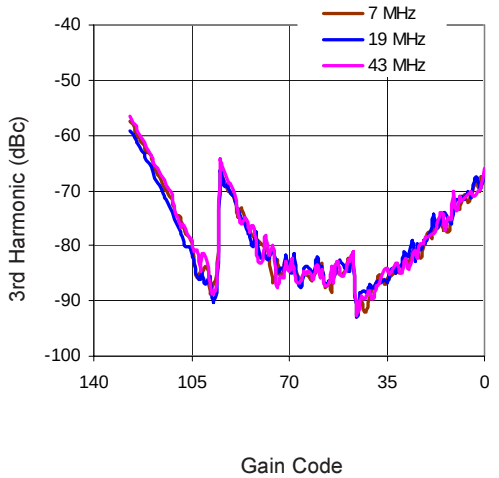
TRANSMIT NOISE vs. GAIN CODE



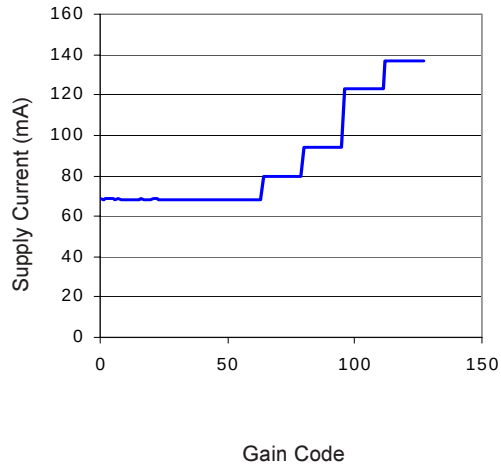
2ND HARMONIC vs. GAIN CODE
(POUT = 61 dBmV @ GCW = 127)



3RD HARMONIC vs. GAIN CODE
(POUT = 61 dBmV @ GCW = 127)



SUPPLY CURRENT vs. GAIN CODE



FUNCTIONAL DESCRIPTION

Upstream CATV Amplifier
The upstream CATV amplifier consists of an input attenuator (ATTN1), pre-amp, intermediate attenuator (ATTN2), power amp, serial data interface, bias control, ramp generator, and a switch. The amplifier and the attenuator blocks are capable of providing a gain range of 63.5 dB with 0.5 db steps across the specified frequencies of operation. The gain and current of the whole chain is determined by a 7 bit word programmed using the serial data interface.

Input Interface
The differential input impedance of the upstream CATV amplifier is 150 ohms. The input anti-aliasing filter should be designed to the same impedance for proper operation. The output impedance of the DAC should also be set accordingly. In order to achieve the specified performance, the inputs should be driven differentially.

Output Interface
The differential output impedance of the upstream CATV amplifier is 75 ohms provided that the suggested value of the shunt feedback resistor of the power amp stage is used. The differential output is converted to a single-ended output with a 1:1 turn ratio transformer.

Switch
During transmit disable mode, the 75 ohm output impedance is maintained by switching in a shunt 75 ohm resistor connected from the single-ended output of the transformer to ground. The switch is toggled by the TXen pin, SH pin, and D7 bit. When TXen and SH is high and D7 = 0 (transmit mode), the switch is open. It is closed when TXen or SH is low or D7 = 1.

Power Amp (PA)
The power amplifier stage is a Class A differential amplifier with off-chip shunt feedback and on-chip series feedback. It is capable of providing an output level of 63 dBmV. The 3.3 V bias of the PA stage comes from the center-tap of the 1:1 turn ratio transformer. The transformer will suppress the even-order distortion and the transients caused by enabling and disabling the PA.

Ramp Generator
This block is a simple RC charging circuit consisting of an internal 1K ohm resistor and an external capacitor Cext. This circuit controls the ramp up and down time of the PA stage during bursts.

Bias Control
The bias control sets the current of the PA stage at various gain states. In the lower gain states, the current of the PA is reduced and overall power consumption decreases.

Serial Interface
The serial interface becomes active when LE (latch enable) is low. The overall gain, current, and chip shutdown are determined by the programming of the bits D0 - D7. See Table 1, Table 2, Table 3, and Serial-Interface Timing Diagram for programming details.

FUNCTIONAL DESCRIPTION (CON'T)

Table 1. Attenuator States

TXen	SH	D7	D6	D5	D4	D3	D2	D1	D0	Gain Code (Decimal)	State
X	0	X	X	X	X	X	X	X	X	X	Shut-down, Transmit Disable
0	1	X	X	X	X	X	X	X	X	X	Transmit Disable
X	X	1	X	X	X	X	X	X	X	X	Shut-down, Transmit Disable
1	1	0	1	1	1	1	1	1	1	127	Av = 28.0 dB
1	1	0	1	1	1	1	1	0	1	125	Av = 27.0 dB
1	1	0	1	1	1	1	0	0	1	121	Av = 25.0 dB
1	1	0	1	1	0	0	1	0	1	101	Av = 15.0 dB
1	1	0	1	1	0	0	0	0	1	97	Av = 13.0 dB
1	1	0	1	0	1	1	1	1	1	95	Av = 12.0 dB
1	1	0	1	0	1	1	1	0	1	93	Av = 11.0 dB
1	1	0	1	0	1	0	0	0	1	81	Av = 5.0 dB
1	1	0	1	0	0	0	0	0	1	65	Av = -3.0 dB
1	1	0	0	1	1	1	1	1	1	63	Av = -4.0 dB
1	1	0	0	1	1	1	1	0	1	61	Av = -5.0 dB
1	1	0	0	1	0	1	0	0	1	41	Av = -15.0 dB
1	1	0	0	1	0	0	0	0	1	33	Av = -19.0 dB
1	1	0	0	0	1	1	1	1	1	31	Av = -20.0 dB
1	1	0	0	0	1	1	1	0	1	29	Av = -21.0 dB
1	1	0	0	0	1	0	1	0	1	21	Av = -25.0 dB
1	1	0	0	0	0	0	0	0	1	1	Av = -35.0 dB
1	1	0	0	0	0	0	0	0	0	0	Av = -35.5 dB

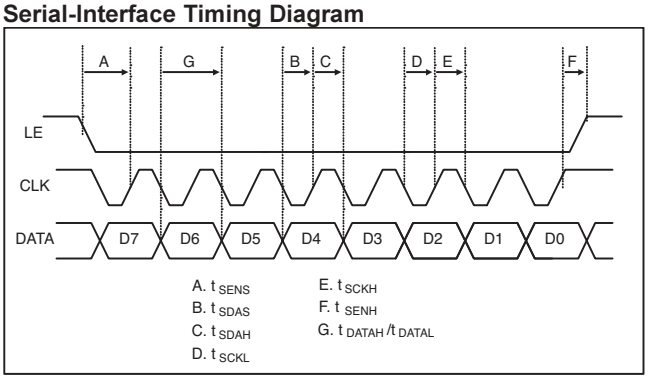
Table 2. Attenuator Values

BIT	ATTENUATION (dB)
D0	0.5
D1	1.0
D2	2.0
D3	4.0
D4	8.0
D5	16.0
D6	32.0

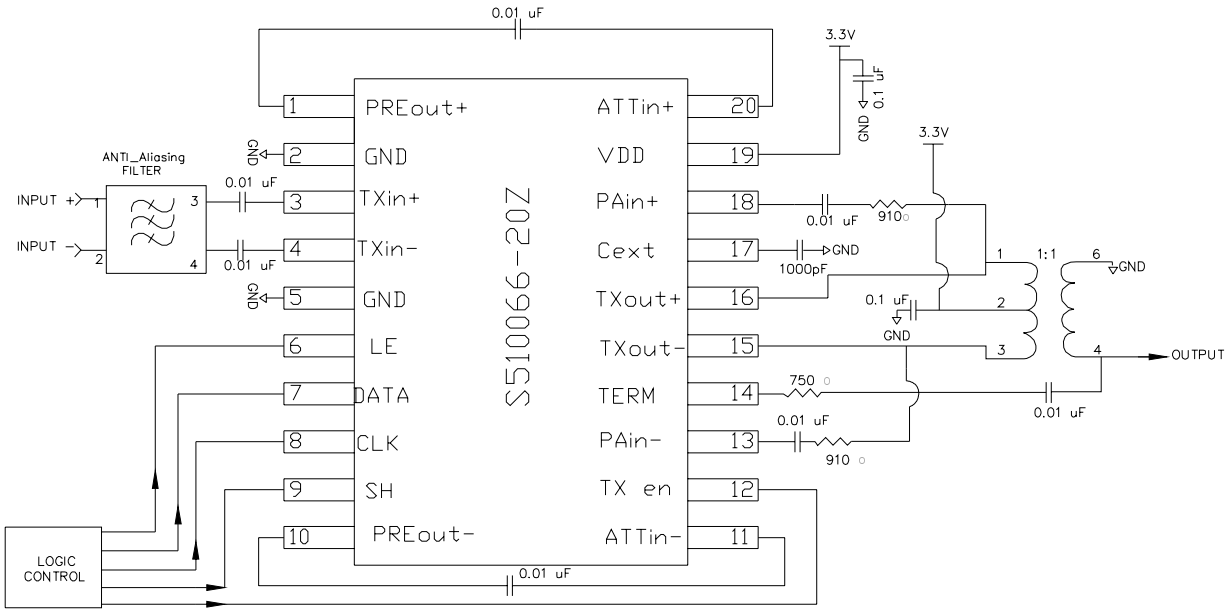
Table 3. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	Shut Down
6	D6	Gain Control, Bit 6
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0

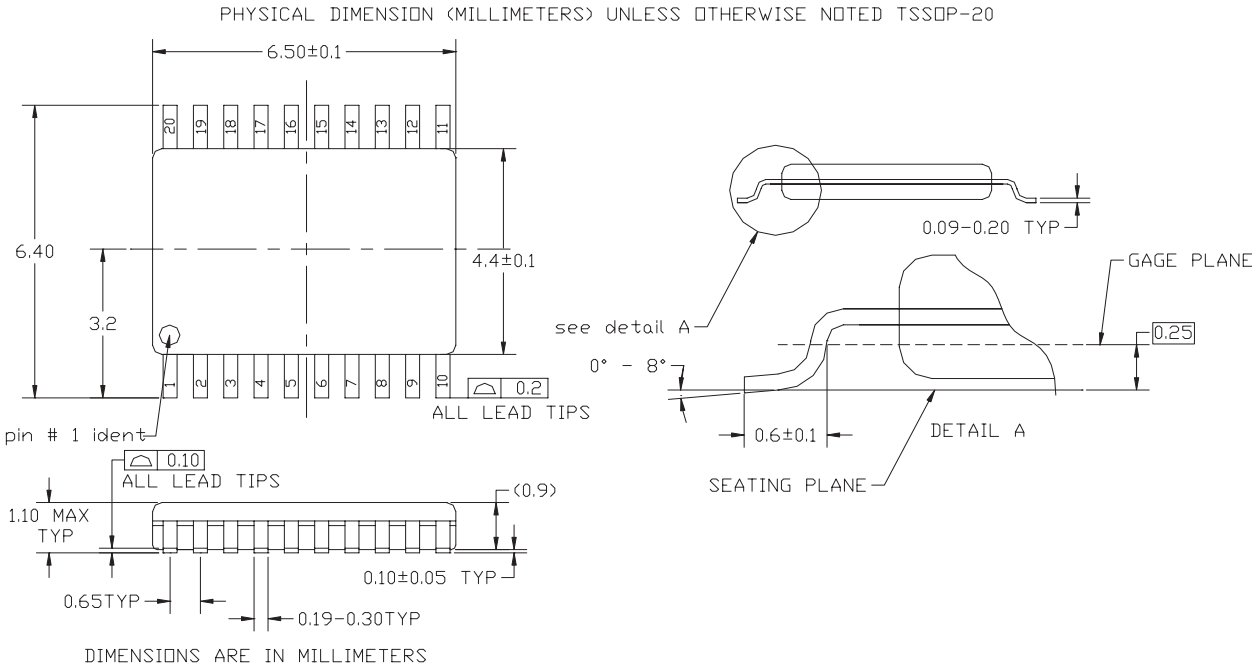
Serial-Interface Timing Diagram



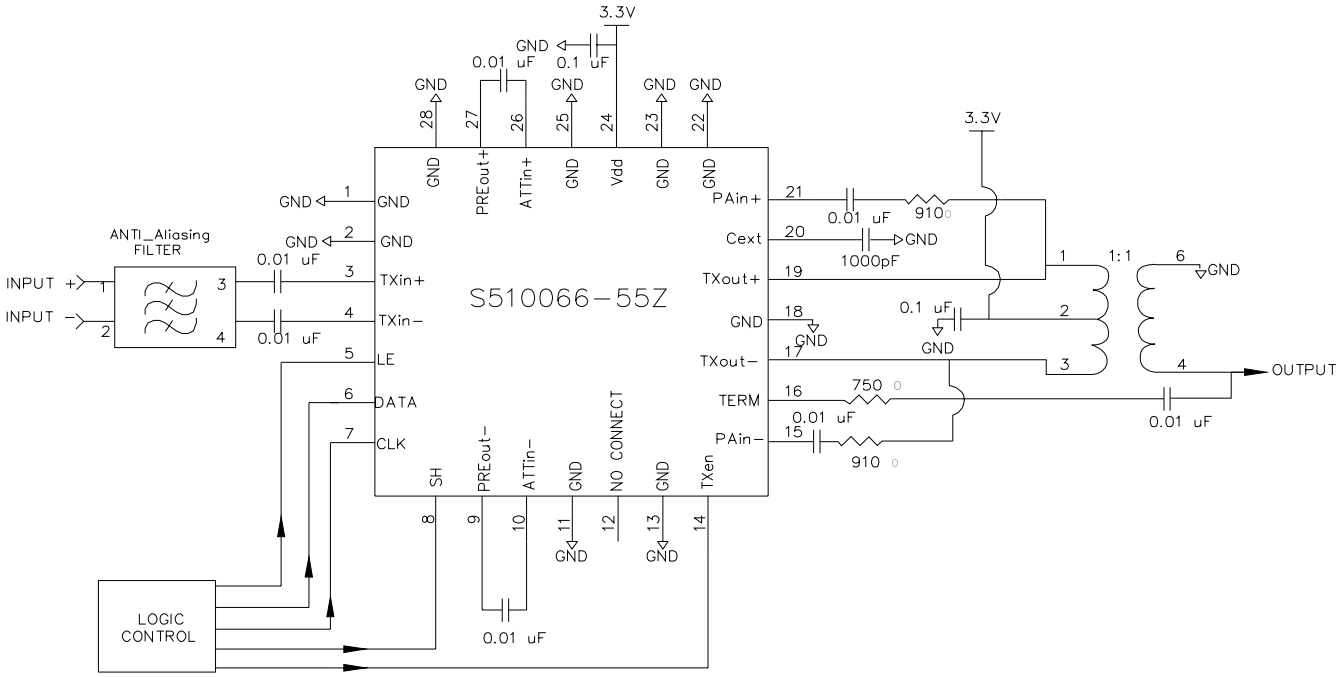
TYPICAL APPLICATION CIRCUIT 20 PIN



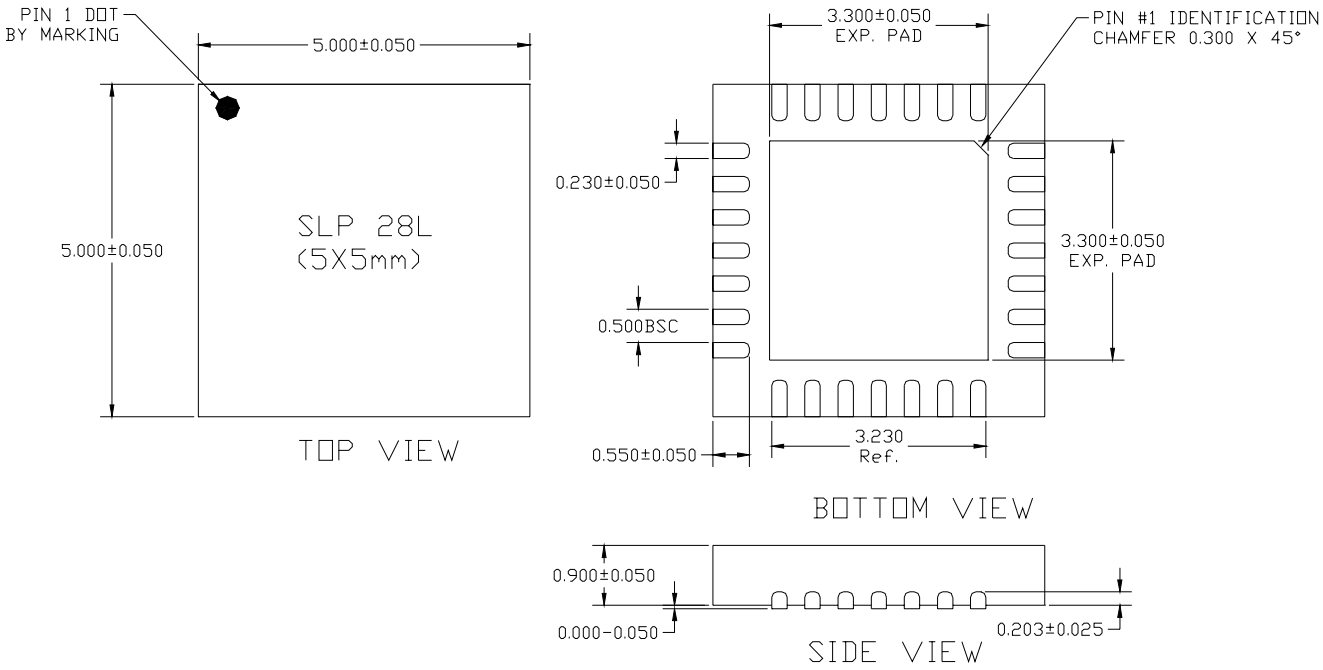
PACKAGE INFORMATION TSSOP-20 (CON'T)



TYPICAL APPLICATION CIRCUIT



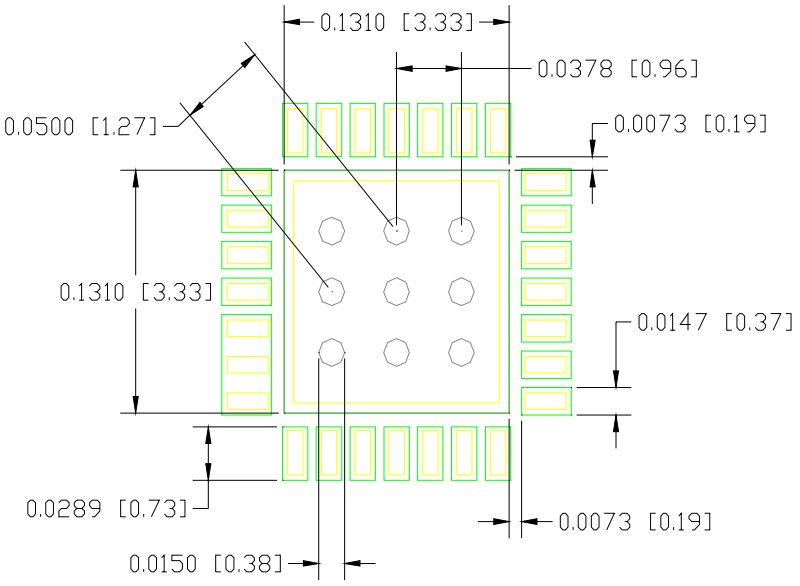
PACKAGE INFORMATION QFN 28 (Units in mm)



PACKAGE INFORMATION (CON'T)

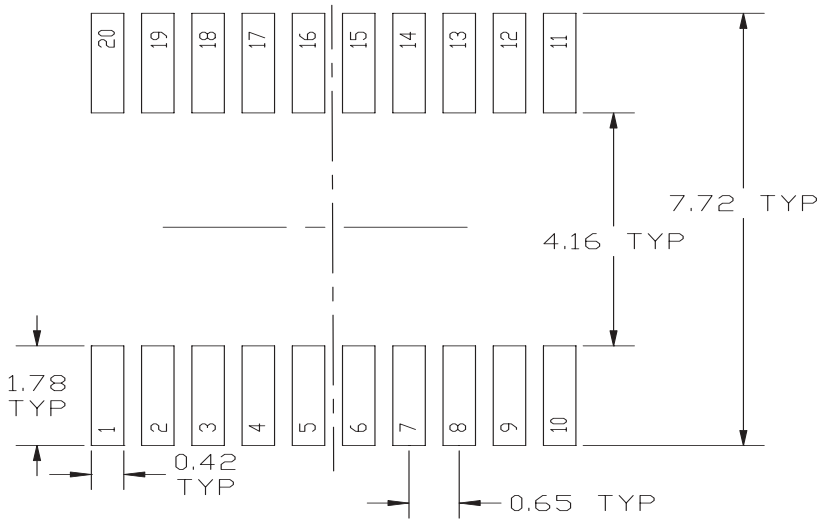
1. Dimensions and tolerances conform to ASME Y14.5-1994.
2. All dimensions are in millimeters. All angles are in degrees.
3. The exposed thermal pad is also an electrical ground .

LAND PATTERN FOR TERMINALS AND THERMAL/GROUND PAD



LAND PATTERN FOR TSSOP-20 (CON'T)

PHYSICAL DIMENSION (MILLIMETERS) UNLESS OTHERWISE NOTED TSSOP-20



DATA SUBJECT TO CHANGE WITHOUT NOTICE