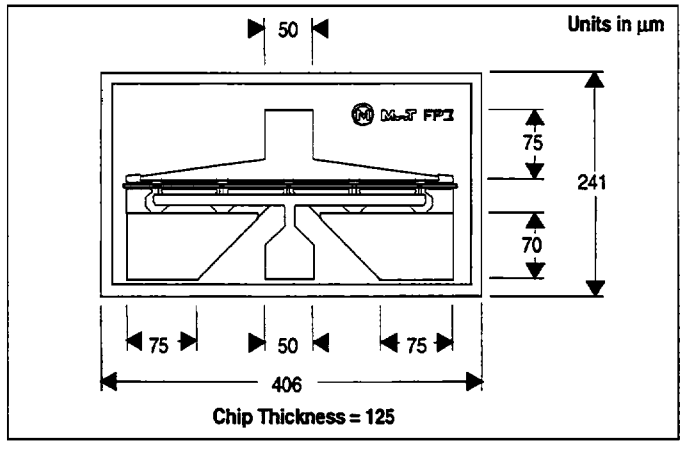
MICROWAVE TECHNOLOGY

MwT-3
26 GHz High Power GaAs FET



- +21 DBM OUTPUT POWER AT 12 GHZ
- 11 DB SMALL SIGNAL GAIN AT 12 GHZ
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 300 MICRON GATE WIDTH
- CHOICE OF CHIP AND THREE PACKAGE TYPES

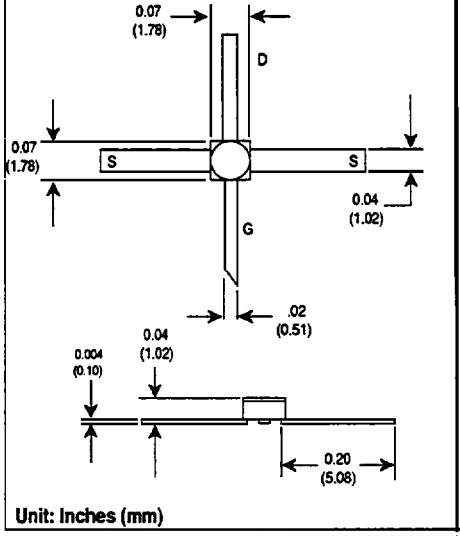
DESCRIPTION

The MwT-3 is a GaAs MESFET device whose nominal quarter-micron gate length and 300 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 26 GHz frequency range with power outputs ranging from +18 to +21 dBm. The straight gate geometry of the MwT-3 makes it equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

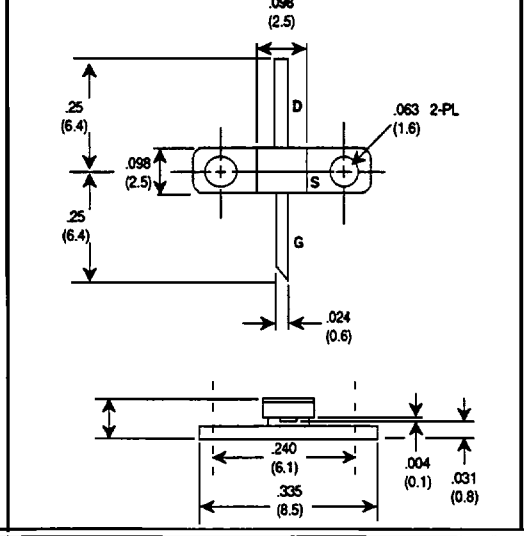
RF SPECIFICATIONS AT Ta = 25°C

				MwT-3 HP MwT-370 HP MwT-371 HP MwT-373 HP	
SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1dB Compression VDS=6.0V IDS=0.6 x IDSS	12 GHz	dBm	20.0	21.0
SSG	Small Signal Gain VDS=6.0V IDS=0.6 x IDSS	12 GHz	dB	10.0	11.0
PAE	Power Added Efficiency VDS=6.0V IDS=0.6 x IDSS	12 GHz	%	30	35
IDSS	Recommended IDSS Range for Optimum P1dB	12 GHz	mA		80-110

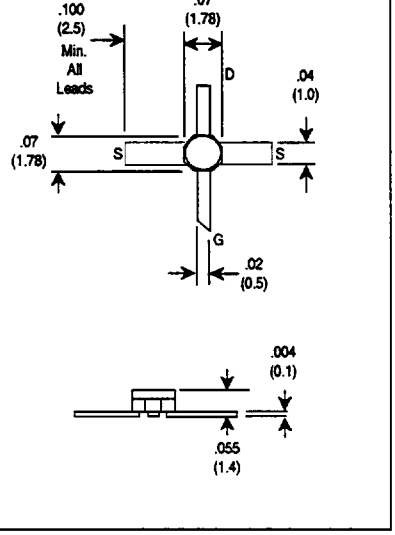
MwT-370
(hermetic)



MwT-371
(hermetic)



MwT-373
(non-hermetic)



Unit: Inches (mm)

DC SPECIFICATIONS AT Ta = 25 °C

* Overall Rth depends on case mounting

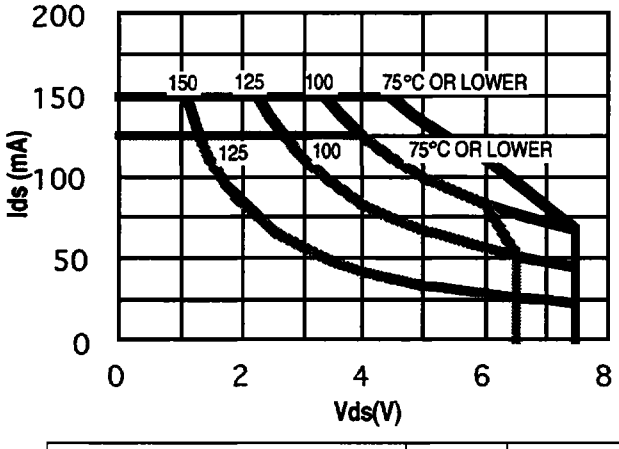
SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Idss	Saturated Drain Current Vds=4.0 V VGS=0.0 V	mA	30		120
Gm	Transconductance Vds=4.0 V VGS=0.0	mS	35	55	
Vp	Pinch-off Voltage Vds=3.0 V IDS=2.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Voltage Igs=-0.2 mA	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd=-0.2 mA	V	-8.0	-12.0	
Rth	Thermal Resistance* MwT-3 Chip, 371 MwT-370, 373	°C/W		150 320*	

MAXIMUM RATINGS AT Ta = 25 ° C

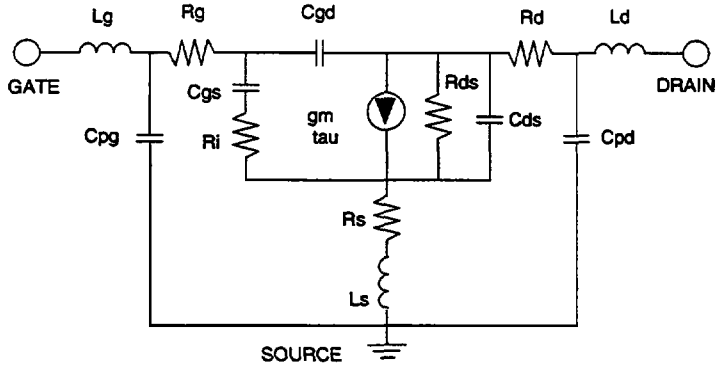
SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	120	180

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

SAFE OPERATING LIMITS vs. Case Temperature — Absolute Maximum — Continuous Maximum



DEVICE EQUIVALENT CIRCUIT MODEL

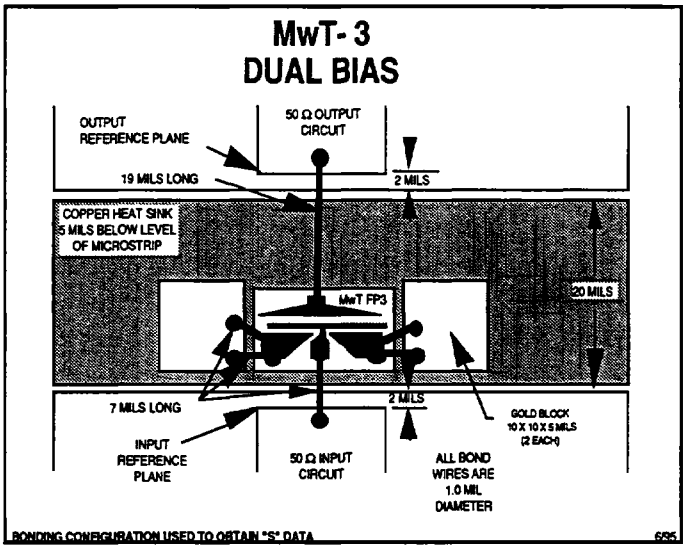


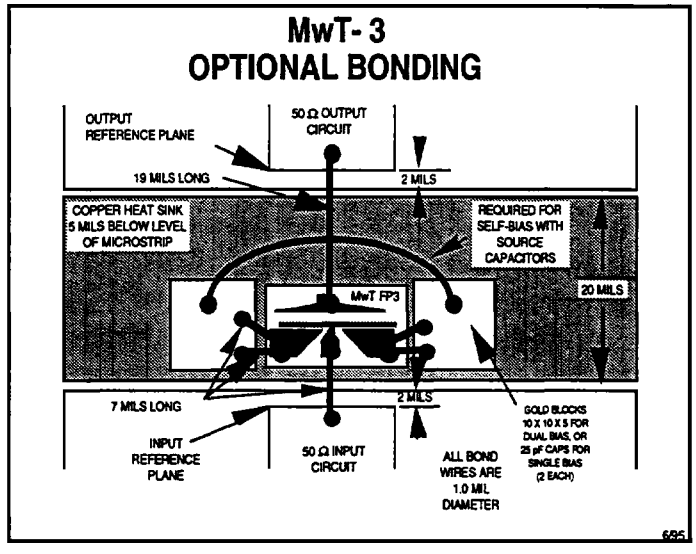
PARAMETER		VALUE	
Gate Bond Wire Inductance	Lg	0.136	nH
Gate Pad Capacitance	Cpg	0.034	pF
Gate Resistance	Rg	0.314	Ω
Gate-Source Capacitance	Cgs	0.348	pF
Channel Resistance	Ri	5.78	Ω
Gate-Drain Capacitance	Cgd	0.022	pF
Transconductance	gm	51.0	mS
Transit time	tau	3.7	psec

PARAMETER		VALUE	
Source Resistance	Rs	1.48	Ω
Source Inductance	Ls	0.034	nH
Drain-Source Resistance	Rds	253.00	Ω
Drain-Source Capacitance	Cds	0.074	pF
Drain Resistance	Rd	3.11	Ω
Drain Pad Capacitance	Cpd	0.012	pF
Drain Inductance	Ld	0.227	nH

RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-3 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.





BIN SELECTION

Every MwT-3 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 18 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS (mA)	30-35	35-40	40-45	45-50	50-55	55-60	60-65	65-70	70-75	75-80	80-85	85-90	90-95	95-100	100-105	105-110	110-115	115-120

BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

DEVICE HANDLING PROCEDURE

1) Open package in clean room environment only.
2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
8) CAUTION: Handling of chips other than as specified above may cause permanent damage.