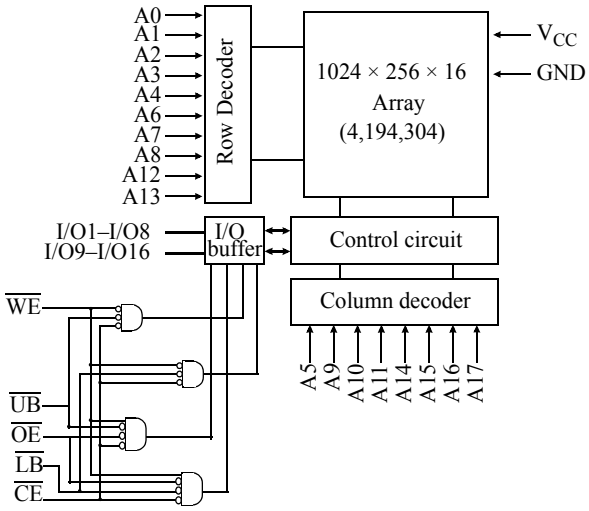
3.3 V 256 K × 16 CMOS SRAM

Features

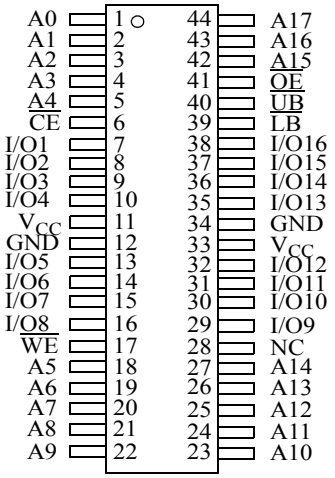
- Pin compatible with AS7C34098
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 4/5/6/7 ns output enable access time
- Low power consumption: ACTIVE
  - 650 mW /max @ 10 ns
- Low power consumption: STANDBY
  - 18 mW /max CMOS
- Individual byte read/write controls
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL- and CMOS-compatible, three-state I/O
- 44-pin JEDEC standard packages
  - 400-mil SOJ
  - TSOP 2
  - 48-ball FBGA 6 x 9 mm
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement for SOJ and TSOP 2

44-pin (400 mil) SOJ
TSOP2



Selection guide

		–10	–12	–15	–20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		4	5	6	7	ns
Maximum operating current	Industrial	180	160	140	110	mA
	Commercial	170	150	130	100	mA
Maximum CMOS standby current		5	5	5	5	mA

Ball arrangement BGA

48-BGA Ball-Grid-Array Package

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{CC}
E	V_{CC}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	$\overline{WE}$	I/O8
H	NC	A8	A9	A10	A11	NC

48-BGA Ball-Grid-Array Package
Version 2 Alternative

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O1	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O9
C	I/O2	I/O3	A5	A6	I/O11	I/O10
D	V_{SS}	I/O4	A17	A7	I/O12	V_{CC}
E	V_{CC}	I/O5	NC	A16	I/O13	V_{SS}
F	I/O7	I/O6	A14	A15	I/O14	I/O15
G	I/O8	NC	A12	A13	$\overline{WE}$	I/O16
H	NC	A8	A9	A10	A11	NC

Functional description

The AS7C34098A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 4/5/6/7 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. The device is guaranteed not to exceed 18mW power consumption in CMOS standby mode. A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O16 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O1–I/O8, and $\overline{UB}$ controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is for 3.3V (AS7C34098A) supply. The device is available in the JEDEC standard 400-mL, 44-pin SOJ, TSOP 2 and also with 48B uBGA package with 6 X 9mm external dimension..

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.50	+5.0	V
Voltage on any pin relative to GND	V_{t2}	–0.50	V_{CC} +0.50	V
Power dissipation	P_D	–	1.5	W
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Ambient temperature with V_{CC} applied	T_{bias}	–55	+125	°C
DC current into outputs (low)	I_{OUT}	–	±20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1–I/O8	I/O9–I/O16	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	X	X	High Z	High Z	Output disable (I_{CC})
L	X	X	H	H			
L	H	L	L	H	D_{OUT}	High Z	Read (I_{CC})
			H	L	High Z	D_{OUT}	
			L	L	D_{OUT}	D_{OUT}	
L	L	X	L	H	D_{IN}	High Z	Write (I_{CC})
			H	L	High Z	D_{IN}	
			L	L	D_{IN}	D_{IN}	

Key: X = Don't care, L = Low, H = High.

Recommended operating conditions

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage		V_{CC} (10/12/15/20)	3.0	3.3	3.6	V
Input voltage		V_{IH}**	2.0	–	V_{CC} + 0.5	V
		V_{IL}*	–0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	°C
	industrial	T_A	–40	–	85	°C

* V_{IL} min = –1.0V for pulse width less than 5ns.
** V_{IH} max = V_{CC} + 2.0V for pulse width less than 5ns.

DC operating characteristics (over the operating range)[1]

Parameter	Symbol	Test conditions		–10		–12		–15		–20		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max V_{IN} = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	V_{CC} = Max $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max Min cycle, 100% duty $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	Industrial	–	180	–	160	–	140	–	110	mA
			Commercial	-	170	-	150	-	130	-	100	mA
Standby power supply current	I_{SB}	V_{CC} = Max $\overline{CE}$ = V_{IH}, f = Max		–	60	–	60	–	60	–	60	mA
	I_{SB1}	V_{CC} = Max $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0		–	5	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V

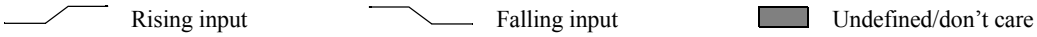
Capacitance (f = 1MHz, T_a = 25° C, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$	V_{IN} = 0V	6	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	8	pF

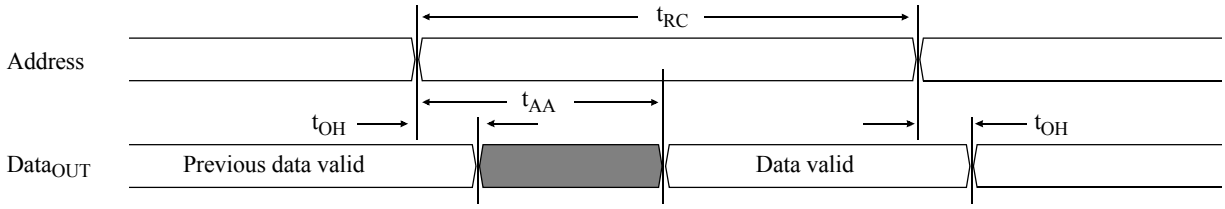
Read cycle (over the operating range)[3,9]

Parameter	Symbol	–10		–12		–15		–20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	
Output enable ($\overline{OE}$) access time	t_{OE}	–	4	–	5	–	6	–	7	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	5	–	6	–	7	–	9	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	5	–	6	–	7	–	9	ns	4, 5
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	–	5	–	6	–	7	–	8	ns	
$\overline{LB}$, $\overline{UB}$ Low to output in low Z	t_{BLZ}	0	–	0	–	0	–	0	–	ns	
$\overline{LB}$, $\overline{UB}$ High to output in high Z	t_{BHZ}	–	5	–	6	–	7	–	9	ns	
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	5

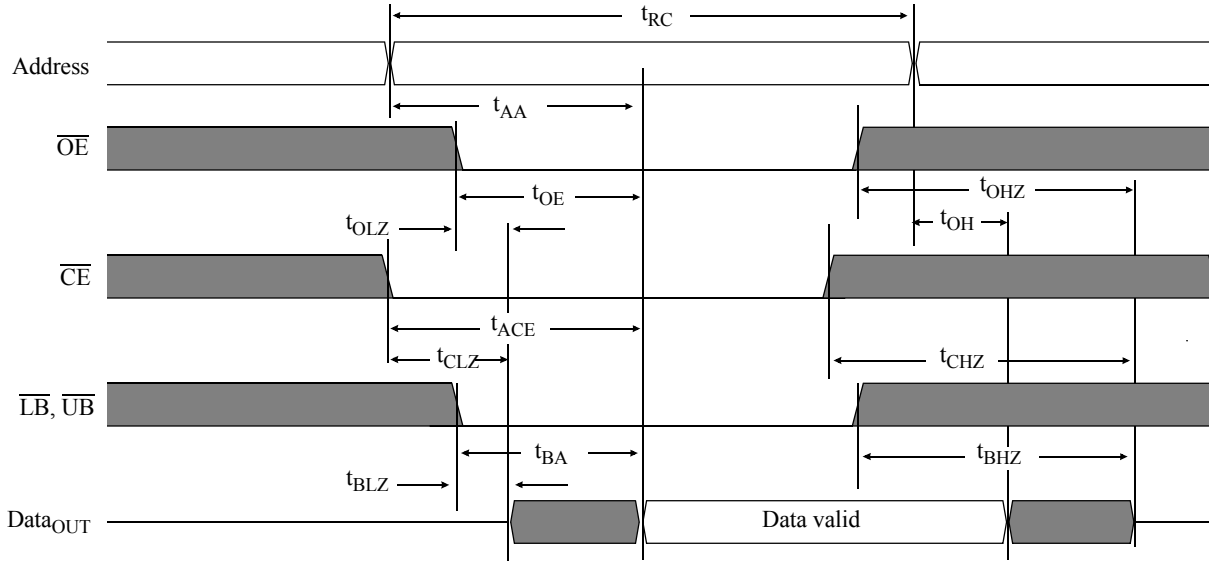
Key to switching waveforms



Read waveform 1 (address controlled)[6,7,9]



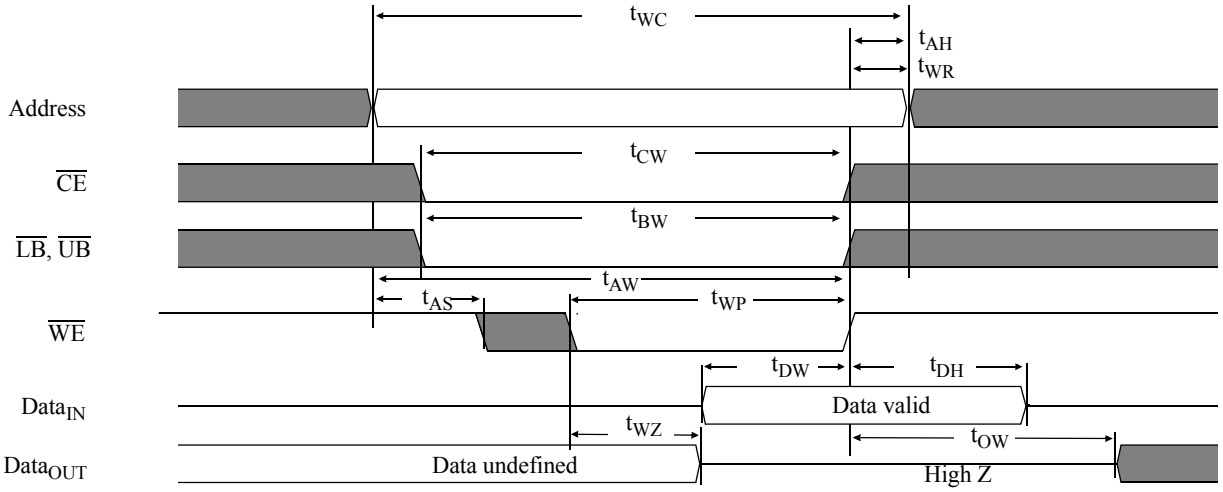
Read waveform 2 ($\overline{CE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)[6,8,9]



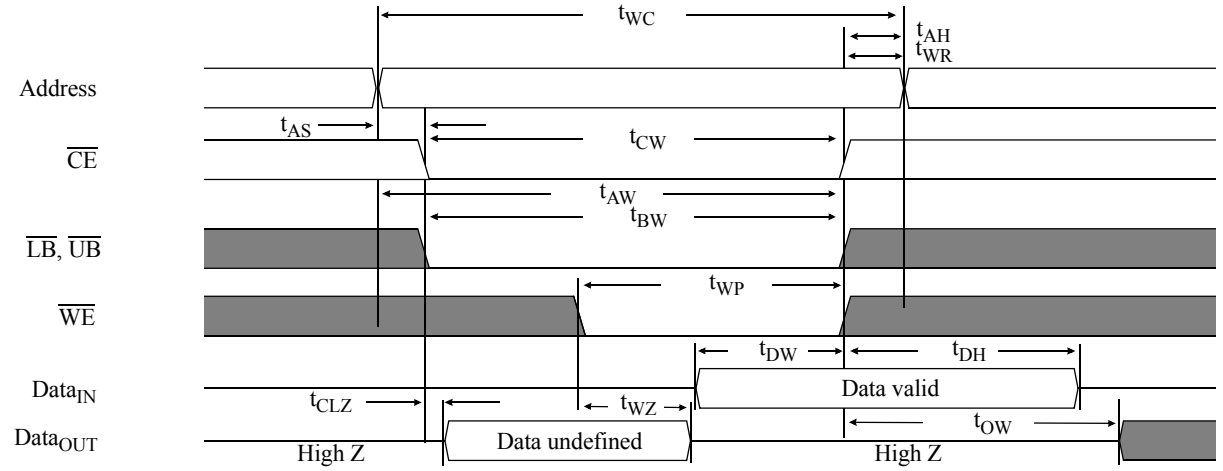
Write cycle (over the operating range)[11]

Parameter	Symbol	–10		–12		–15		–20		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	7	–	8	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	7	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width ($\overline{OE}$ = High)	t_{WP1}	7	–	8	–	10	–	12	–	ns	
Write pulse width ($\overline{OE}$ = Low)	t_{WP2}	10	–	12	–	15	–	20	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6		7	–	9	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High-Z	t_{WZ}	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5
Byte enable Low to write end	t_{BW}	7	–	8	–	10	–	12	–	ns	4, 5

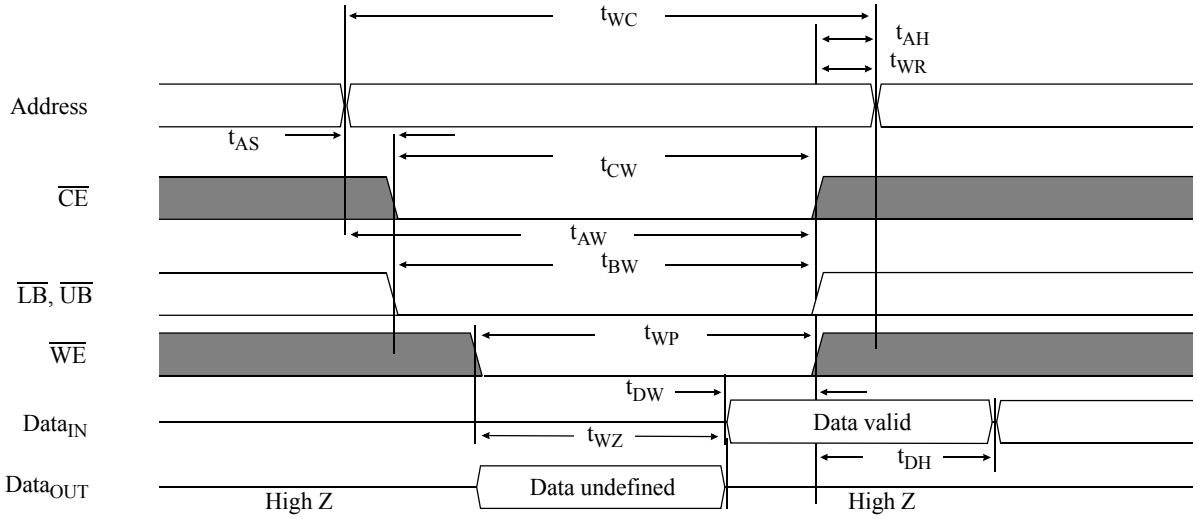
Write waveform 1($\overline{WE}$ controlled)[10,11]



Write waveform 2 ($\overline{CE}$ controlled)[10,11]



Write waveform 3 [10,11]



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

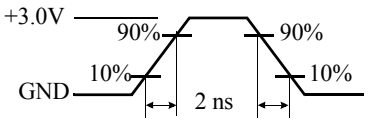
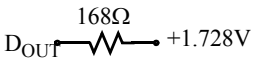


Figure A: Input pulse

Thevenin equivalent:



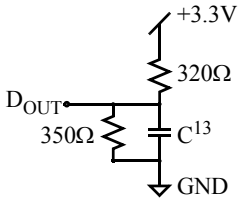
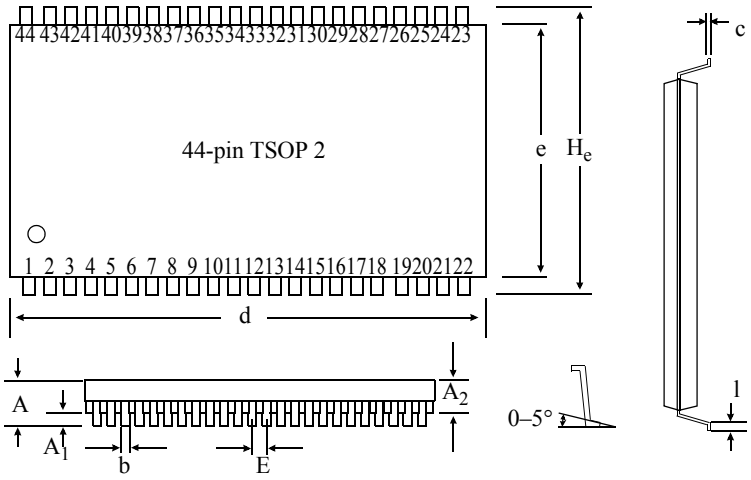


Figure B: 3.3V Output load

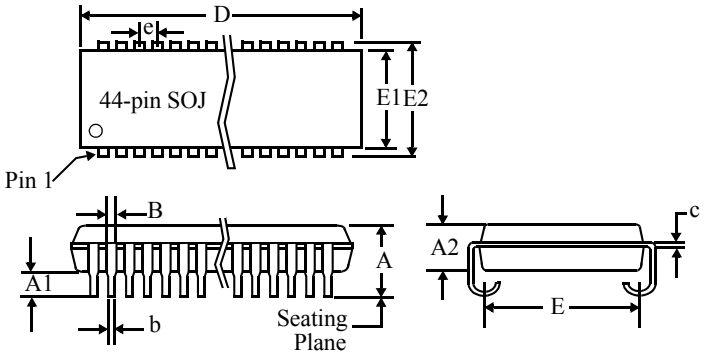
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A and B.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure B. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 N/A
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A
13 C=30pF, except on High Z and Low Z parameters, where C=5pF.

Package dimensions

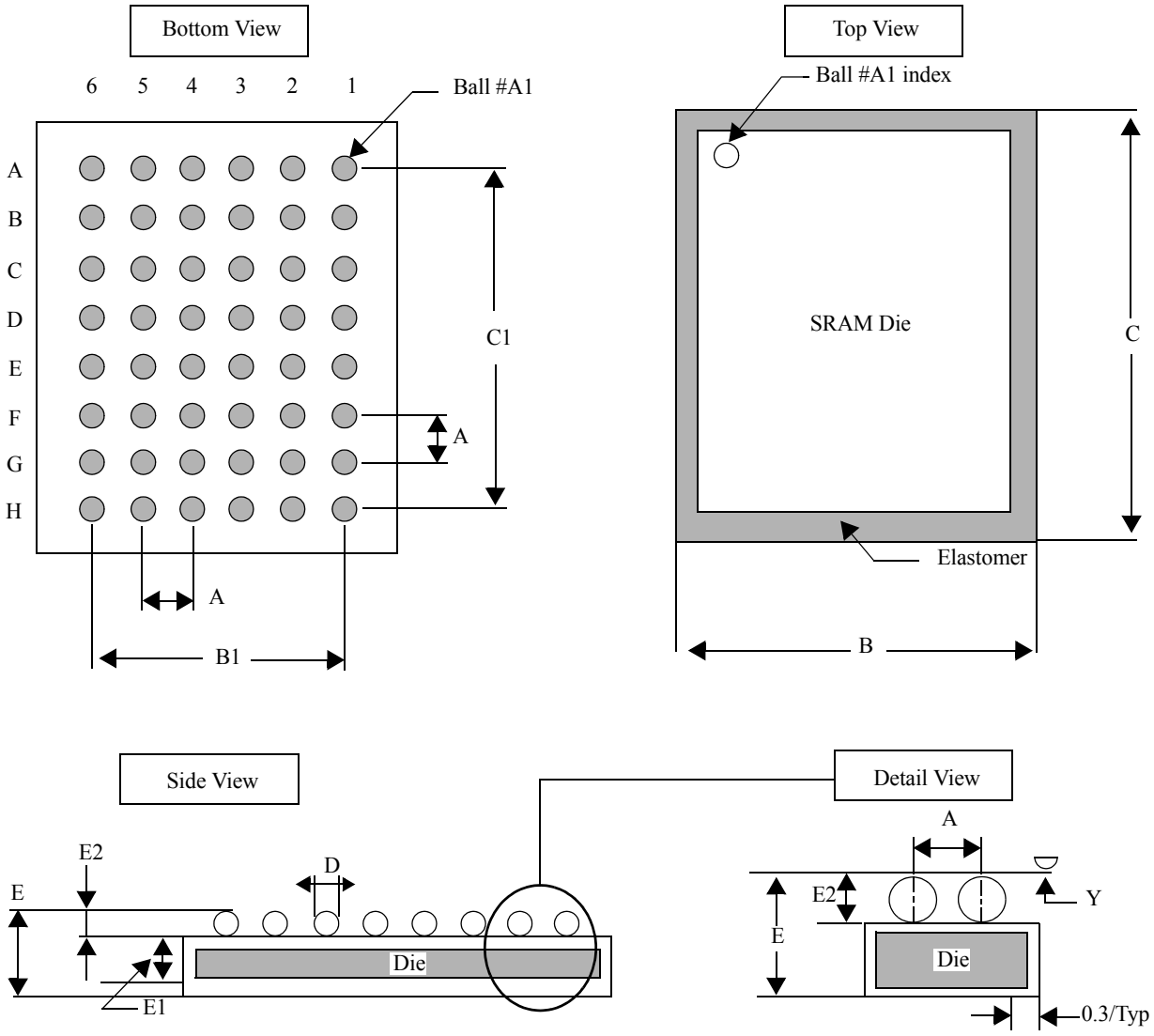


	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A_1	0.05	0.15
A_2	0.95	1.05
b	0.3	0.45
c	0.12	0.21
d	18.31	18.52
e	10.06	10.26
H_e	11.68	11.94
E	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mils	
	Min(mils)	Max(mils)
A	0.128	0.148
A1	0.025	-
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	

48-ball FBGA



	Minimum	Typical	Maximum
A	–	0.75	–
B	5.90	6.00	6.10
B1	–	3.75	–
C	8.90	9.00	9.10
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	–	1.20
E1	–	0.32	–
E2	0.24	0.27	0.3
Y	–	–	0.10

Notes

1. Bump counts: 48 (8 row × 6 column).
2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).
3. Units: millimeters.
4. All tolerance are ±0.050 unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.10 (max).

Ordering Codes

Package	Temperature	10 ns	12 ns	15 ns	20 ns
SOJ	Commercial	AS7C34098A-10JC	AS7C34098A-12JC	AS7C34098A-15JC	AS7C34098A-20JC
	Industrial	AS7C34098A-10JI	AS7C34098A-12JI	AS7C34098A-15JI	AS7C34098A-20JI
TSOP 2	Commercial	AS7C34098A-10TC	AS7C34098A-12TC	AS7C34098A-15TC	AS7C34098A-20TC
	Industrial	AS7C34098A-10TI	AS7C34098A-12TI	AS7C34098A-15TI	AS7C34098A-20TI
BGA	Commercial	AS7C34098A-10BC	AS7C34098A-12BC	AS7C34098A-15BC	AS7C34098A-20BC
	Industrial	AS7C34098A-10BI	AS7C34098A-12BI	AS7C34098A-15BI	AS7C34098A-20BI
BGA Ball Arrange-ment Version 2	Commercial	AS7C34098A-10B2C	AS7C34098A-12B2C	AS7C34098A-15B2C	AS7C34098A-20B2C
	Industrial	AS7C34098A-10B2I	AS7C34098A-12B2I	AS7C34098A-15B2I	AS7C34098A-20B2I

Note: Add suffix 'N' to the above part numbers for Lead Free Parts. (Ex: AS7C34098A - 10TCN)

Part numbering system

AS7C	X	4098A	–XX	J, T, or B	X	X
SRAM prefix	Voltage: 3 - 3.3V CMOS	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2 B: 48-ball FBGA 6 x 9 mm	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, –40°C to 85°C	N = Lead Free Parts

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