209-Bump BGA
Commercial Temp
Industrial Temp

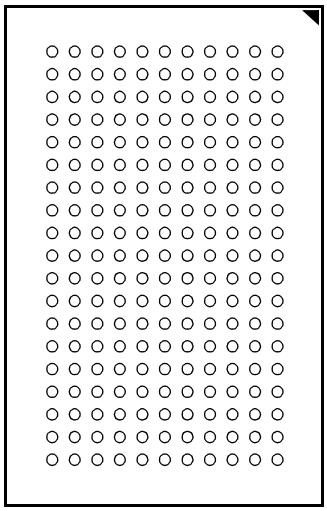
ΣRAM 2M x 9, 1M x 18, 512K x 36 Separate I/O Sigma SDR SRAM

333 MHz
1.8 V V_{DD}
1.8 V and 1.5 V I/

Features

- Observes the Sigma RAM pinout standard
- 1.8 V +150/–100 mV core power supply
- 1.5 V or 1.8 V I/O supply
- Pipelined read operation
- Fully coherent read and write pipelines
- Echo Clock outputs track data output drivers
- ZQ mode pin for user-selectable output drive strength
- 2 user-programmable chip enable inputs for easy depth expansion
- IEEE 1149.1 JTAG-compatible Boundary Scan
- 209-bump, 14 mm x 22 mm, 1 mm bump pitch BGA package
- Pin compatible with future 32M, 64M and 128M devices

		- 333
Pipeline Mode	tKHKH	3.0 ns
	tKHQV	1.5 ns



Bottom View

209-Bump, 14 mm x 22 mm BGA
1 mm Bump Pitch, 11 x 19 Bump Array

Sigma RAM Family Overview

The GS8180S09/18/36B are built in compliance with the Sigma RAM pinout standard for Separate I/O synchronous SRAMs. They are 18,874,368-bit (16Mb) SRAMs. These are the first in a family of wide, very low voltage CMOS I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

GSI's family of Common I/O ΣRAMs are offered in a number of configurations that emulate other synchronous SRAMs, such as Burst RAMs, NBT RAMs, Late Write, or Double Data Rate (DDR) SRAMs. The logical differences between the protocols employed by these RAMs hinge mainly on various combinations of address bursting, output data registering, and write cueing. ΣRAMs allow a user to implement the interface protocol best suited to the task at hand.

Functional Description

Because a Sigma RAM is a synchronous device, address, data Inputs, and read/ write control inputs are captured on the rising edge of the input clock. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

Because the Separate I/O ΣRAM always transfers data in two packets, A0 is internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfer. Since the LSB is tied off internally, the address field of a Separate I/O SDR ΣRAM is always one address pin less than the advertised index depth (e.g., the 1M x 18 has a 512K addressable index).

Single Data Rate (SDR) Separate I/O Sigma RAMs implement a pipelined read and incorporate a rising-edge-triggered output register. For read cycles, a pipelined SRAM's output data is temporarily stored by the edge-triggered output register during the access cycle, and then released to the output drivers at the next rising edge of clock.

GS818x18/36B ΣRAMs are implemented with GSI's high performance CMOS technology and are packaged in a 209-bump BGA.

8180S36 Pinout

512K x 36 Separate I/O—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	Dc1	Dc2	A	E2	A (16M)	MCL	A (8M)	E3	A	Qb1	Qb2
B	Dc3	Dc4	MCL	NC	A	$\overline{W}$	A	MCL	NC	Qb3	Qb4
C	Dc5	Dc6	NC	MCL	NC (128M)	$\overline{E1}$	NC	NC	MCL	Qb5	Qb6
D	Dc7	Dc8	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	Qb7	Qb8
E	Dc9	Qc1	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	Db1	Qb9
F	Qc3	Qc2	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	Db2	Db3
G	Qc5	Qc4	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	Db4	Db5
H	Qc7	Qc6	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	Db6	Db7
J	Qc9	Qc8	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	Db8	Db9
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	Dd9	Dd8	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	Qa8	Qa9
M	Dd7	Dd6	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	Qa6	Qa7
N	Dd5	Dd4	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	Qa4	Qa5
P	Dd3	Dd2	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	Qa2	Qa3
R	Qd9	Dd1	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	Qa1	Da9
T	Qd7	Qd8	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	Da8	Da7
U	Qd5	Qd6	NC	A	NC (64M)	A	NC (32M)	A	NC	Da6	Da5
V	Qd3	Qd4	A (2M)	A	A	A1	A	A	A (4M)	Da4	Da3
W	Qd1	Qd2	TMS	TDI	A	MCL	A	TDO	TCK	Da2	Da1

Rev 10 **11 x 19 Bump BGA—14 x 22 mm2 Body—1 mm Bump Pitch—MS-028vBC**

- Note:
  Users of CMOS I/O Sigma RAMs may wish to connect D4, D8, T4, T8 and K4 to $V_{DDQ}/2$ to allow alternate use of HSTL I/O Sigma RAMs.

8180S18 Pinout

1M x 18 Separate I/O—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	Db1	Db2	A	E2	A (16M)	MCL	A (8M)	E3	A	NC	NC
B	Db3	Db4	MCL	NC	A	$\overline{W}$	A	NC	NC	NC	NC
C	Db5	Db6	NC	NC	NC (128M)	$\overline{E1}$	A	NC	MCL	NC	NC
D	Db7	Db8	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
E	Db9	Qb1	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
F	Qb3	Qb2	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	Qb5	Qb4	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	Qb7	Qb6	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	Qb9	Qb8	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	Qa8	Qa9
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	Qa6	Qa7
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	Qa4	Qa5
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	Qa2	Qa3
R	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	Qa1	Da9
T	NC	NC	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	Da8	Da7
U	NC	NC	NC	A	NC (64M)	A	NC (32M)	A	NC	Da6	Da5
V	NC	NC	A (2M)	A	A	A1	A	A	A (4M)	Da4	Da3
W	NC	NC	TMS	TDI	A	MCL	A	TDO	TCK	Da2	Da1

Rev 10

11 x 19 Bump BGA—14 x 22 mm2 Body—1 mm Bump Pitch—MS-028vBC

- Note:
  Users of CMOS I/O Sigma RAMs may wish to connect D4, D8, T4, T8 and K4 to $V_{DDQ}/2$ to allow alternate use of HSTL I/O Sigma RAMs.

8180S09 Pinout

2M x 9 Separate I/O—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	D1	D2	A	E2	A, NC (16M)	MCL	A, NC (8M)	E3	A	NC	NC
B	D3	D4	NC	NC	A (x36)	$\overline{W}$	A	NC	NC	NC	NC
C	D5	D6	NC	NC	A, NC (128M)	$\overline{E1}$	A (x18)	A (x9)	NC	NC	NC
D	D7	D8	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
E	D9	Q1	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
F	Q3	Q2	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	Q5	Q4	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	Q7	Q6	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	Q9	Q8	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ	$\overline{CQ}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	NC	NC
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	NC	NC
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	NC	NC
R	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
T	NC	NC	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
U	NC	NC	NC	A	NC (64M)	A	NC (32M)	A	NC	NC	NC
V	NC	NC	A (2M)	A	A	A1	A	A	A (4M)	NC	NC
W	NC	NC	TMS	TDI	A	MCL	A	TDO	TCK	NC	NC

Rev 1

11 x 19 Bump BGA—14 x 22 mm2 Body—1 mm Bump Pitch—MS-028vBC

- Note:
  Users of CMOS I/O Sigma RAMs may wish to connect D4, D8, T4, T8 and K4 to $V_{DDQ}/2$ to allow alternate use of HSTL I/O Sigma RAMs.

Pin Description Table

Pin Location	Symbol	Description	Type	Comments
A3, A5, A7, A9, B5, B7, U4, U6, U8, V3, V4, V5, V6, V7, V8, V9, W5, W7	A	Address	Input	(all versions)
C7	A	Address	Input	(x09 and x18 versions)
C5, C8	A	Address	Input	(x09 version only)
K3	CK	Clock	Input	Active High
K1	CQ	Echo Clock	Output	Active High
K11	CQ	Echo Clock	Output	Active High (x18 and x36 versions)
K2	$\overline{CQ}$	Echo Clock	Output	Active Low
K10	$\overline{CQ}$	Echo Clock	Output	Active Low (x18 and x36 versions)
	DQ	Data I/O	Input/Output	—
C6	$\overline{E1}$	Chip Enable	Input	Active Low
A4, A8	E2 & E3	Chip Enable	Input	Programmable Active High or Low
G6, H6	EP2 & EP3	Chip Enable Program Pin	Input	—
	$\overline{G}$	Asynchronous Output Enable	Input	Active Low
W9	TCK	Test Clock	Input	Active High
W4	TDI	Test Data In	Input	—
W8	TDO	Test Data Out	Output	—
W3	TMS	Test Mode Select	Input	—
L6, M6, J6	M2, M3 & M4	Mode Control Pins	Input	—
N6	MCH	Must Connect High	Input	Active High
A6, D6, K6, P6, T6, W6	MCL	Must Connect Low	Input	Active Low (all versions)
B3, C9	MCL	Must Connect Low	Input	Active Low (x18 and x36 versions)
B8, C4	MCL	Must Connect Low	Input	Active Low (x36 version only)

Pin Description Table

Pin Location	Symbol	Description	Type	Comments
B4, B9, C3, D4, D5, D7, D8, K4, K8, K9, T4, T5, T7, T8, U3, U5, U7, U9	NC	No Connect	—	Not connected to die or any other pin (all versions)
A10, A11, B8, B10, B11, C4, C10, C11, D10, D11, E10, E11, F10, F11, G10, G11, H10, H11, J10, J11, L1, L2, M1, M2, N1, N2, P1, P2, R1, R2, T1, T2, U1, U2, V1, V2, W1, W2	NC	No Connect	—	Not connected to die or any other pin (x09 and x18 versions)
C5, C8	NC	No Connect	—	Not connected to die or any other pin (x18 and x36 versions)
B3, C9, K10, K11, L10, L11, M10, M11, N10, N11, P10, P11, R10, R11, T10, T11, U10, U11, V10, V11, W10, W11	NC	No Connect	—	Not connected to die or any other pin (x18 version only)
C7	NC	No Connect	—	Not connected to die or any other pin (x36 version only)
B6	$\overline{W}$	Write	Input	Active Low
E5, E6, E7, G5, G7, J5, J7, L5, L7, N5, N7, R5, R6, R7	V_{DD}	Core Power Supply	Input	1.8 V Nominal
E3, E4, E8, E9, G3, G4, G8, G9, J3, J4, J8, J9, L3, L4, L8, L9, N3, N4, N8, N9, R3, R4, R8, R9	V_{DDQ}	Output Driver Power Supply	Input	1.8 V or 1.5 V Nominal
D3, D9, F3, F4, F5, F7, F8, F9, H3, H4, H5, H7, H8, H9, K5, K7, M3, M4, M5, M7, M8, M9, P3, P4, P5, P7, P8, P9, T3, T9	V_{SS}	Ground	Input	—
F6	ZQ	Output Impedance Control	Input	—

Background

Separate I/O Sigma RAMs have been designed to be closely related to Common I/O Sigma RAMs in pinout and overall architecture. The similarities give Separate I/O Sigma RAMs a cost advantage by allowing users and vendors to reuse supporting infrastructure and design elements. Separate I/O Sigma RAMs come in Single and Double Data Rate configurations. Because they are designed to operate with both the input data pins and the output data pins operating at full speed all the time, Separate I/O Sigma RAMs produce twice the bandwidth of Common I/O SRAMs of the same speed and output bus width.

Sigma RAM Bandwidth at 333 Mhz Clocking

Configuration		x9	x18	x36	x72	Units
Common I/O	SDR	3	6	12	24	Gb/s
Common I/O	DDR	6	12	24	48	Gb/s
Separate I/O	SDR	6	12	24	48	Gb/s
Separate I/O	DDR	12	24	48	96	Gb/s

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the Sigma RAM Separate I/O interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads multiple writes are needed because burst read or write transfers from Separate I/O SRAMs cut the RAM's bandwidth in half. Separate I/O Sigma RAMs offer users the simplest possible control scheme for back-to-back read-write operations.

Although the Separate I/O Sigma RAM family of pinouts has been designed to support Single and Double Data Rate options, not all Sigma RAM implementations will support both protocols. The following timing diagrams provide a quick comparison between the SDR and DDR protocol options available in the context of the Separate Sigma RAM standard. This particular data sheet covers the Single Data Rate (SDR) Separate
I/O Sigma RAM.

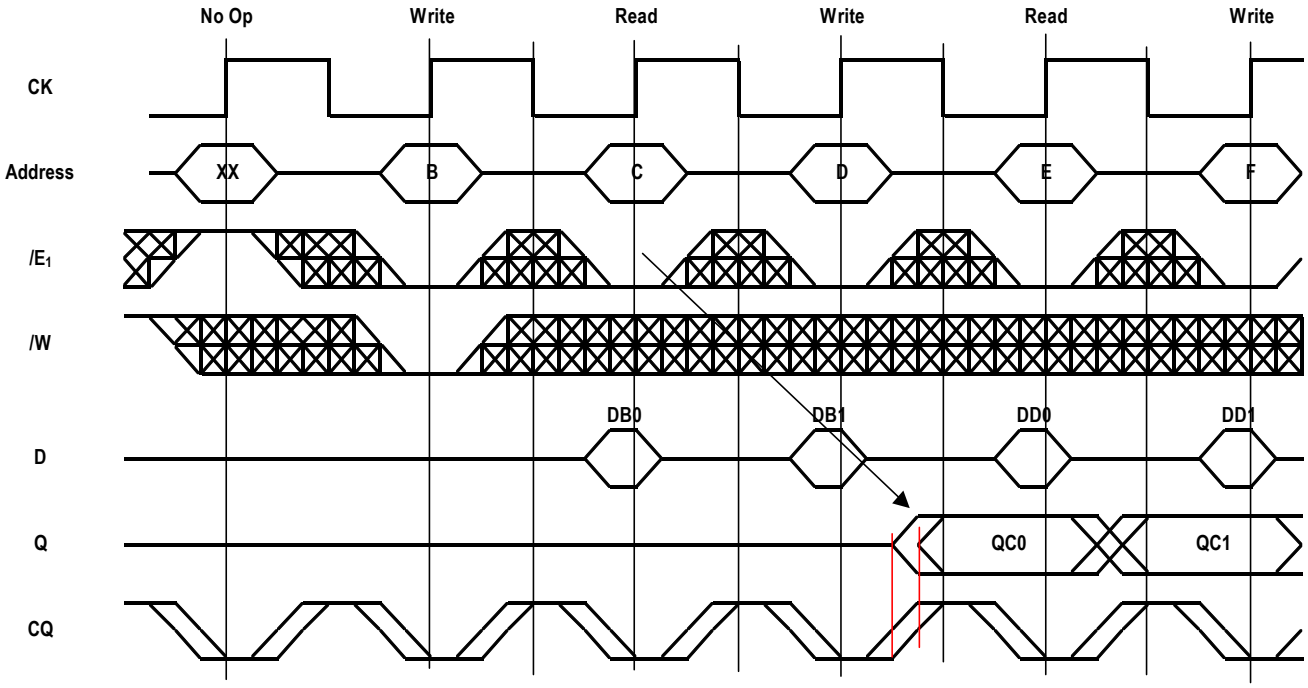
The character of the applications for fast synchronous SRAMs in networking systems are extremely diverse. ΣRAMs have been developed to address the diverse needs of the networking market in a manner that can be supported with a unified development and manufacturing infrastructure. ΣRAMs address each of the bus protocol options commonly found in networking systems.

Mode Selection Truth Table Standard

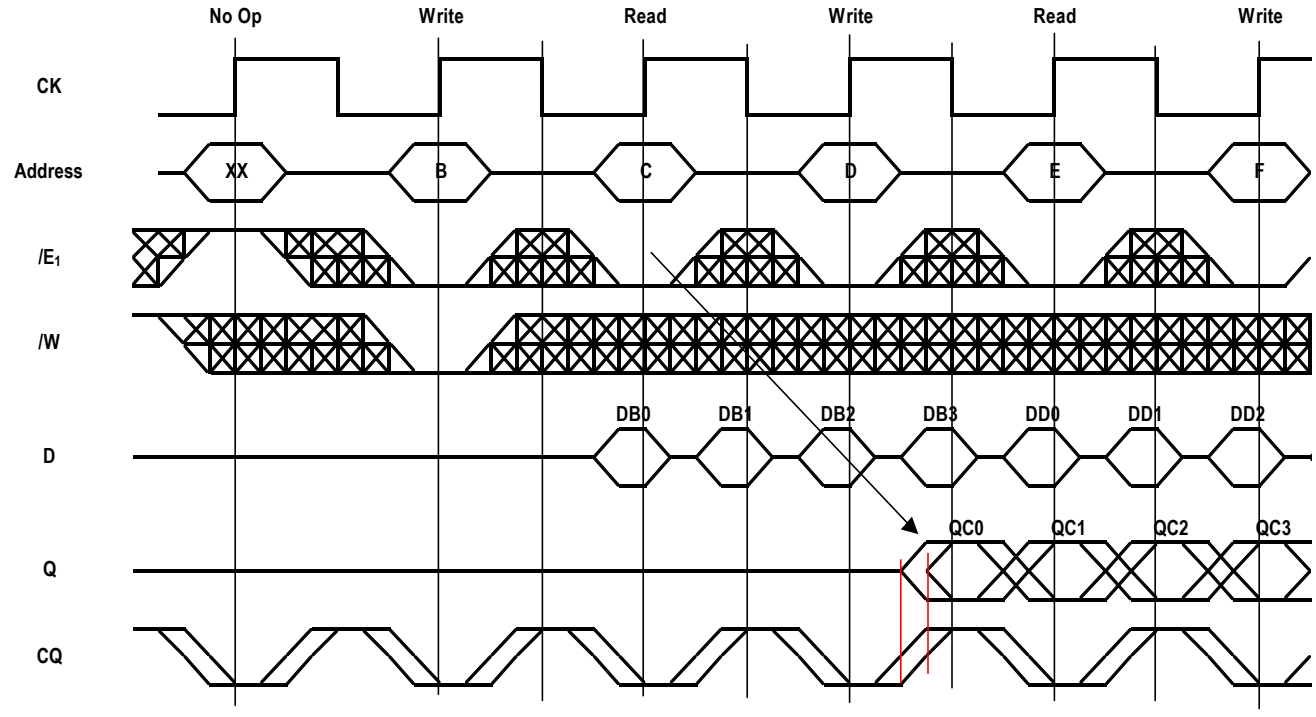
M2	M3	M4	Function	In This Data Sheet?
0	0	0	RFU	n/a
0	0	1	RFU	n/a
0	1	0	RFU	n/a
0	1	1	Double Data Rate	No
1	0	0	RFU	n/a
1	0	1	RFU	n/a
1	1	0	Late Write, Pipelined Read	Yes
1	1	1	RFU	n/a

Separate I/O Sigma RAM Family Mode Comparison—SDR vs. DDR

Single Data Rate



Double Data Rate



Alternating Read-Write Operations

In order to make interface with Separate I/O Sigma RAMs as straightforward as possible, the control logic has been optimized specifically for alternate read-write cycles. A Separate I/O Sigma RAM can begin an alternating sequence of reads and writes with either a read or a write. The status of the $\overline{W}$ pin is evaluated at the beginning of the first active cycle after the RAM has been deselected via $\overline{E1}$. The status of the $\overline{W}$ pin is not checked again until the RAM has been deselected and reselected via $\overline{E1}$. The user may introduce as few or as many deselect cycles between active cycles as are desired, but the user must inform the RAM at the beginning of the first active cycle, via $\overline{W}$, whether to restart with a read or write cycle.

All address, data, and control inputs (with the exception of EP2, EP3, and the mode pins, M2–M4) are synchronized to rising clock edges. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E1}$, E2, and E3). Deassertion of any one of the Enable inputs will deactivate the device. **It should be noted that ONLY deactivation of the RAM via E2 and/or E3 (a Bank Deselect) deactivates the Echo Clocks, CQ1–CQn. Conversely, only E1 is used to identify a "first active cycle" event.**

Read Operations

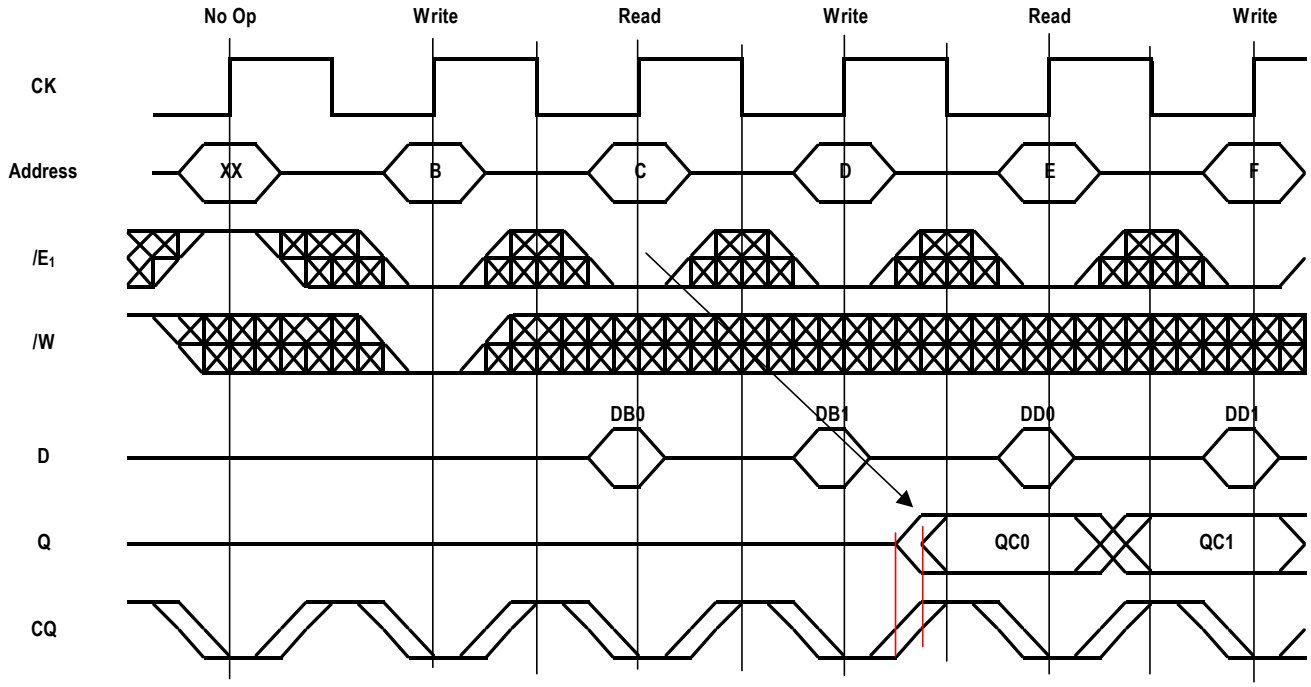
Read operation will be initiated at the rising edge of clock if the previous cycle was a write and all three chip enables ($\overline{E1}$, E2, and E3) are active. If the previous cycle was a deselect ($\overline{E1}$ high), then all three chip enables must be active and the Write enable signal ($\overline{W}$) must be deasserted high. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the Output pins.

Write Operations

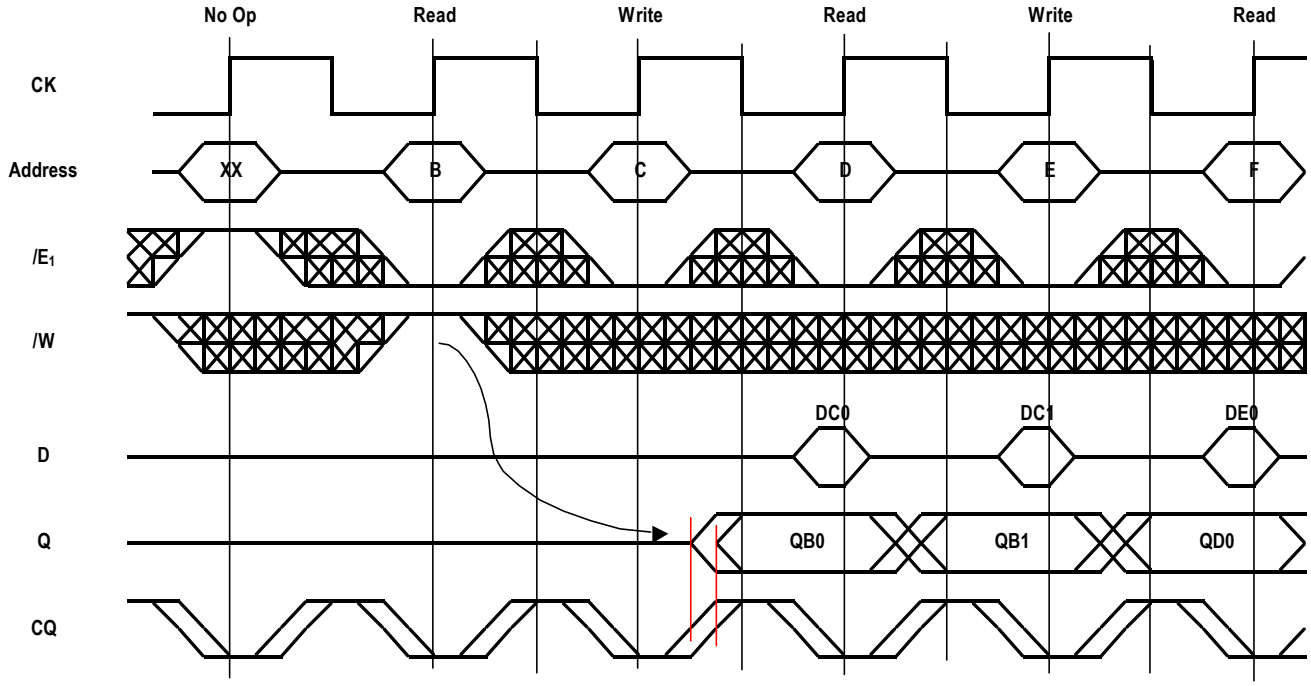
Write operation will be initiated at the rising edge of clock if the previous cycle was a read and all three chip enables ($\overline{E1}$, E2, and E3) are active. If the previous cycle was a deselect ($\overline{E1}$ high), then all three chip enables must be active and the Write enable signal ($\overline{W}$) must be asserted low. Separate I/O Sigma RAMs employ an "Late Write" protocol, meaning the Address input and the Write command are due into the RAM on the same rising edge of clock, but Data In is due into the RAM on the next rising edge of clock.

Separate I/O Sigma RAMs accumulate the input data in a register and then feeds the accumulated data into the array at the first opportunity. Separate I/O Sigma RAMs are fully coherent, which is to say, if the user asks for data just written to the RAM, the most recent copy of the data will be read directly out of the holding registers rather than from the array (which contains stale data).

Single Data Rate Separate I/O Sigma RAM with First Cycle Write



Single Data Rate Separate I/O Sigma RAM with First Cycle Read



Special Functions

Echo Clock

ΣRAMs feature Echo Clocks, CQ1,CQ2, $\overline{CQ1}$, and $\overline{CQ2}$ that track the performance of the output drivers. The Echo Clocks are delayed copies of the main RAM clock, CK. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The Echo Clocks are designed to fire with the rest of the data output drivers. Sigma RAMs provide both in-phase, or true, Echo Clock outputs (CQ1 and CQ2) and inverted Echo Clock outputs ($\overline{CQ1}$ and $\overline{CQ2}$).

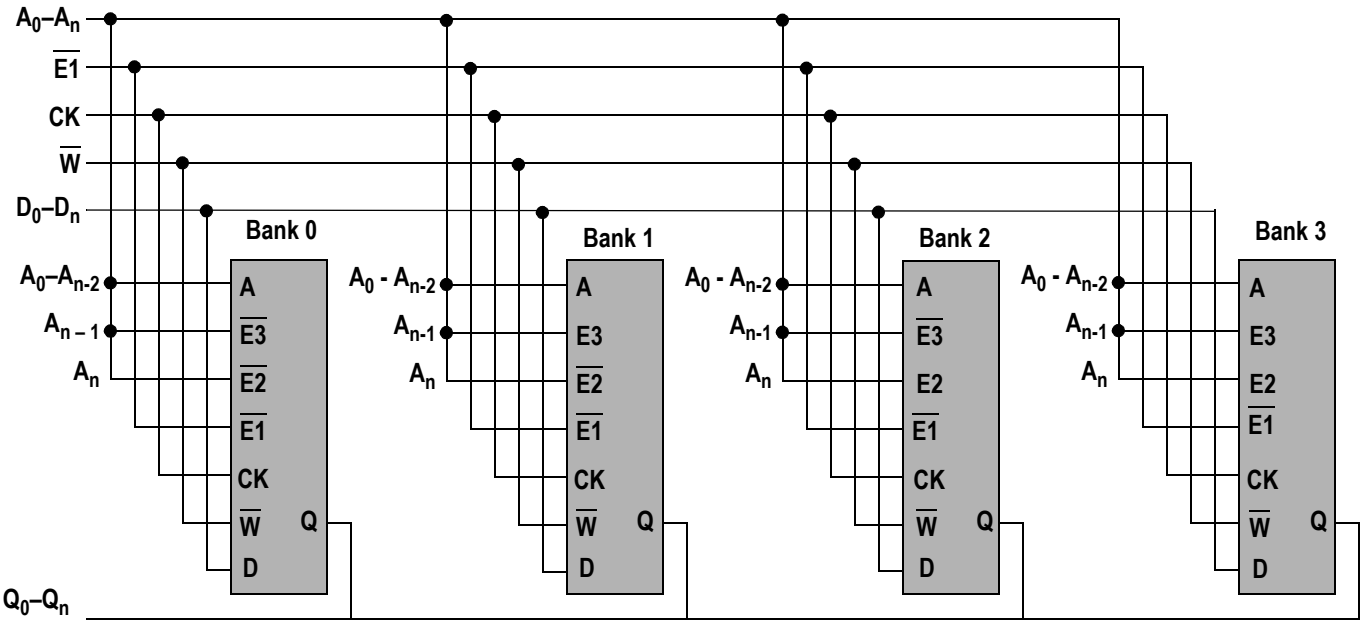
It should be noted that deselection of the RAM via E2 and E3 also deselects the Echo Clock output drivers. Echo Clocks are always active unless deselected by E2 or E3. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. **Deselection of the RAM via E1 does not deactivate the Echo Clocks.**

Programmable Enables

ΣRAMs feature two user-programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and EP3. For example, if EP2 is held at V_{DD}, E2 functions as an active high enable. If EP2 is held to V_{SS}, E2 functions as an active low chip enable input.

Programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four ΣRAMs in binary sequence (00, 01, 10, 11) and driving the enable inputs with two address inputs, four ΣRAMs can be made to look like one larger RAM to the system.

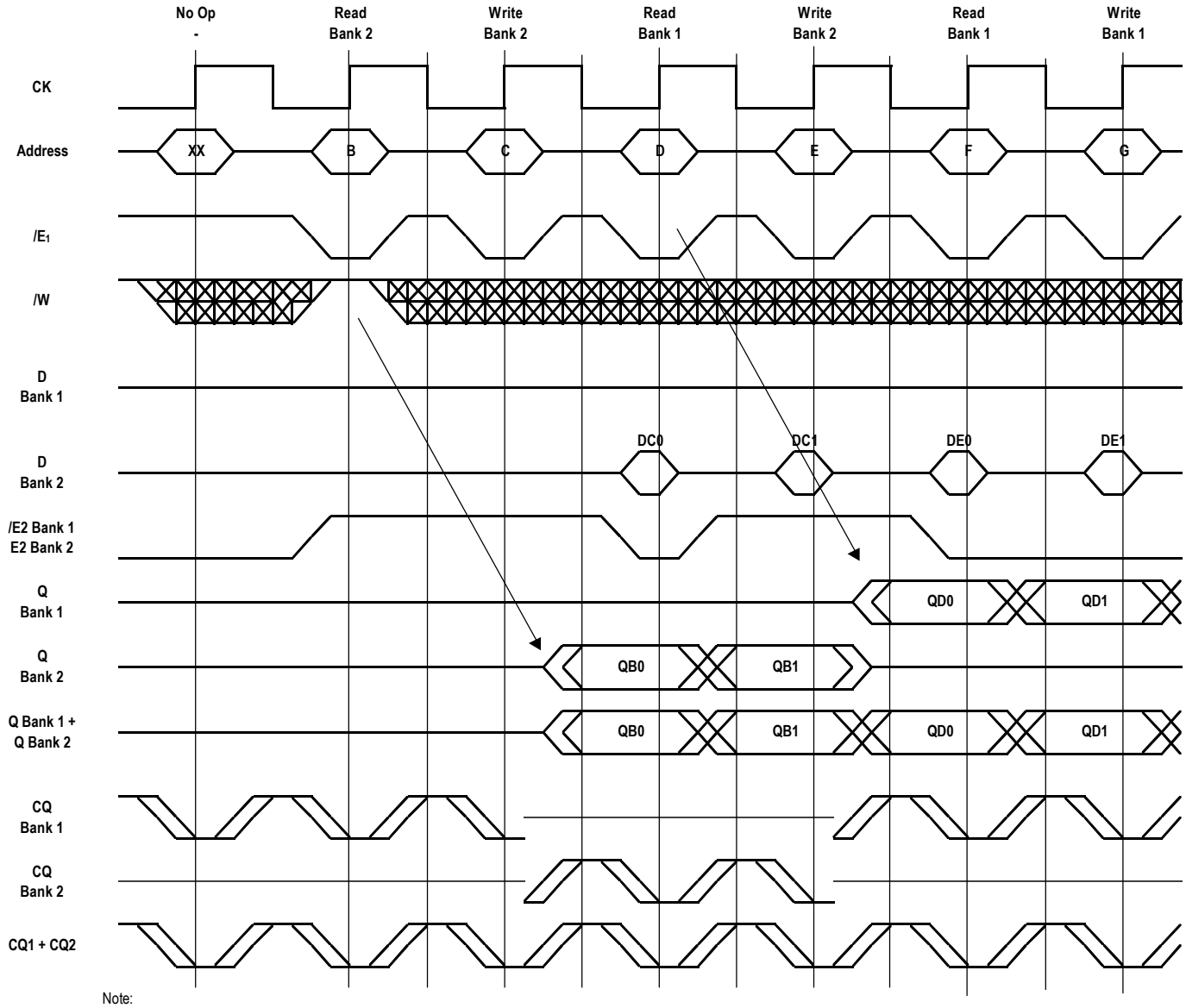
Example Four Bank Depth Expansion Schematic



Bank Enable Truth Table

	EP2	EP3	E2	E3
Bank 0	VSS	VSS	Active Low	Active Low
Bank 1	VSS	VDD	Active Low	Active High
Bank 2	VDD	VSS	Active High	Active Low
Bank 3	VDD	VDD	Active High	Active High

Echo Clock Control in Two Banks of SDR Separate I/O Sigma RAMs

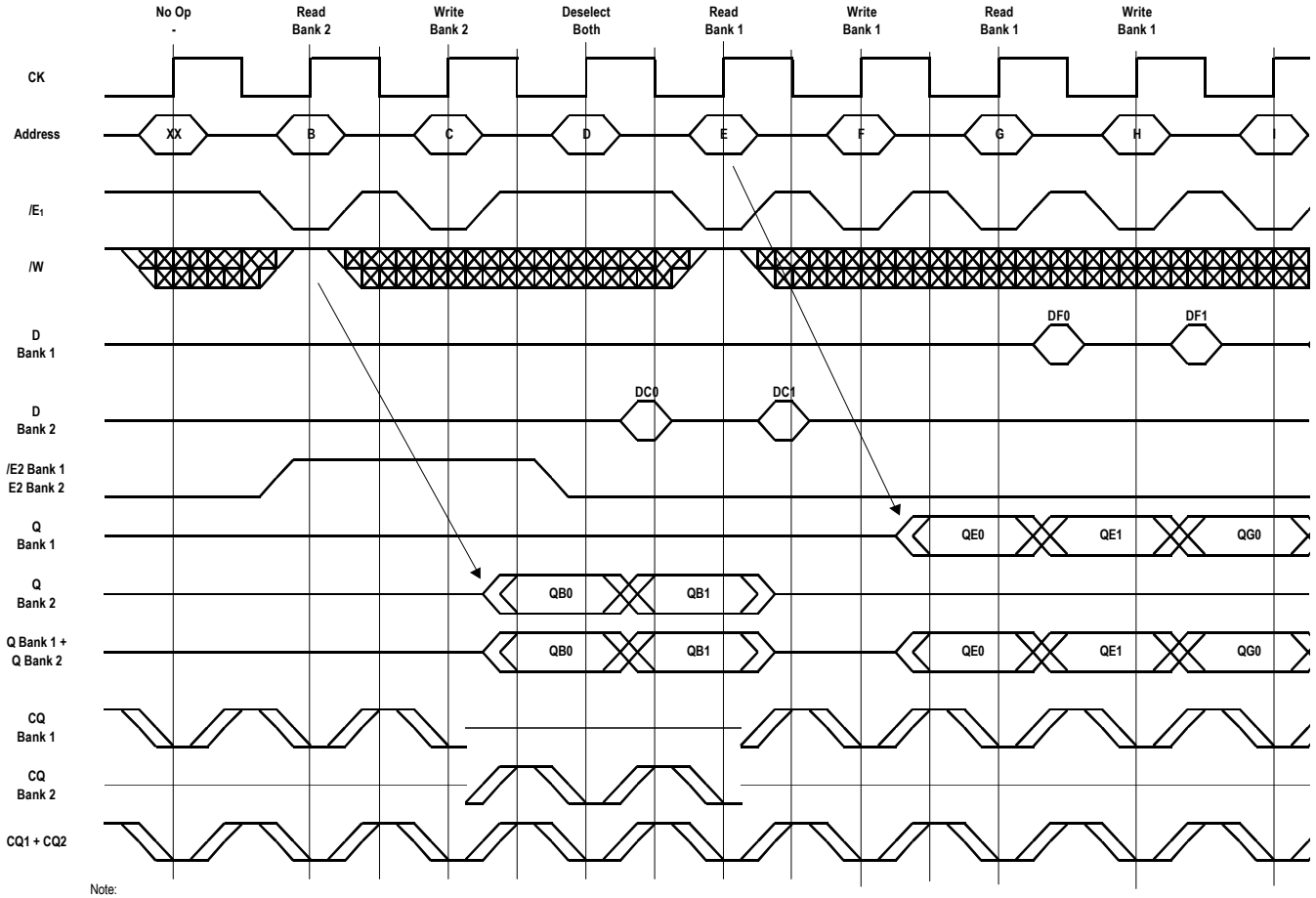


Note:
1 E1\ does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.
2 Reads or Writes launched in a bank continue in the same bank.

It should be noted that deselection of the RAM via E2 and E3 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. Deselection of the RAM via $\overline{E1}$ does not deactivate the Echo Clocks.

In some applications it may be appropriate to pause between banks—to deselect both RAMs with $\overline{E1}$ before resuming read operations. An $\overline{E1}$ deselect at a bank switch will allow at least one clock to be issued from the new bank before the first read cycle in the bank. Although the following drawing illustrates a $\overline{E1}$ read pause upon switching from Bank 1 to Bank 2, a Write to Bank 2 would have the same effect, causing the RAM in Bank 2 to issue at least one clock before it is needed.

.Separate I/O Sigma RAM Bank Switch with $\overline{E1}$ Deselect



Note:
1 E1\ does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.
2 Reads or Writes launched in a bank continue in the same bank.

FLXDrive™ Output Driver Impedance Control

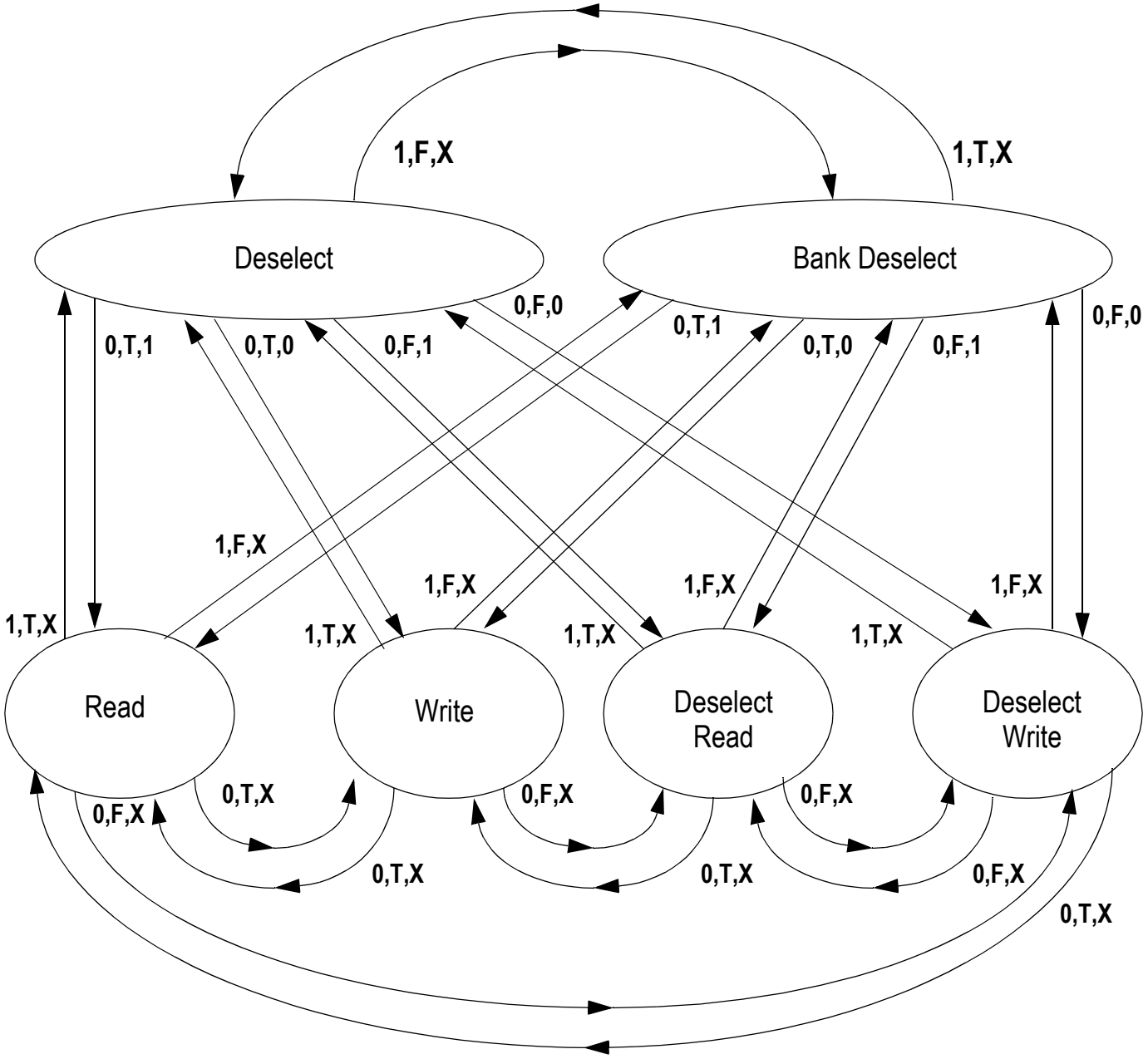
The ZQ pin allows selection between ΣRAM nominal drive strength (ZQ low) for multi-drop bus applications and low drive strength (ZQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Separate I/O SDR Sigma RAM Truth Table

CK	Previous State	Control Inputs			Next State	D (t_{n+1})	D (t_{n+2})	Q (t_{n+1})	Q (t_{n+2})
		$\overline{E1}$	E	$\overline{W}$				CQ (t_{n+1})	CQ (t_{n+2})
↑	Deselect, Bank Deselect, Deselect Read, Deselect Write	1	F	X	Bank Deselect	X	—	Hi-Z	—
↑	Write	1	F	X	Bank Deselect	D1	—	Hi-Z	—
↑	Read	1	F	X	Bank Deselect	X	—	Q1 / CQ1	—
↑	Deselect, Bank Deselect, Deselect Write	1	T	X	Deselect	X	—	Hi-Z / CQ0	—
↑	Deselect Read	1	T	X	Deselect	X	—	Hi-Z	—
↑	Write	1	T	X	Deselect	D1	—	Hi-Z / CQ0	—
↑	Read	1	T	X	Deselect	X	—	Q1 / CQ1	—
↑	Deselect, Bank Deselect	0	F	0	Deselect Write	X	X	Hi-Z	—
↑	Deselect Read	0	F	X	Deselect Write	X	X	Hi-Z	—
↑	Read	0	F	X	Deselect Write	X	X	Q1 / CQ1	—
↑	Deselect, Bank Deselect	0	F	1	Deselect Read	X	—	Hi-Z	Hi-Z
↑	Deselect Write	0	F	X	Deselect Read	X	—	Hi-Z	Hi-Z
↑	Write	0	F	X	Deselect Read	D1	—	Hi-Z	Hi-Z
↑	Deselect, Bank Deselect	0	T	0	Write	D0	D1	Hi-Z / CQ0	—
↑	Deselect Read	0	T	X	Write	D0	D1	Hi-Z	—
↑	Read	0	T	X	Write	D0	D1	Q1 / CQ1	—
↑	Deselect, Bank Deselect	0	T	1	Read	X	—	Q0 / CQ0	Q1 / CQ1
↑	Deselect Write	0	T	X	Read	X	—	Q0 / CQ0	Q1 / CQ1
↑	Write	0	T	X	Read	D1	—	Q0 / CQ0	Q1 / CQ1

Notes:
1. X = Don't Care, H = High, L = Low. E = T (True) if E2 = 1 and $\overline{E3}$ = 0; E = F (False) if E2 = 0 or $\overline{E3}$ = 1.
2. D0 and D1 are the first and second data input transfers in a write.
3. Q0 and Q1 are the first and second data output transfers in a read.
4. CQ0 and CQ1 are the echo clocks associated with the first and second data transfers.
5. "—" indicates that the input needed or driver state is determined by a subsequent operation.

Separate I/O Sigma RAM Control State Diagram



Key: X,X,X = $\overline{E1}$, E, $\overline{W}$ where E = T (True) if E2 = 1 and $\overline{E3}$ = 0; E = F (False) if E2 = 0 or $\overline{E3}$ = 1

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.5	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.5 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.5 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
1.8V I/O Supply Voltage	V_{DDQ}	1.7	1.8	V_{DD}	V	1
1.5V I/O Supply Voltage	V_{DDQ}	1.4	1.5	1.6V	V	1
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

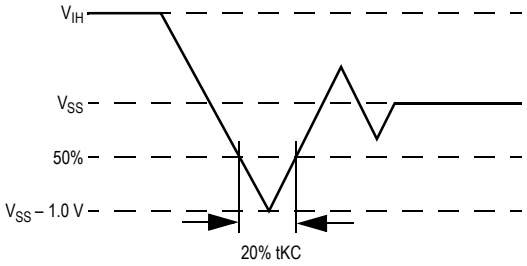
Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 1.4 V ≤ V_{DDQ} ≤ 1.6 V (i.e., 1.5 V I/O) and 1.7 V ≤ V_{DDQ} ≤ 1.95 V (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.
2. The power supplies need to be powered up in the following sequence: V_{DD}, V_{DDQ}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

CMOS I/O DC Input Characteristics

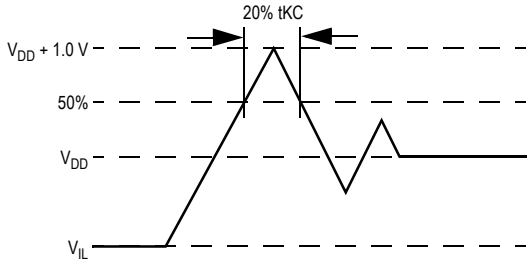
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
CMOS Input High Voltage	V_{IH}	0.65 * V_{DDQ}	—	V_{DD}+ 0.3	V	2
CMOS Input Low Voltage	V_{IL}	–0.3	—	0.35 * V_{DDQ}	V	2

Note: For devices supplied with CMOS input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF

Note: This parameter is sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	TBD	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	TBD	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	TBD	°C/W	3

Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87.
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.

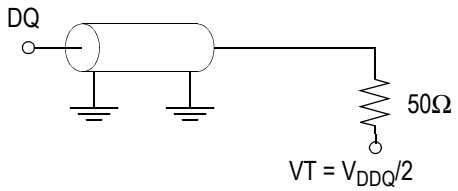
AC Test Conditions

Parameter	Conditions
Input high level	V_{DDQ}
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

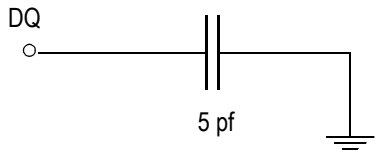
Notes:
1. Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagrams

AC Test Load A



AC Test Load B



Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA	
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ $V_{IN} \leq V_{IL}$	–100 uA –2 uA	2 uA 2 uA	
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA	

Selectable Impedance CMOS Output Driver DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Low Drive Output High Voltage	V_{OHL}	I_{OHL} = –4 mA	V_{DDQ} – 0.4 V		1
Low Drive Output Low Voltage	V_{OLL}	I_{OLL} = 4 mA	—	0.4 V	1
High Drive Output High Voltage	V_{OHH}	I_{OHH} = –8 mA	V_{DDQ} – 0.4 V		2
High Drive Output Low Voltage	V_{OLH}	I_{OLH} = 8 mA	—	0.4 V	2

Operating Currents

Parameter	Test Conditions	Symbol	-333		-300		-275		-250		Units
			0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	
Operating Current	$\overline{E1} \le V_{IL}$ Max. tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$	I_{DDP} Pipeline	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Bank Deselect Current	E2 or E3 False tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$	I_{SB1} Pipeline	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Chip Disable Current	$\overline{E1} \ge V_{IH}$ Min. tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$	I_{SB2} Pipeline	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
CMOS Deselect Current	Device Deselected All inputs V_{SS} + 0.10 V $\ge V_{IN} \ge$ V_{DD} – 0.10 V	I_{DD3} Pipeline	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA

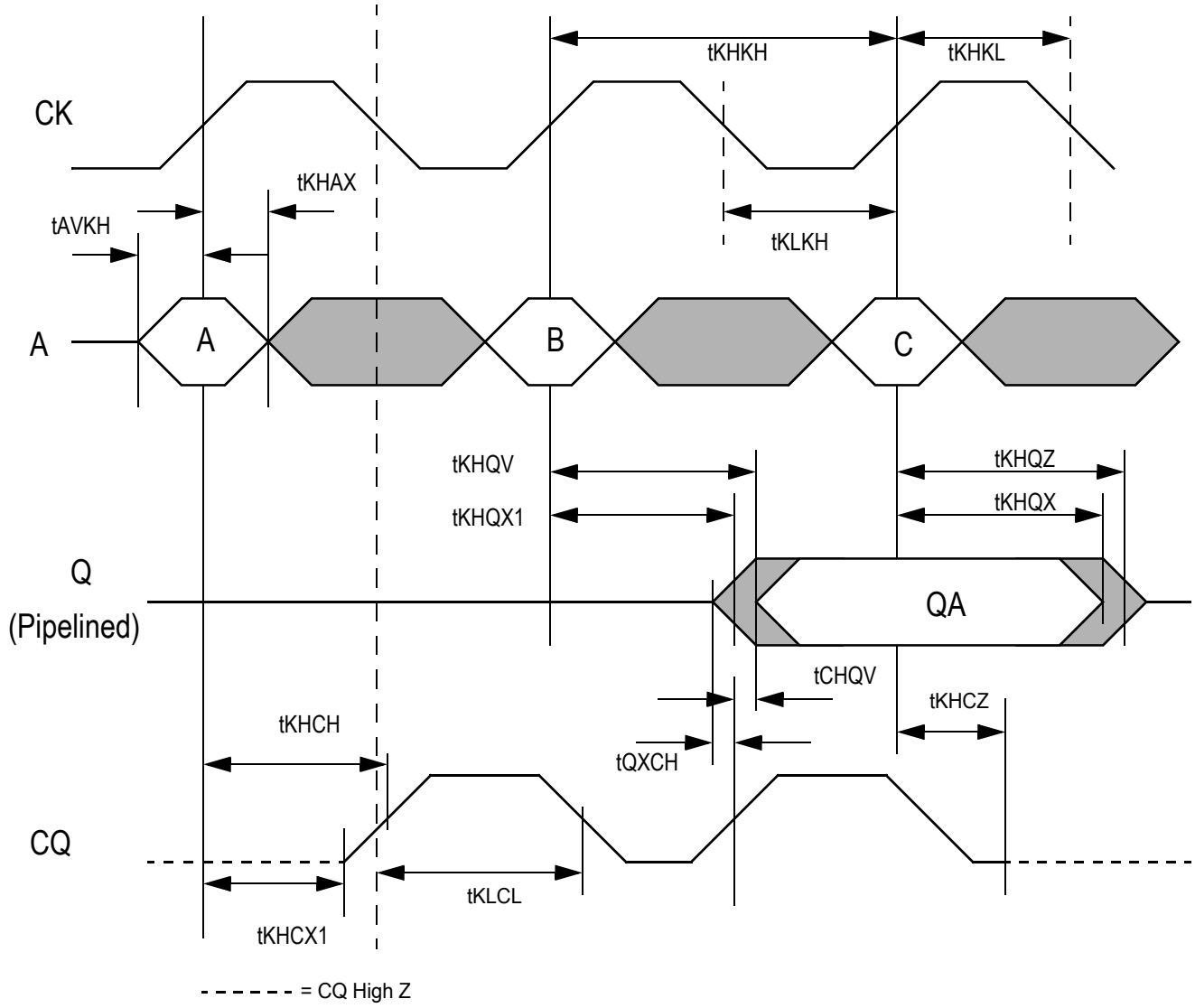
Note: Power measured with outputs disconnected.

AC Electrical Characteristics

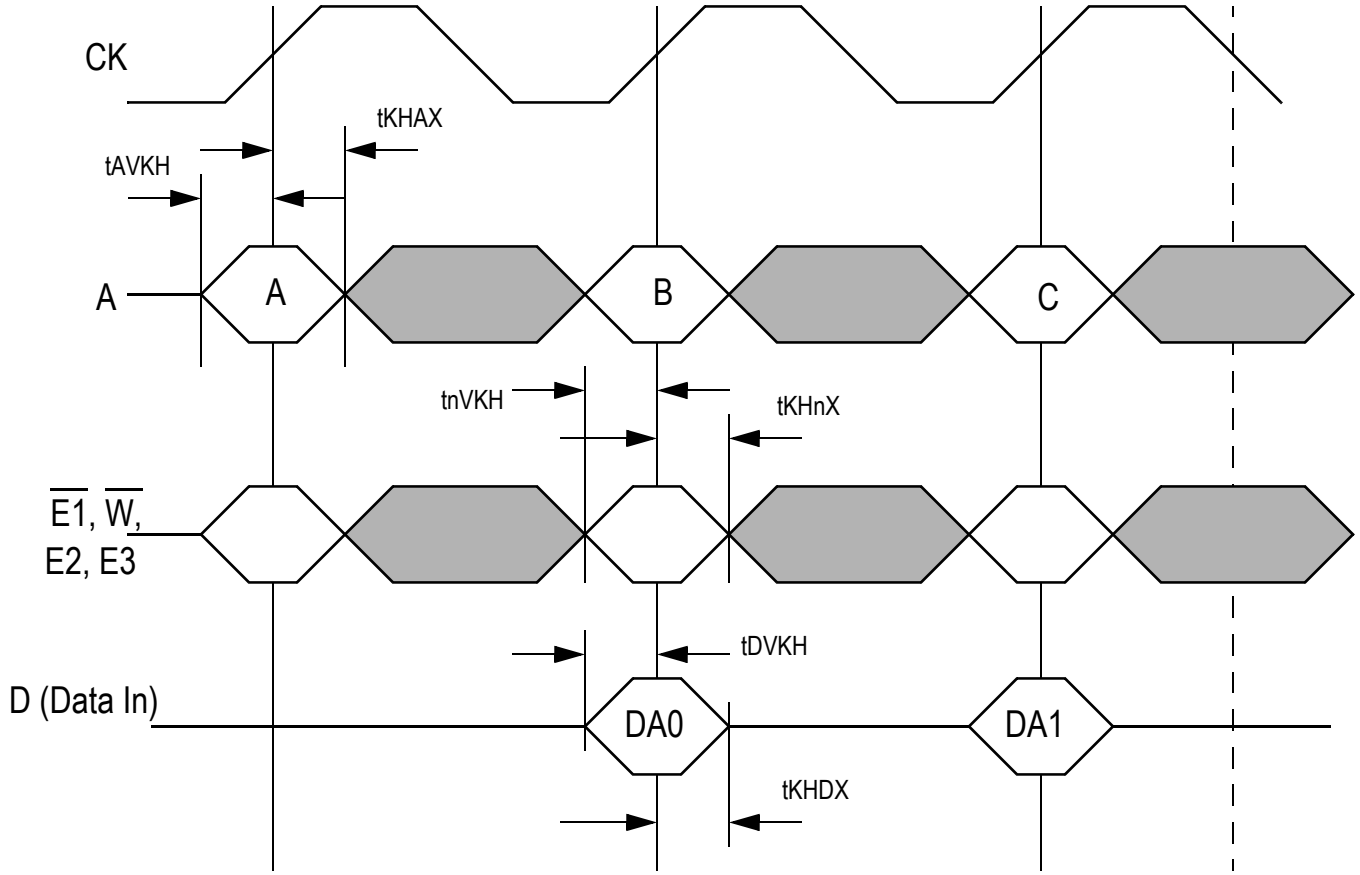
Parameter	Symbol	-333		-300		-275		-250		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	3.0	—	3.3	—	3.6	—	4.0	—	ns	—
Clock High to Output Valid	tKHQV	—	1.6	—	1.8	—	1.9	—	2.1	ns	—
Clock High to Output in High-Z	tKHQZ	0.5	1.6	0.5	1.8	0.5	1.9	0.5	2.1	ns	1
Clock High to Output Invalid	tKHQX	0.5	—	0.5	—	0.5	—	0.5	—	ns	—
Clock High to Output in Low-Z	tKHQX1	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Echo Clock Low-Z	tKHCX1	0.5	—	0.5	—	0.5	—	0.5	—	ns	2, 4
Clock High to Echo Clock High	tKHCH	0.6	1.5	0.6	1.7	0.6	1.8	0.6	2.0	ns	4
Clock Low to Echo Clock Low	tKLCL	0.6	1.7	0.6	1.8	0.6	2.0	0.6	2.2	ns	4
Output Invalid to Echo Clock High	tCHQX	—	–0.5	—	–0.6	—	–0.6	—	–0.7	ns	2
Echo Clock High to Output Valid	tCHQV	—	0.5	—	0.6	—	0.6	—	0.7	ns	2
Clock High to Echo Clock High-Z	tKHCZ	0.5	1.5	0.5	1.7	0.5	1.8	0.5	2.0	ns	1, 2
Clock HIGH Time	tKHKL	1.2	—	1.3	—	1.4	—	1.6	—	ns	—
Clock LOW Time	tKLKH	1.2	—	1.3	—	1.4	—	1.6	—	ns	—
Address Valid to Clock High	tAVKH	0.6	—	0.7	—	0.7	—	0.8	—	ns	—
Clock High to Address Don't Care	tKHAX	0.4	—	0.4	—	0.5	—	0.5	—	ns	—
Enable Valid to Clock High	tEVKH	0.6	—	0.7	—	0.7	—	0.8	—	ns	—
Clock High to Enable Don't Care	tKHEX	0.4	—	0.4	—	0.5	—	0.5	—	ns	—
Write Valid to Clock High	tWVKH	0.6	—	0.7	—	0.7	—	0.8	—	ns	—
Clock High to Write Don't Care	tKHWX	0.4	—	0.4	—	0.5	—	0.5	—	ns	—
Data In Valid to Clock High	tDVKH	0.6	—	0.7	—	0.7	—	0.8	—	ns	—
Clock High to Data In Don't Care	tKHDX	0.4	—	0.4	—	0.5	—	0.5	—	ns	—

Notes:
1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.
3. For any specific temperature and voltage tKHCZ < tKHCX1.
4. Tested using AC Test Load B

Timing Parameter Key - Read Cycle Timing



Timing Parameter Key - Control and Data In Timing



Note: tnVKH = tEVKH, tWVKH, etc. and tKHnX = tKHEX, tKHWX, etc.

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Unlike JTAG implementations that have been common among SRAM vendors for the last several years, this implementation does offer a form of EXTEST, known as Clock Assisted EXTEST, reducing or eliminating the “hand coding” that has been required to overcome the test program compiler errors caused by previous non-compliant implementations.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to V_{DD}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as TAP registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

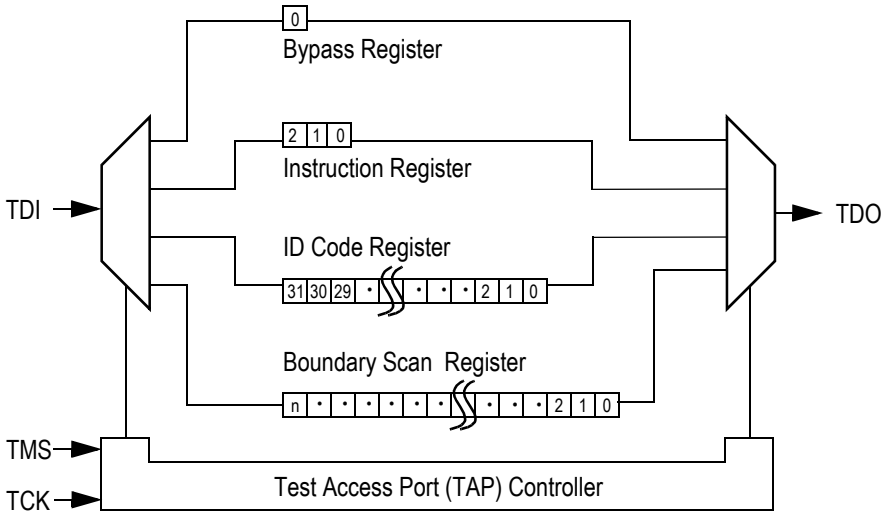
Bypass Register

The Bypass Register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die **Revision Code**				Not Used												I/O Configuration				**GSI Technology JEDEC Vendor ID Code**										Presence Register
Bit #	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1
x09	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

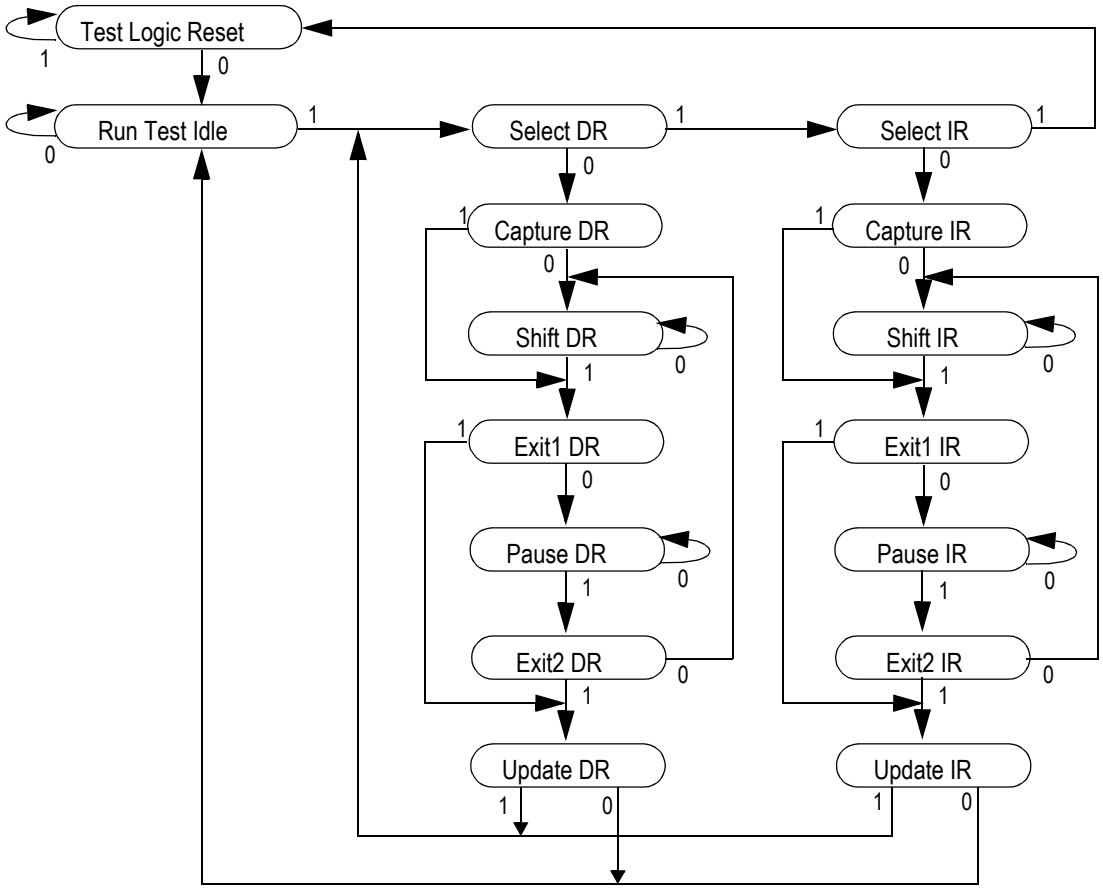
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990—the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1-compliant because some of the mandatory instructions are uniquely implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers.This device will not perform INTEST or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state, the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register, the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the Boundary Scan Register between

the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the Instruction Register has the same effect as the Pause-DR command. This functionality is not Standard 1149.1-compliant.

EXTEST (EXTEST-A)

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. The EXTEST implementation in this device does not, without further user intervention, actually move the contents of the scan chain onto the RAM's output pins. Therefore this device is not strictly 1149.1-compliant. Nevertheless, this RAM's TAP does respond to an all 0s instruction, EXTEST (000), by overriding the RAM's control inputs and activating the Data I/O output drivers. The RAM's main clock (CK) may then be used to transfer Boundary Scan Register contents associated with each I/O from the scan register to the RAM's output drivers and onto the I/O pins. A single CK transition is sufficient to transfer the data, but more transitions will do no harm.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are reserved for future use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST-A	000	Places the Boundary Scan Register between TDI and TDO. This RAM implements an Clock Assisted EXTEST function. *Not 1149.1 Compliant *	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. This RAM does not implement 1149.1 PRELOAD function. *Not 1149.1 Compliant *	1
GSI	101	GSI Private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in Test-Logic-Reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

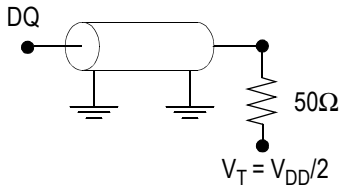
Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	V_{IHT}	0.65 * V_{DD}	V_{DD}+0.3	V	1
Test Port Input Low Voltage	V_{ILT}	–0.3	0.35 * V_{DD}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INTH}	–100	2	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INTL}	–2	2	uA	3
TDO Output Leakage Current	I_{OLT}	–2	2	uA	4
Test Port Output High Voltage	V_{OHT}	V_{DDQ} – 100 mV	—	V	5, 6
Test Port Output Low Voltage	V_{OLT}	—	100 mV	V	7

Notes:
1. Input Under/overshoot voltage must be –1 V < Vi < V_{DD} + 1 V with a pulse width not to exceed 20% tTKC.
2. $V_{DD} \geq V_{IN} \geq V_{IL}$
3. $0\ V \leq V_{IN} \leq V_{IL}$
4. Output Disable, V_{OUT} = 0 to V_{DD}
5. The TDO output driver is served by the V_{DD} supply.
6. I_{OH} = –100 uA
7. I_{OL} = +100 uA

JTAG Port AC Test Conditions

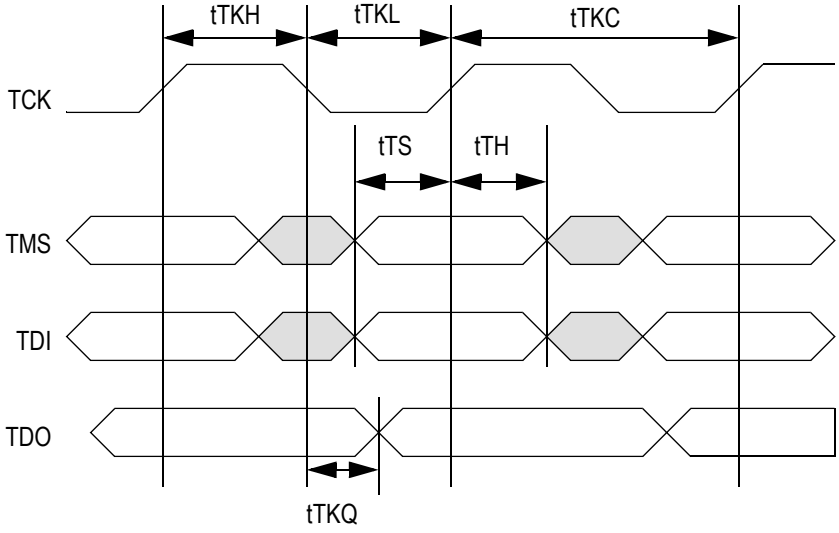
Parameter	Conditions
Input high level	V_{DD} – 200 mV
Input low level	200 mV
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DD}/2

JTAG Port AC Test Load



Notes:
1. Include scope and jig capacitance.
2. Test conditions as as shown unless otherwise noted.

JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

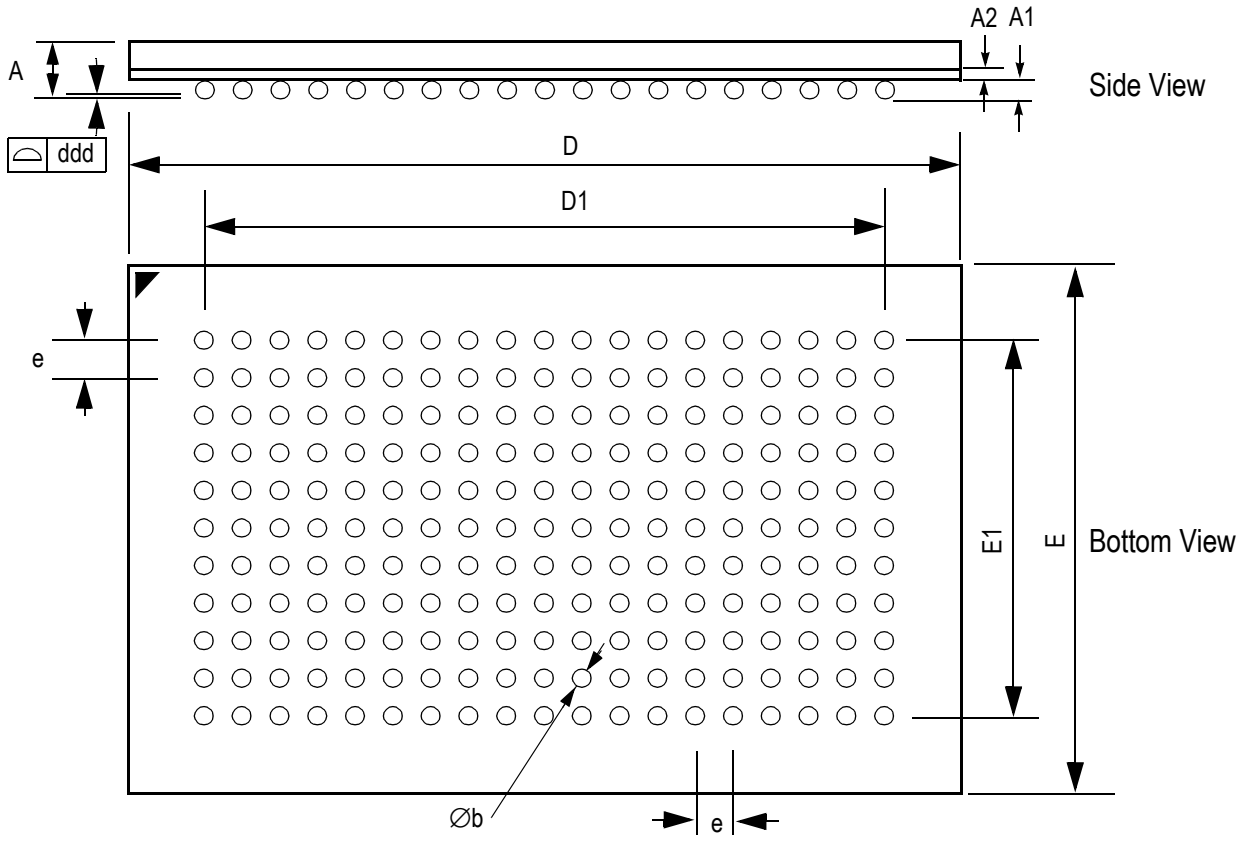
Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	20	—	ns
TCK Low to TDO Valid	tTKQ	—	10	ns
TCK High Pulse Width	tTKH	10	—	ns
TCK Low Pulse Width	tTKL	10	—	ns
TDI & TMS Set Up Time	tTS	5	—	ns
TDI & TMS Hold Time	tTH	5	—	ns

Output Driver Characteristics

TBD

Package Dimensions—209-Bump BGA

14 mm x 22 mm Body, 1.0 mm Bump Pitch, 11 x 19 Bump Array



Symbol	Min.	Typ.	Max.	Units
A	—	—	1.7	mm
A1	0.40	0.50	0.60	mm
A2	0.31	0.36	0.38	mm
b	0.50	0.60	0.70	mm
D	21.9	22.0	22.1	mm
D1	—	18.0 (BSC)	—	mm
E	13.9	14.0	14.1	mm
E1	—	10.0 (BSC)	—	mm
e	—	1.00 (BSC)	—	mm
ddd	—	0.15	—	mm

Rev 1.2

Ordering Information—GSI Sigma RAM

Org	Part Number[1]	Type	Package	Speed (MHz)	T_A[3]
512Kx 36	GS8180**S**36B-333	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	C
512Kx 36	GS8180**S**36B-300	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	C
512Kx 36	GS8180**S**36B-275	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	275	C
512Kx 36	GS8180**S**36B-250	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	C
512Kx 36	GS8180**S**36B-333I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	I
512Kx 36	GS8180**S**36B-300I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	I
512Kx 36	GS8180**S**36B-275I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	275	I
512Kx 36	GS8180**S**36B-250I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	I
1M x 18	GS8180**S**18B-333	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	C
1M x 18	GS8180**S**18B-300	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	C
1M x 18	GS8180**S**18B-275	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	275	C
1M x 18	GS8180**S**18B-250	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	C
1M x 18	GS8180**S**18B-333I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	I
1M x 18	GS8180**S**18B-300I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	I
1M x 18	GS8180**S**18B-275I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	275	I
1M x 18	GS8180**S**18B-250I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	I
2Mx 9	GS8180**S**09B-333	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	C
2Mx 9	GS8180**S**09B-300	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	C
2Mx 9	GS8180**S**09B-275	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	275	C
2Mx 9	GS8180**S**09B-250	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	C
2Mx 9	GS8180**S**09B-333I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	I
2Mx 9	GS8180**S**09B-300I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	I
2Mx 9	GS8180**S**09B-275I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	275	I
2Mx 9	GS8180**S**09B-250I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	I

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS818x36B-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Revisions
8180S091836_r1; 8180S091836_r1_01	Format	• Updated format to comply with Technical Publications standards • ID register contents updated on page 24

