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LTR	DESCRIPTION	DATE	APPROVED

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Defense Electronics Supply Center Dayton, Ohio	PREPARED BY Ray Monnin	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY DA DiCenzo	
Original date of drawing: 9 November 1987	APPROVED BY Robert P. Evans	TITLE: MICROCIRCUITS, 8-BIT MICRO-PROCESSOR CPU, NMOS, MONOLITHIC SILICON
	SIZE A / CODE IDENT. NO. 67268	DWG NO. 5962-87685
AMSC N/A	REV	PAGE 1 OF 22

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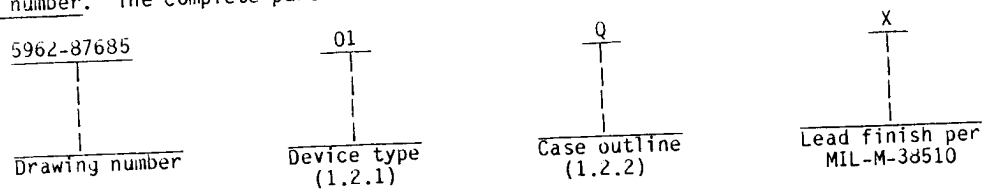
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8088	8-bit microprocessor CPU

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead 9/16" x 2 1/16") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-1 V dc to +7 V dc
Input voltage range	-1 V dc to +7 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation P_D	2.5 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc ±10%
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum high level input voltage (V_{IH})	V_{CC} + 0.5 V dc
Minimum low level input voltage (V_{IL})	-0.5 V dc
Maximum low level input voltage (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level input voltage	V_{IL}		1, 2, 3		0.8	V
High level input voltage	V_{IH}		1, 2, 3	2.0		V
High level output voltage	V_{OH}	$I_{OH} = -400\ \mu A$ $V_{CC} = 4.5\ V$	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	$I_{OL} = 2.0\ mA$ $V_{CC} = 4.5\ V$	1, 2, 3		0.45	V
Power supply current	I_{CC}	$T_C = +25°C$ $V_{CC} = 5.5\ V$ (The I_{CC} is measured while running a functional pattern with specified value I_{OL}/I_{OH} loads applied.)	1, 2, 3		340	mA
Input leakage current	I_{LI}	$V_{CC} = 5.5\ V$ $V_{IN} = 5.5\ V$ and $0\ V$	1, 2, 3	-10	10	µA
Output leakage current	I_{LO}	$V_{CC} = 5.5\ V$ $V_{OUT} = 5.5\ V$ and $0.45\ V$	1, 2, 3	-10	10	µA
Clock input high voltage	V_{CH}	$V_{CC} = 4.5\ V$ and $5.5\ V$	1, 2, 3	3.9		V
Clock input low voltage	V_{CL}	$V_{CC} = 4.5\ V$ and $5.5\ V$	1, 2, 3		0.6	V
Capacitance of input buffer (All input except AD_0-AD_7, RQ/GT)	C_{IN}	$F_C = 1$ MHz See 4.3.1c	4		20	pF
Capacitance of I/O buffer (AD_0-AD_7, RQ/GT)	C_{IO}	$F_C = 1$ MHz See 4.3.1c	4		20	pF
Functional testing		See 4.3.1.d	7, 8			
Clock cycle period 2/	t_{CLCL}	(See figures 3 and 4) 1/	9,10,11	200	500	ns
Clock low time	t_{CLCH}		9,10,11	118		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Clock high time	t_{CHCL}	(See figures 3 and 4) 1/	9,10,11	69		ns
Data in setup time	t_{DVCL}		9,10,11	30		ns
Data in hold time	t_{CLDX}		9,10,11	10		ns
READY setup time into 8088	t_{RYHCH}		9,10,11	118		ns
READY hold time into 8088	t_{CHRYX}		9,10,11	30		ns
READY inactive to CLK	t_{RYLCL}		9,10,11	-8		ns
HOLD setup time	t_{HVCH}		9,10,11	35		ns
INTR, NMI, TEST setup time	t_{INVCH}		9,10,11	30		ns
RQ/GT setup time	t_{GVCH}		9,10,11	30		ns
RQ hold time into 8086	t_{CHGX}		9,10,11	40		ns
READY active to status passive	t_{RYHSH}		9,10,11		110	ns
Status active delay	t_{CHSV}		9,10,11	10	110	ns
Status inactive delay 3/ 4/	t_{CLSH}		9,10,11	10	130	ns
Address valid delay	t_{CLAV}		9,10,11	10	110	ns
Address hold time 3/ 4/	t_{CLAX}		9,10,11	10		ns
Address float delay 4/	t_{CLAZ}		9,10,11	10	80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

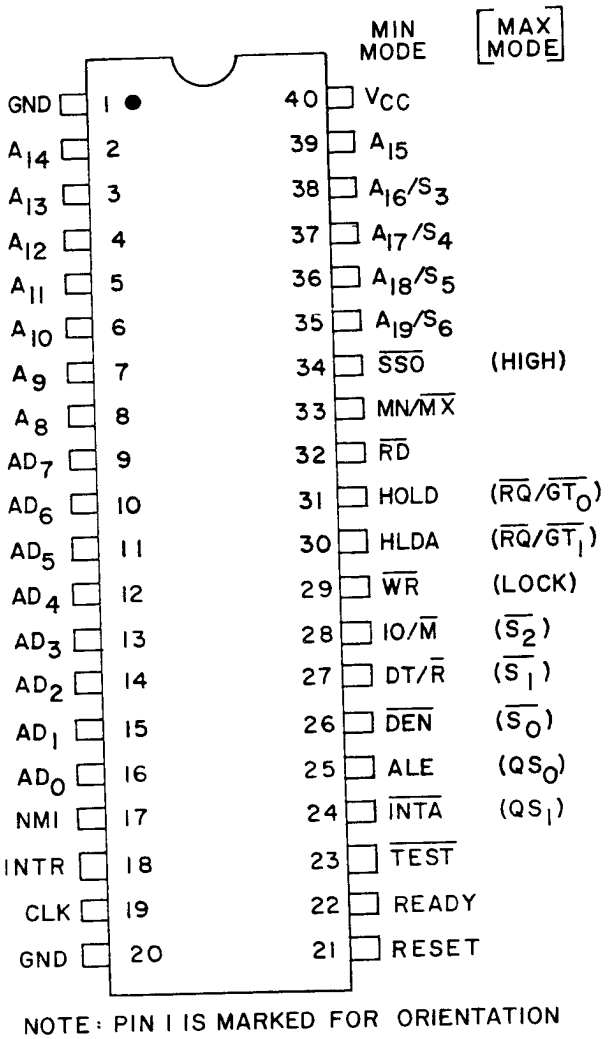
Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
ALE width 5/	t_{LHLL}	(See figures 3 and 4) 1/	9,10,11	98		ns
ALE active delay 4/	t_{CLLH}		9,10,11		80	ns
ALE inactive delay 4/	t_{CHLL}		9,10,11		85	ns
Address hold time to ALE inactive 3/	t_{LLAX}		9,10,11	59		ns
Data valid delay 4/	t_{CLDV}		9,10,11	10	110	ns
Data hold time 5/	t_{CHDX}		9,10,11	10		ns
Data hold time after $\overline{WR}$ 5/	t_{WHDX}		9,10,11	88		ns
Control active delay 1 4/	t_{CVCTV}		9,10,11	10	110	ns
Control active delay 2 4/	t_{CHCTV}		9,10,11	10	110	ns
Control inactive delay 4/	t_{CVCTX}		9,10,11	10	110	ns
Address float to READ active 6/	t_{AZRL}		9,10,11	0		ns
$\overline{RD}$ active delay 4/	t_{CLRL}		9,10,11	10	165	ns
$\overline{RD}$ inactive delay 4/	t_{CLRH}		9,10,11	10	150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{RD}$ inactive to next address active 5/	t_{RHAV}	(See figures 3 and 4) 1/	9,10,11	155		ns
HLDA valid delay 4/	t_{CLHAV}		9,10,11	10	160	ns
GT active delay 4/	t_{CLGL}		9,10,11		110	ns
GT inactive delay 4/	t_{CLGH}		9,10,11		85	ns
$\overline{WR}$ width 5/	t_{WLWH}		9,10,11	340		ns
Address valid to ALE low 6/	t_{AVAL}		9,10,11	58		ns
$\overline{RD}$ width 5/	t_{RLRH}		9,10,11	325		ns
Output rise time	t_{OLOH}	From 0.8 to 2.0 V 1/ 6/	9,10,11		20	ns
Output fall time	t_{OHOL}	From 2.0 to 0.8 V 1/ 6/	9,10,11		12	ns

1/ Test conditions for all ac timings are as follows:
V_{CC} = 4.5 V, 5.5 V
V_{IL} = 0.45 V, V_{IH} = 2.4 V
V_{ILC} = 0.25 V, V_{IHC} = 4.3 V
V_{OL} = 1.4 V, V_{OH} = 1.6 V
Figure 3 and 4
2/ Test conditions for t_{CLCL} maximum are:
V_{CC} = 4.5 V
V_{IL} = 0 V
V_{IH} = 4 V
V_{IHC} = 5 V
V_{ILC} = 0 V
V_{OL} = 1 V
3/ Minimum specification tested at V_{CC} maximum (5.5 V) only.
4/ Maximum specification tested at V_{CC} minimum (4.5 V) only.
5/ Tested at V_{CC} maximum (5.5 V) only.
6/ Tested at V_{CC} minimum (4.5 V) only.



NOTE: PIN 1 IS MARKED FOR ORIENTATION

FIGURE 1. Terminal connections.

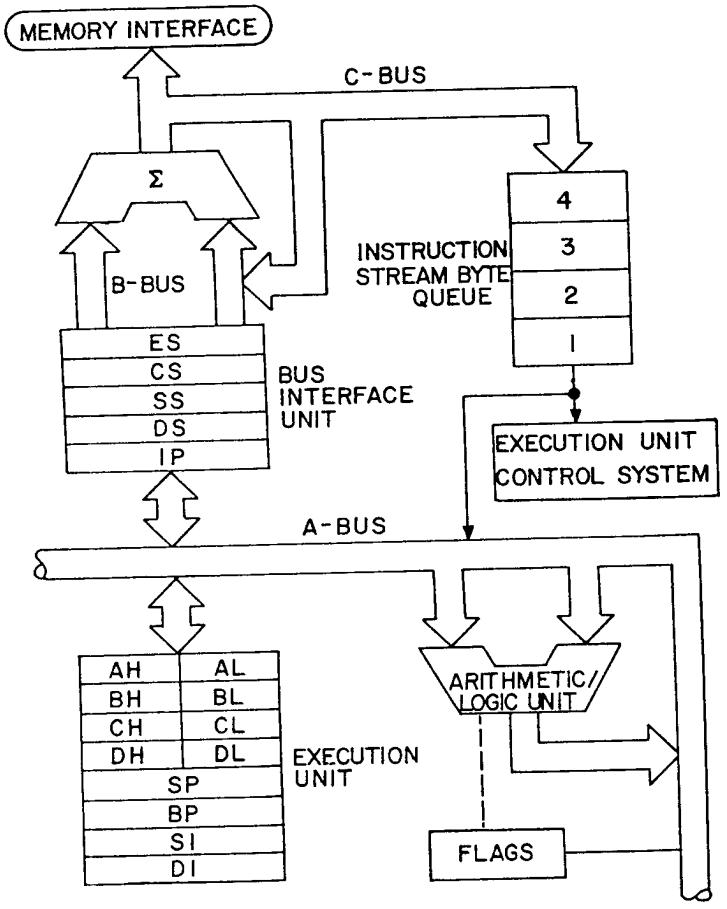
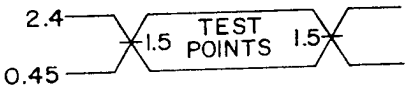


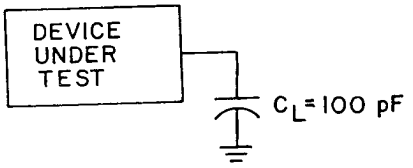
FIGURE 2. Block diagram.

SWITCHING TEST (INPUT/OUTPUT WAVEFORM)



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0".

SWITCHING TEST (LOAD CIRCUIT)



C_L includes jig capacitance.

FIGURE 3. Switching tests.

BASIC SYSTEM TIMING

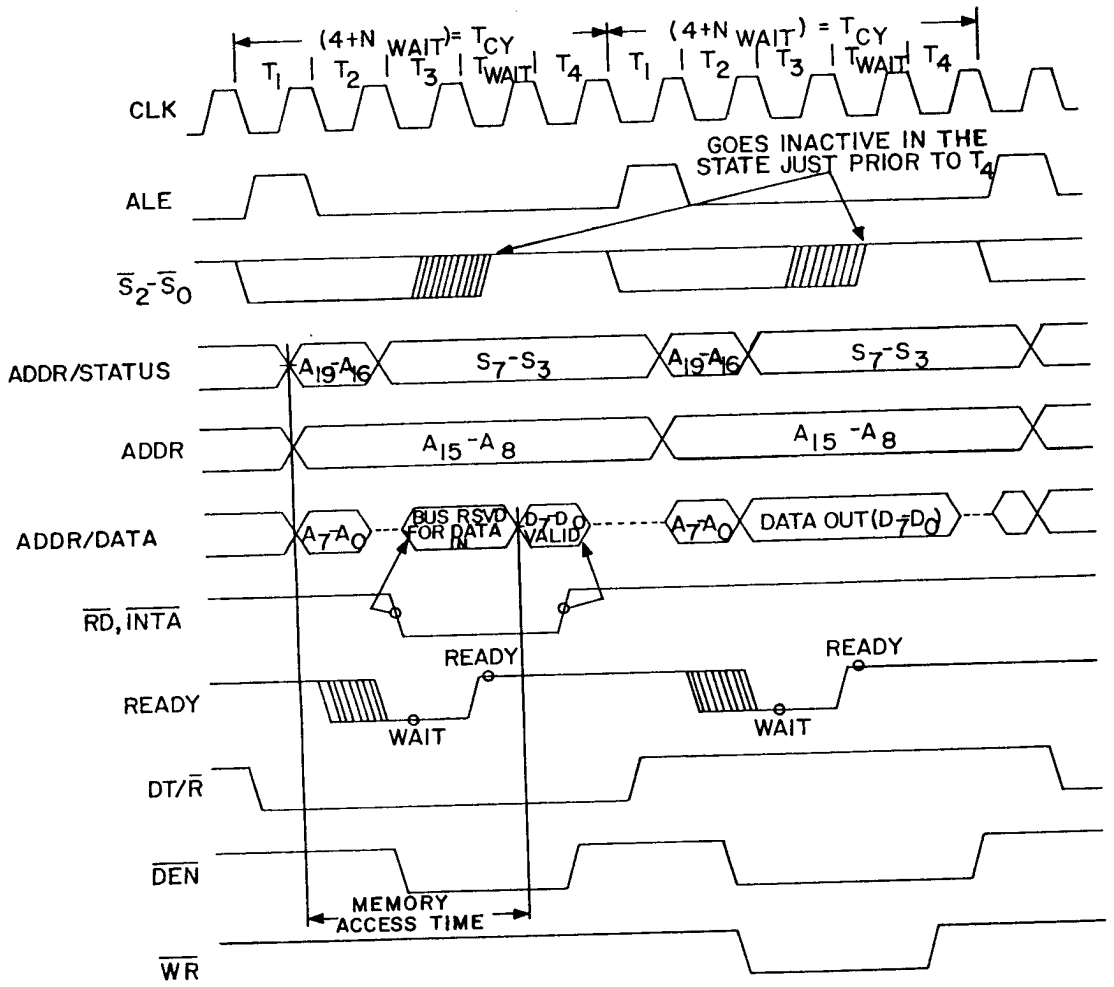


FIGURE 4. Switching waveforms.

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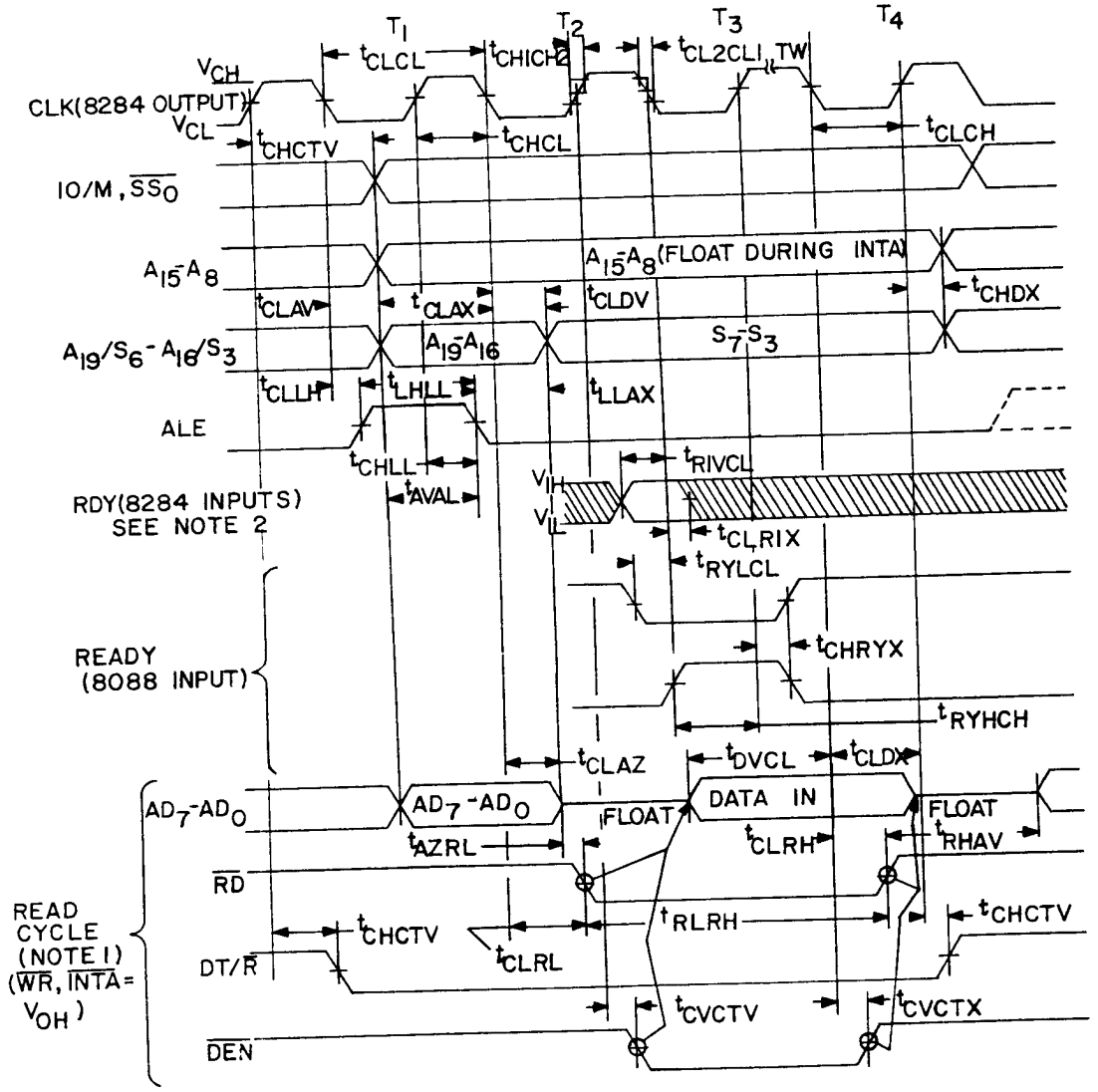
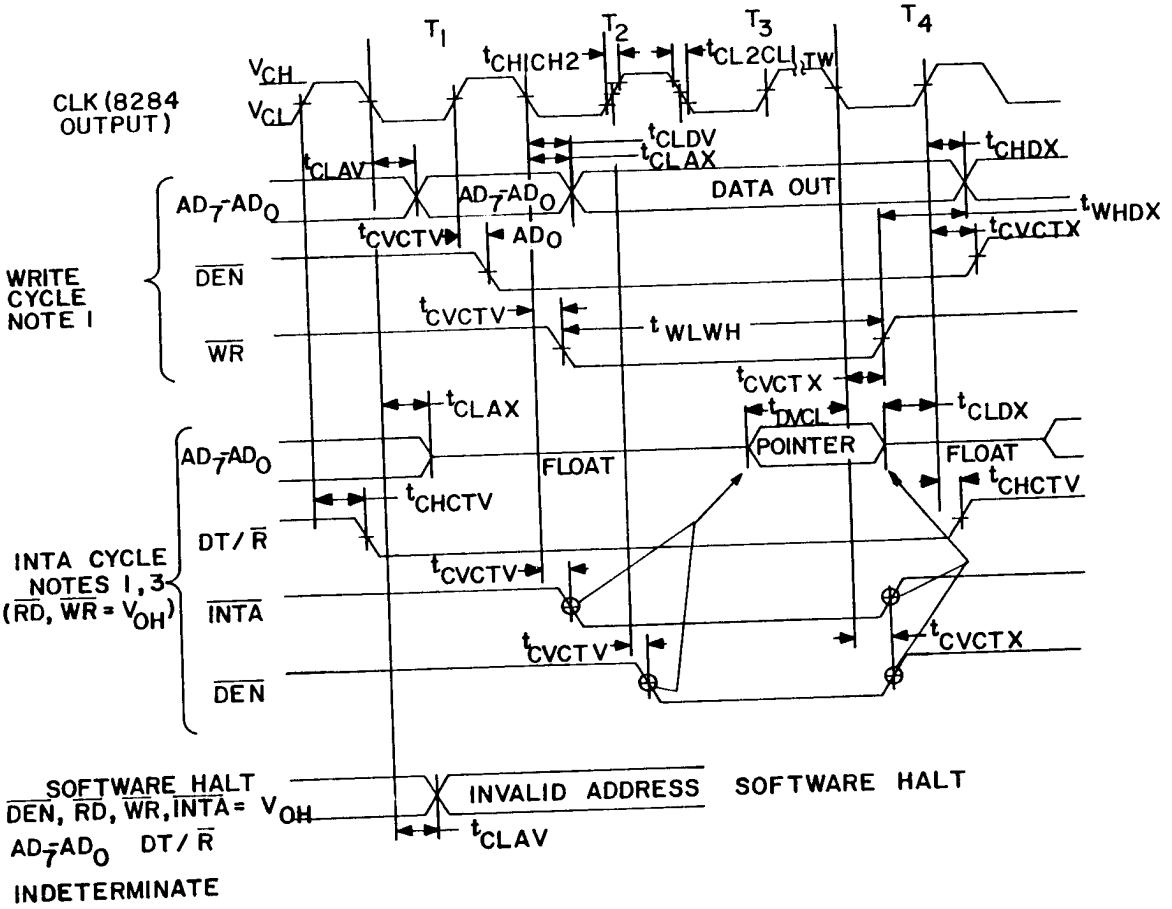
BUS TIMING - MINIMUM MODE SYSTEM



See notes on next page.

FIGURE 4. Switching waveforms - Continued.

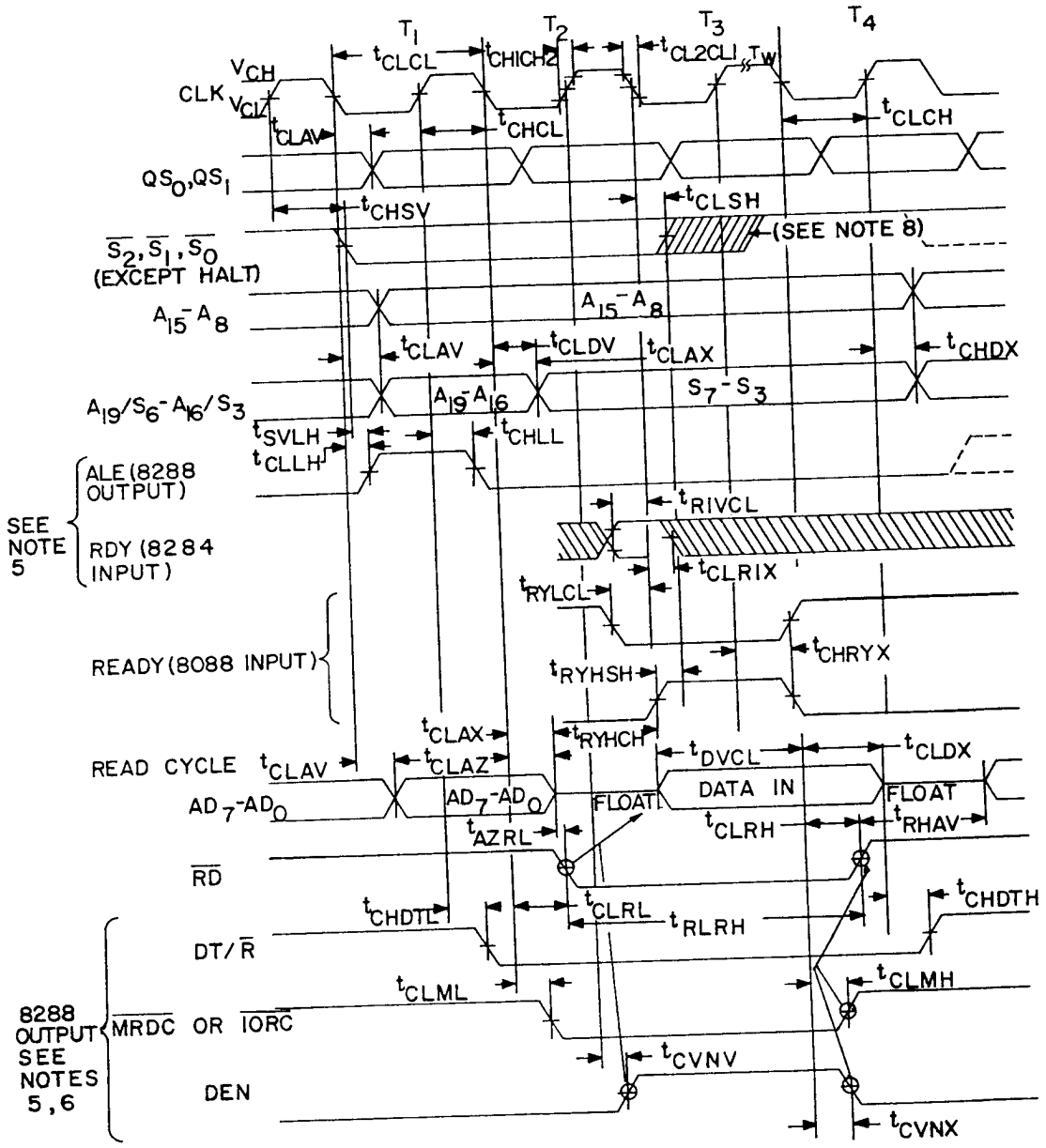
BUS TIMING-MINIMUM MODE SYSTEM (CONTINUED)



NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back to back. The 8088 local ADDR/DATA bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at 8284 are shown for reference only.
5. All timing measurements are made at 1.5 V unless otherwise noted.

FIGURE 4. Switching waveforms - Continued.

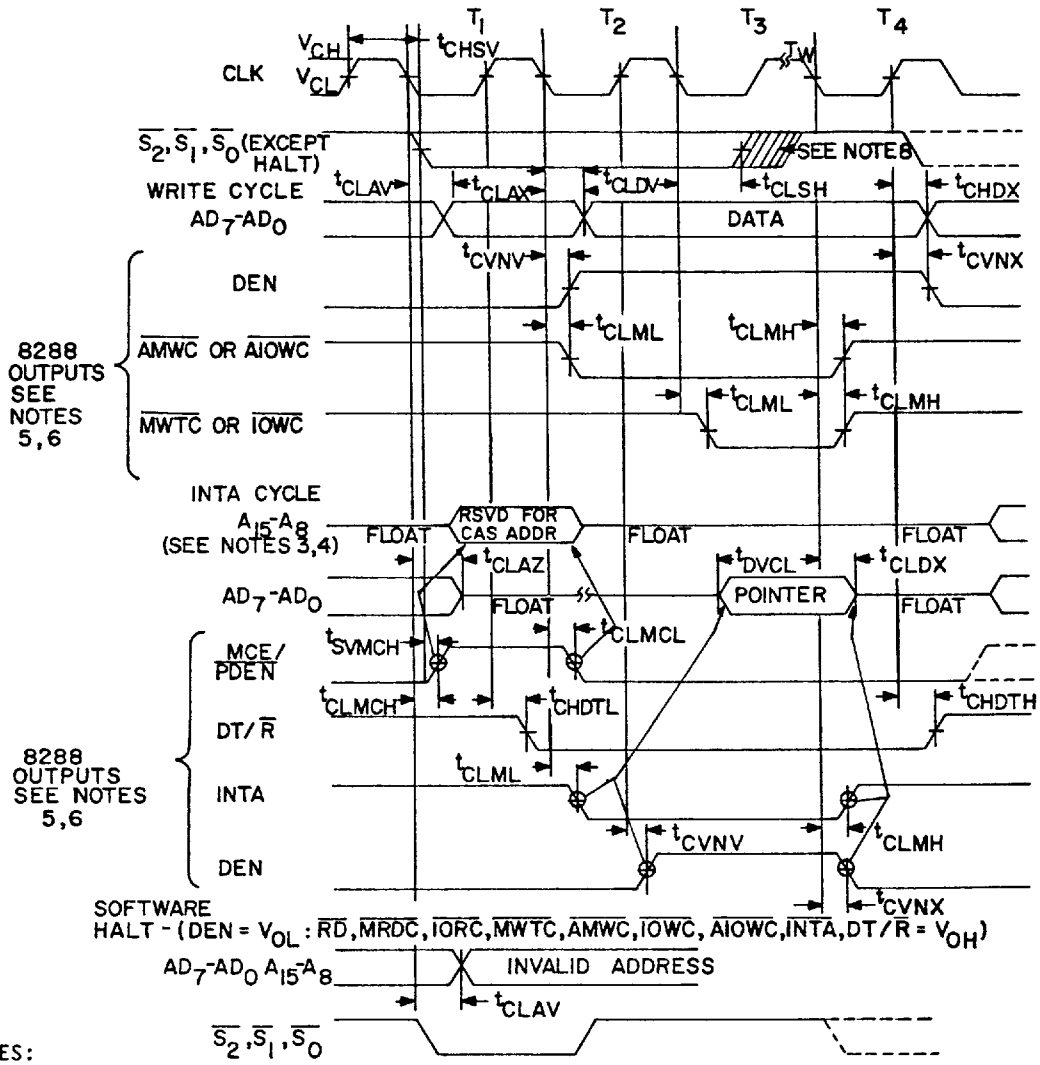
BUS TIMING - MAXIMUM MODE



See notes on next page.

FIGURE 4. Switching waveforms - Continued.

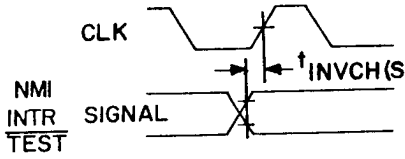
BUS TIMING-MAXIMUM MODE SYSTEM (USING 8288)



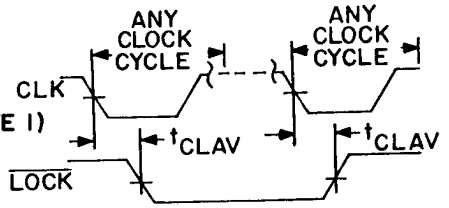
NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycles.
4. Two INTA cycles run back to back. The 8088 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 8284 or 8288 are shown for reference only.
6. The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA, and DEN) lags the active high 8288 CEN.
7. All timing measurements are made at 1.5 V unless otherwise noted.
8. Status inactive in state just prior to T_4.

FIGURE 4. Switching waveforms - Continued.

ASYNCHRONOUS SIGNAL RECOGNITION

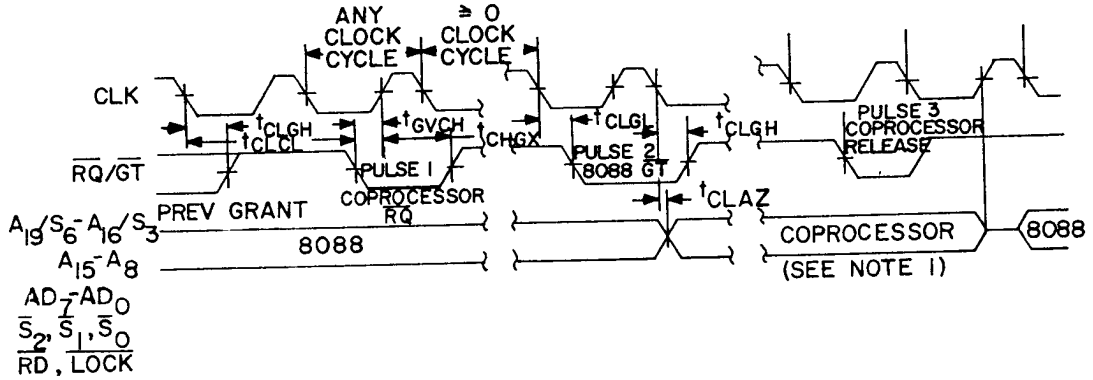


BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



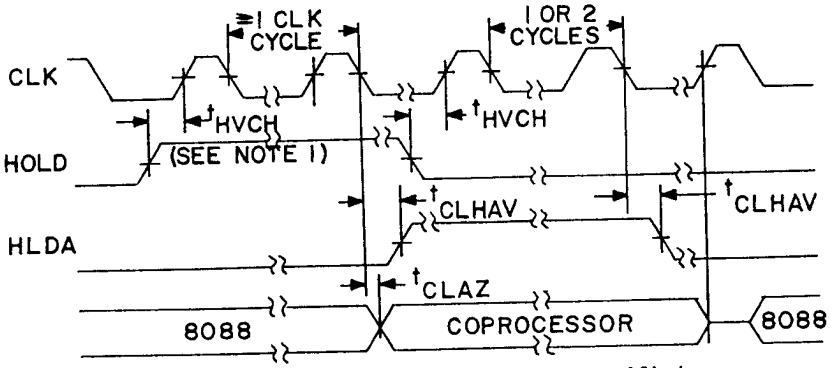
NOTE:
1. Set-up requirements for asynchronous signals only to guarantee recognition at next CLK.

REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE:
1. The coprocessor may not drive the buses outside the region shown without rising contention.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



NOTE:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.

FIGURE 4. Switching waveforms - Continued.

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{IO} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 shall include verification of instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8, 9,10,11
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Pin description. The following pin function descriptions are for 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 8088 (without regard to additional bus buffers).

Pin number	Name	I/O	Description
9-16	AD_7-AD_0	I/O	Address data bus. These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, and T_4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".
39, 2-8	A_{15}-A_8	O	Address bus. These lines provide address bits 8 through 15 for the entire bus cycle (T_1-T_4). These lines do not have to be latched by ALE to remain valid. A_{15}-A_8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".
35-38	A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3	O	Address/status. During T_1, these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2,T_3,T_W and T_4. S_6 is always LOW. The status of the interrupt enable flat bit (S_5) is updated at the beginning of each clock cycle S_4 and S_3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge".

S_4	S_3	Characteristics
0 (LOW)	0	Alternate data
0	1	Stack
1 (HIGH)	0	Code or none
1	1	Data
S_6 is 0 (LOW)		

Pin number	Name	I/O	Description
32	$\overline{RD}$	O	Read. Read strobe indicates that the processor is performing a memory or I/O read cycle depending on the state of the IO/$\overline{M}$ pin or S_2. This signal is used to read devices which reside on the 8088 local bus. $\overline{RD}$ is active LOW during T_2,T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 8088 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge".
22	READY	I	READY. The acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 8284 clock generator to form READY. This signal is active HIGH. The 8088 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
18	INTR	I	Interrupt request. A level-triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
23	$\overline{TEST}$	I	$\overline{TEST}$. Input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues; otherwise, the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
17	NMI	I	Non maskable interrupt. An edge-triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
21	RESET	I	RESET. Causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
19	CLK	I	Clock. Provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing.

Pin number	Name	I/O	Description
40	V_{CC}		V_{CC}. The +5 V ±10% power supply pin.
1, 20	GND		GND. The ground pins.
33	MIN/$\overline{MX}$	I	Minimum/maximum. Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.
28	IO/$\overline{M}$	O	Status line. An inverted maximum mode $\overline{S}_2$. It is used to distinguisn a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge."
29	$\overline{WR}$	O	Write. Strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T_2,T_3, and T_W of any write cycle. It is active LOW and floats to 3-state OFF in local bus "hold acknowledge".
24	$\overline{INTA}$	O	INTA. Used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2,T_3 and T_W of each interrupt acknowledgement cycle.
25	ALE	O	Address latch enable. Provided by the processor to latch the address into 8282/8283 address latch. It is a HIGH pulse active during clock low of T_1 of any bus cycle. Note that ALE is never floated.
27	DT/$\overline{R}$	O	Data transmit/receive. Needed in a minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S}_1$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T-HIGH, R-LOW). This signal floats to 3-state OFF in local bus "hold acknowledge".
26	$\overline{DEN}$	O	Data enable. Provided as an output enable for the 8286/8287 in a minimum system that uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T_2 until the middle of T_4; while for a write cycle, it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge".

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-87685012X	34335	8088/BQA	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088