

KK8137

DUAL 5.1V REGULATOR WITH DISABLE AND RESET

The KKA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1 V at currents up to 1 A. An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated voltage value. Output 2 can be disabled by TTL input. Short circuit and thermal protections are included.

- Output currents up to 1 A
- Fixed precision OUTPUT voltages 5.1 V ± 2%
- OUTPUT 1 with RESET facility
- OUTPUT 2 with DISABLE by TTL input
- Short circuit protection at both outputs
- Thermal protection
- Low drop output voltage



**TO-220AB/7
HEPTAWAT
(Plastic Package)**

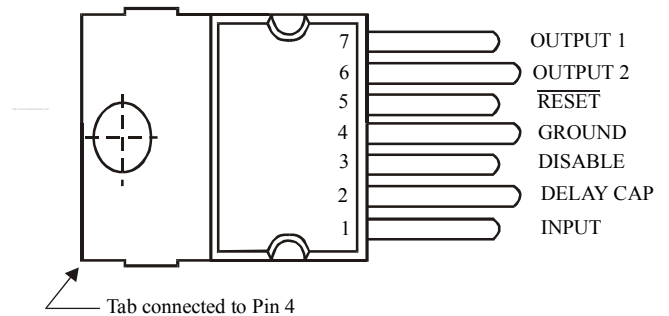
ORDERING INFORMATION

KK8137A Plastic Package

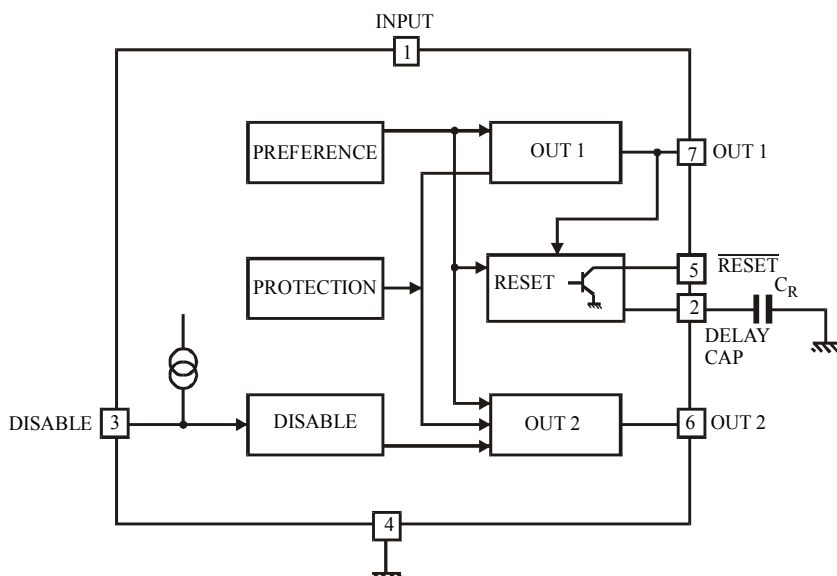
KK8137A chip

$T_J = -0^\circ$ to 130°C

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{IN}	DC Input Voltage Pin 1		20	V
V _{DIS}	Disable Input Voltage Pin 3		20	V
V _{RST}	Voltage at Pin 5		20	V
I _{O1,2 SC}	Short Circuit Output Current	$V_{IN} = 7\text{ V}$	1.6	A
		$V_{IN} = 16\text{ V}$	1.0	
T _{stg}	Storage Temperature	-65	150	°C
T _J	Junction Temperature	0	150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{IN}	DC Input Voltage Pin 1	7.0	14	V
V _{DIS}	Disable Input Voltage Pin 3	0	7.0	V
V _{RST}	Voltage at Pin 5		10	V
I _{O1,2}	Output Currents		1.0	A
T _J	Junction Temperature	0	130	°C

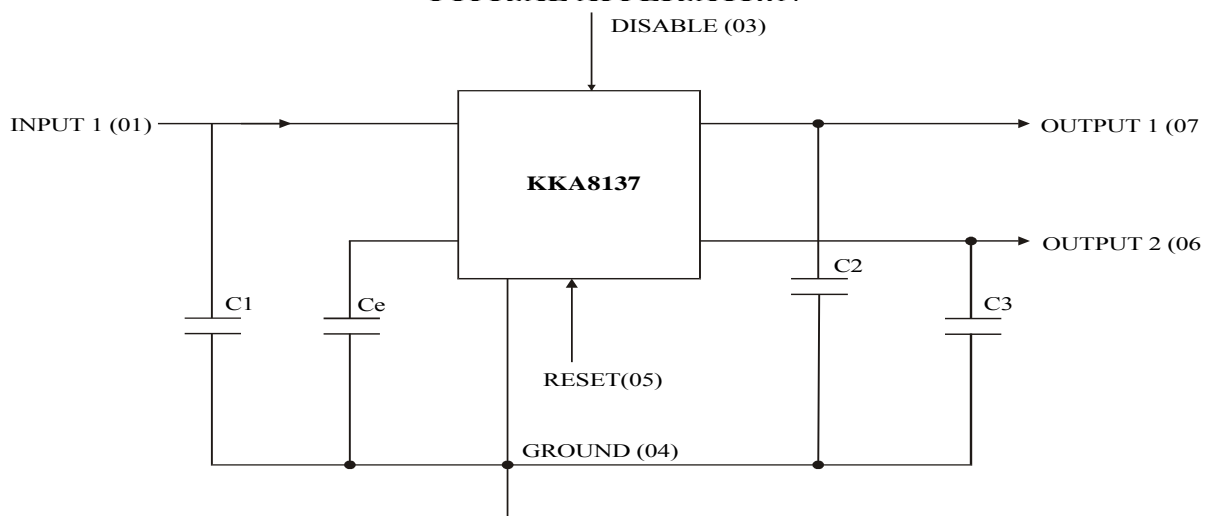
THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th (j-c)}	Maximum Thermal Resistance Junction-case	6	°C/W
R _{th (j-a)}	Maximum Thermal Resistance Junction-ambient	60	°C/W

ELECTRICAL CHARACTERISTICS ($V_{IN} = 7\text{ V}$, $T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
$V_{O1,2}$	Output Voltage	$V_{IN} = 7\text{ V}$, $V_{DIS} = 2.0\text{ V}$, $I_{O1} = -10\text{ mA}$	5.0	5.2	V
		$7\text{ V} \leq V_{IN} \leq 14\text{ V}$, $-5\text{ mA} \leq I_{O1} \leq -750\text{ mA}$, $V_{DIS} = 2.0\text{ V}$	4.9	5.3	
$\Delta V_{O1,2LI}$	Line Regulation	$7\text{ V} \leq V_{IN} \leq 14\text{ V}$, $I_{O1,2} = -200\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		50	mV
$\Delta V_{O1,2LO}$	Load Regulation	$V_{IN} = 7\text{ V}$, $-5\text{ mA} \leq I_{O1,2} \leq -0.6\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		100	mV
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2} = -750\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		1.4	V
I_Q	Quiescent Current	$I_{O1,2} = -1.0\text{ mA}$, $V_{DIS} = 2.0\text{ V}$		2.0	mA
		$V_{IN1} = 7\text{ V}$, $V_{IN2} = 10\text{ V}$, $V_{DIS} = 0.8\text{ V}$, $I_{O1} = -10\text{ mA}$		2.0	
I_{DIS}	Disable Bias Current	$0\text{ V} \leq V_{DIS} \leq 7\text{ V}$, $V_{IN} = 7\text{ V}$	-100	2.0	μA
V_{OIRST}	Reset Threshold Voltage	$K = V_{O1}$, $V_{DIS} = 2.0\text{ V}$	$K - 0.4$	$K - 0.1$	V
V_{RTH}	Reset Threshold Hysteresis	$V_{DIS} = 2.0\text{ V}$	20	75	mV
V_{RL}	Saturation Volt. at Pin 5 in Reset Condition	$V_5 = 5.0\text{ V}$, $V_{DIS} = 2.0\text{ V}$, $I_5 = 5.0\text{ mA}$		0.4	B
I_{RH}	Leakage Current at Pin 5 in Normal Condition	$V_5 = 10\text{ V}$, $V_{DIS} = 2.0\text{ V}$, $V_{IN} = 7\text{ V}$		10	μA
t_{RD}	Reset Pulse Delay at Pin 5	$V_{DIS} = 2.0\text{ V}$, $V_{IN} = 5\text{ V to } 7\text{ V}$	15	35	ns
V_{DISH}	Disable Voltage High (out 2 active)	$V_{IN} = 7\text{ V}$	2		V
V_{DISL}	Disable Voltage Low (out 2 disabled)	$V_{IN} = 7\text{ V}$		0.8	V

TYPICAL APPLICATION



$C1$ to $C3 = 10\ \mu\text{F}$

$$t_{RD} = \frac{C_e \bullet 2.5\text{V}}{10\ \mu\text{A}}$$

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