

General Description

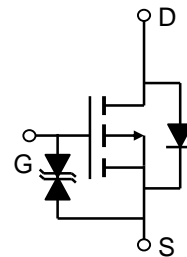
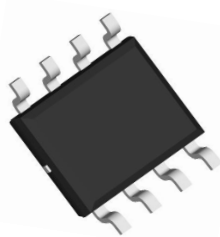
The AO4427 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications. The device is ESD protected

Features

$V_{DS} (V) = -30V$
 $I_D = -12.5 A (V_{GS} = -20V)$
 $R_{DS(ON)} < 12m\Omega (V_{GS} = -20V)$
 $R_{DS(ON)} < 14m\Omega (V_{GS} = -10V)$
 ESD Rating: 2KV HBM



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^{AF}	I_D	$T_A=25^\circ C$	A
		$T_A=70^\circ C$	
Pulsed Drain Current ^B	I_{DM}	-60	
Power Dissipation ^A	P_D	$T_A=25^\circ C$	3
		$T_A=70^\circ C$	2.1
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{AF}	$R_{\theta JA}$	$t \leq 10s$	28	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	54	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	21	30	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±25V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1.7	-2.5	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-20V, I _D =-12.5A T _J =125°C		9.4	12	mΩ
		V _{GS} =-10V, I _D =-10A		11.5	14	
		V _{GS} =-4.5V, I _D =-5A		32		mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-12.5A		24		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V			-1	V
I _S	Maximum Body-Diode Continuous Current				-4.2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		2330	2900	pF
C _{oss}	Output Capacitance		480			pF
C _{rss}	Reverse Transfer Capacitance		320	448		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	3.4	6.8	10	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-12.5A		41	52	nC
Q _{gs}	Gate Source Charge		10			nC
Q _{gd}	Gate Drain Charge		12			nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =1.2Ω, R _{GEN} =3Ω		12.8		ns
t _r	Turn-On Rise Time		10.3			ns
t _{D(off)}	Turn-Off DelayTime		49.5			ns
t _f	Turn-Off Fall Time		29			ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-12.5A, dI/dt=100A/μs		28	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-12.5A, dI/dt=100A/μs		20		nC

A: The value of R_{θJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s junction to ambient thermal resistance rating.

Rev8: Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

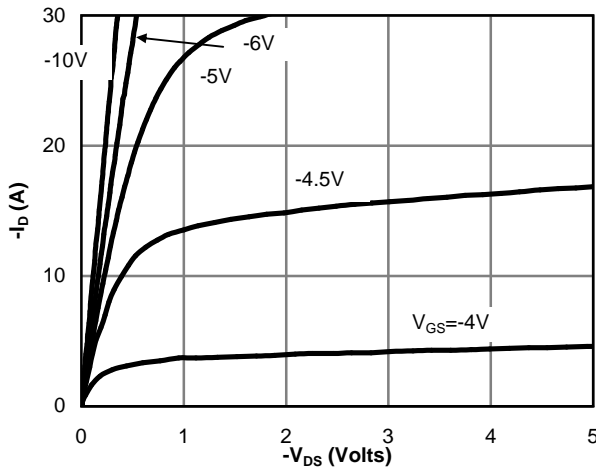


Figure 1: On-Region Characteristics

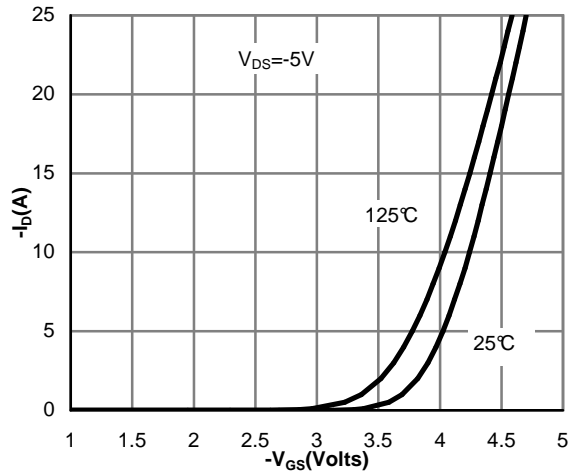


Figure 2: Transfer Characteristics

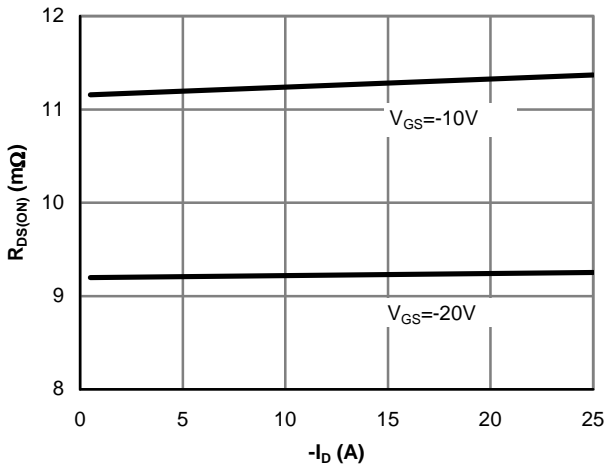


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

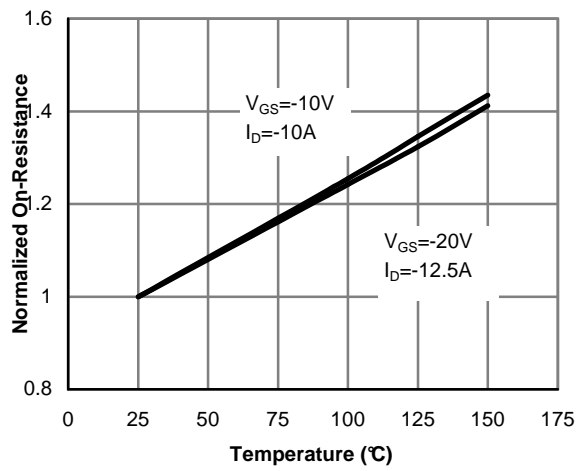


Figure 4: On-Resistance vs. Junction Temperature

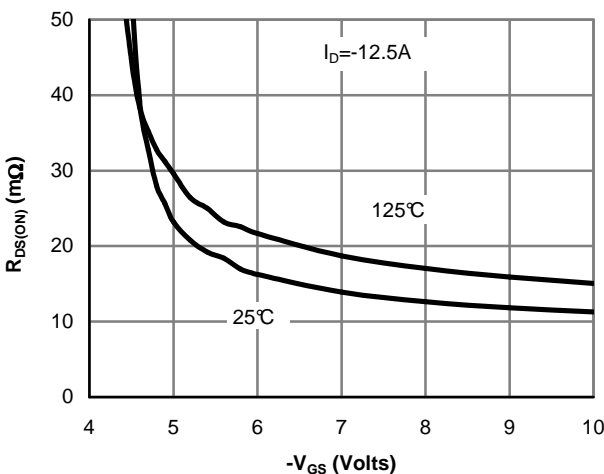


Figure 5: On-Resistance vs. Gate-Source Voltage

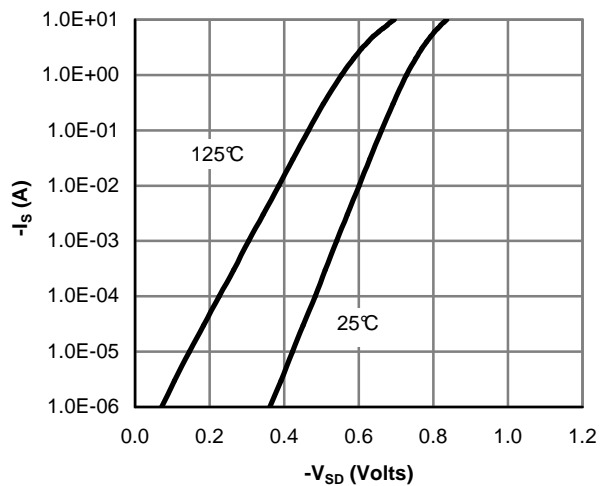


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

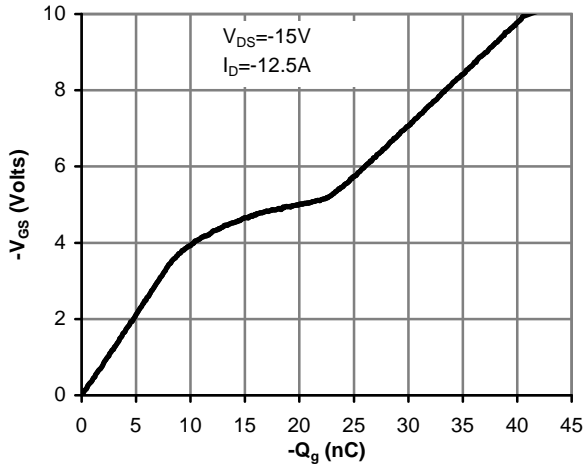


Figure 7: Gate-Charge Characteristics

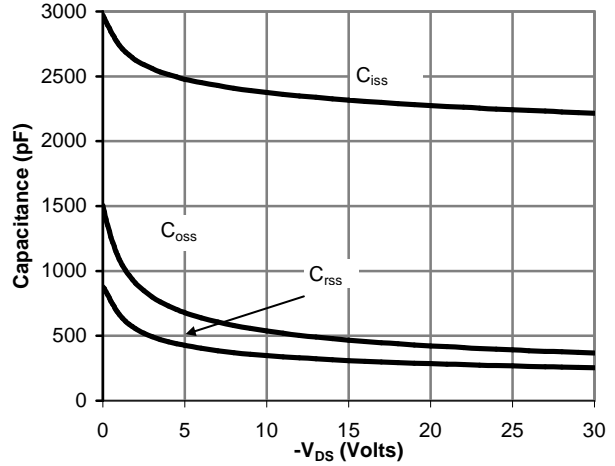


Figure 8: Capacitance Characteristics

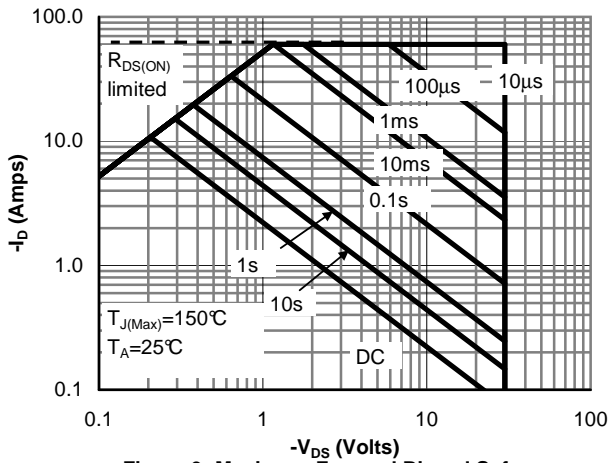


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

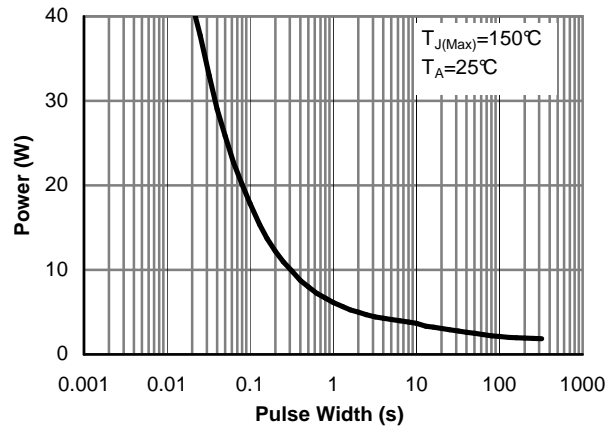


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

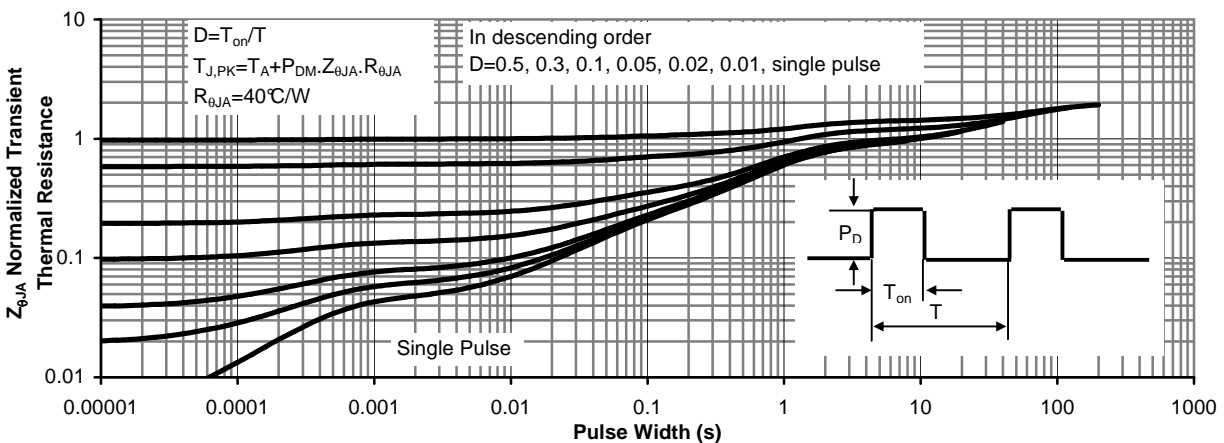


Figure 11: Normalized Maximum Transient Thermal Impedance