REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Z for vendor CAGE 27014. Editorial changes throughout.	97-01-28	Ray Monnin
B	Change limits for test parameter Differential non-linearity, group A subgroup 2 to ± ¾ max LSB. -lgt	99-07-21	Ray Monnin

REV																			
SHEET																			
REV	B	B	B	B	B	B													
SHEET	15	16	17	18	19	20													

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Sandra Rooney

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
94-08-18

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, 12-BIT + SIGN DATA, ACQUISITION SYSTEM WITH SELF-CALIBRATION, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-93195**

SHEET 1 OF 20

DSCC FORM 2233
APR 97

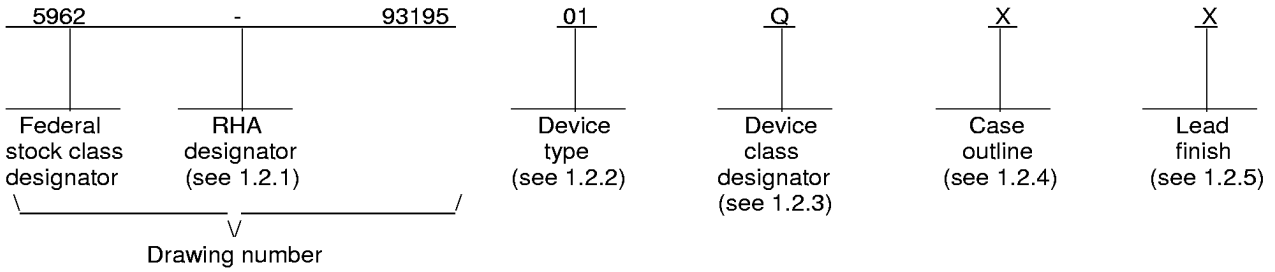
5962-E384-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	12458	12-bit + sign data acquisition system with self-calibration, 5 MHz
02	12H458	12-bit + sign data acquisition system with self-calibration, 8 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	44	Leaded chip carrier
Y	See figure 1	44	Quad flat pack
Z	See figure 1	44	Gullwing lead chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{A+} and V_{D+})	6.0 V
Voltage at input and output pins except IN0-IN7	-0.3 V to V^+ + 0.3 V
Voltage at analog inputs IN0-IN7	GND - 5 V to V^+ + 5 V
$\lvert V_{A+} - V_{D+} \rvert$	300 mV
Input current at any pin 2/	±5 mA
Package input current 2/	±20 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D):	
Case X	1.75 W
Cases Y and Z	2.5 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	3.5°C/W
Cases Y and Z	5.8°C/W
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-ambient(θ_{JA}):	
Case X	70°C/W
Cases Y and Z	50°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{A+} and V_{D+})	3.0 V to 5.5 V
Supply voltage $\lvert V_{A+} - V_{D+} \rvert$	≤ 100 mV
V_{IN+} Input range	$GND \le V_{IN+} \le V_{A+}$
V_{IN-} Input range	$GND \le V_{IN-} \le V_{A+}$
V_{REF+} Input voltage	$1\ V \le V_{REF+} \le V_{A+}$
V_{REF-} Input voltage	$0\ V \le V_{REF-} \le V_{REF+} - 1\ V$
$V_{REF+} - V_{REF-}$	$1\ V \le V_{REF} \le V_{A+}$
V_{REF} Common mode range 3/	$0.1\ V_{A+} \le V_{REFCM} \le 0.6\ V_{A+}$

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > (V_{A+}$ or $V_{D+})$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current of 5 mA, to simultaneously exceed the power supply voltages.

3/ V_{REFCM} (Reference voltage common mode range) is defined as $(V_{REF+} + V_{REF-})/2$.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figures 1, 2, and 3.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 4.

3.2.3 Block diagram(s). The block or logic diagram(s) shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 93 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive and negative integral linearity error	$\pm E_{IL}$	After auto-cal	1, 2, 3	All		±1	LSB
Resolution with no missing codes	RES	After auto-cal	1, 2, 3	All		13	Bits
Differential nonlinearity	E_{DL}	After auto-cal	1, 3	All		±1/2	LSB
			2			±3/4	
Zero error	E_Z	After auto-cal	1, 2, 3	All		±1	LSB
Positive full-scale error	$+E_{FS}$	After auto-cal	1, 2, 3	All		±2	LSB
Negative full-scale error	$-E_{FS}$	After auto-cal	1, 2, 3	All		±2	LSB
DC common mode error	CME	2/	1, 2, 3	All		±3.5	LSB
8-Bit +sign and "watchdog" mode positive and negative integral linearity error	I_{LE}		1, 2, 3	All		±1/2	LSB
8-Bit +sign and "watchdog" mode total unadjusted error	E_{TU}	After auto-zero	1, 2, 3	All		±3/4	LSB
8-Bit +sign and "watchdog" mode resolution with no missing codes	WRES		1, 2, 3	All		9	Bits
8-Bit +sign and "watchdog" mode differential non-linearity	D_{NL}		1, 2, 3	All		±1/2	LSB
8-Bit +sign and "watchdog" mode zero error	W_{ZE}	After auto-zero	1, 2, 3	All		±1/2	LSB
8-Bit +sign and "watchdog" positive and negative full-scale error	WFSE		1, 2, 3	All		±1/2	LSB
Differential input voltage range	V_{DIF}		1, 2, 3	All	Gnd	V_{A+}	V
Common mode input voltage range	V_{CMI}		1, 2, 3	All	Gnd	V_{A+}	V
Power supply sensitivity	P_{SS}	Zero error 3/ $V_{A+} = V_{D+} = 5$ V ±10 %	1, 2, 3	All		±1.75	LSB
		Full-scale error $V_{REF+} = 4.5$ V, V_{REF-} = Gnd				±2.00	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{D+} supply current	I_{D+}	$\overline{CS}$ = "1" 4/	1, 2, 3	All		1.0	mA
V_{A+} supply current	I_{A+}	$\overline{CS}$ = "1" 4/	1, 2, 3	All		5.0	mA
Multiplexer ON-channel leakage current	I_{LON}	V_{A+} = 5.5 V 4/ ON-channel = 5.5 V, OFF-channel = 0 V	1, 2, 3	All		0.3	µA
		V_{A+} = 5.5 V 4/ ON-channel = 0 V, OFF-channel = 5.5 V					
Multiplexer OFF-channel leakage current	I_{LOFF}	V_{A+} = 5.5 V 4/ ON-channel = 5.5 V, OFF-channel = 0 V	1, 2, 3	All		0.3	µA
		V_{A+} = 5.5 V 4/ ON-channel = 0 V, OFF-channel = 5.5 V					
Internal reference output voltage	V_{REFOUT}	$V_{A+} = V_{D+}$ = 5 V 5/	1, 2, 3	All	2.4	2.6	V
Internal reference load regulation	REFL	Sourcing ($0 < I_L \le +4$ mA) $V_{A+} = V_{D+}$ = 5 V	1, 2, 3	All		0.2	%/mA
		Sinking ($-1 \le I_{IL} < 0$ mA) $V_{A+} = V_{D+}$ = 5 V				1.2	
Line regulation	V_{REF}	$4.5 V \le V_{A+} \le 5.5 V$ $V_{A+} = V_{D+}$ = 5 V	1, 2, 3	All		15	mV
Internal reference short circuit current	I_{SC}	V_{REFOUT} = 0 V $V_{A+} = V_{D+}$ = 5 V	1, 2, 3	All		25	mA
Logical "1" input voltage	$V_{IN}(1)$	$V_{A+} = V_{D+}$ = 5.5 V 6/	1, 2, 3	All	2.0		V
Logical "0" input voltage	$V_{IN}(0)$	$V_{A+} = V_{D+}$ = 4.5 V 6/	1, 2, 3	All		0.8	V
Logical "1" input current	$I_{IN}(1)$	V_{IN} = 5 V 6/	1, 2, 3	All		1.0	µA
Logical "0" input current	$I_{IN}(0)$	V_{IN} = 0 V 6/	1, 2, 3	All	-1.0		µA
Logical "1" output voltage	$V_{OUT}(1)$	$V_{A+} = V_{D+}$ = 4.5 V, 6/ I_{OUT} = -360 µA	1, 2, 3	All	2.40		V
		$V_{A+} = V_{D+}$ = 4.5 V, 6/ I_{OUT} = -10 µA			4.25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical "0" output voltage	$V_{OUT}(0)$	$V_{A+} = V_{D+} = 4.5$ V 6/ $I_{OUT} = 1.6$ mA	1, 2, 3	All		0.4	V
TRI-STATE output leakage current	I_{OUT}	$V_{OUT} = 0$ V 6/	1, 2, 3	All	-3.0		µA
		$V_{OUT} = 5$ V 6/				3.0	
Clock duty cycle	t_{CLK}		9, 10, 11	All	40	60	%
Conversion time	t_C	13-Bit resolution sequencer state S5	9, 10, 11	All		44 (t_{CLK}) +50	ns
		9-Bit resolution sequencer state S5				21 (t_{CLK}) +50	
Acquisition time	t_A	Sequencer State S7 built-in minimum for 13-bits	9, 10, 11	All		9 (t_{CLK}) +50	ns
		Built-in minimum for 9-bits and "watchdog" mode				2 (t_{CLK}) +50	
Auto-zero time	t_Z	Sequencer State S2	9, 10, 11	All		76 (t_{CLK}) +50	ns
Full calibration time	t_{CAL}	Sequencer State S2	9, 10, 11	All		4944 (t_{CLK}) +50	ns
"Watchdog" mode comparison time	t_{WD}	Sequencer States S6, S4 and S5	9, 10, 11	All		11 (t_{CLK}) +50	ns
$\overline{CS}$ or address valid to ALE low set-up time	$t_{1,3}$	7/, See figure 6.	9, 10, 11	All	40		ns
$\overline{CS}$ or address valid to ALE low hold time	$t_{2,4}$	7/, See figure 6.	9, 10, 11	All	20		ns
ALE Pulse width	t_5	7/, See figure 6	9, 10, 11	All	45		ns
$\overline{RD}$ high to next ALE high	t_6	7/, See figure 6	9, 10, 11	All	35		ns
ALE low to $\overline{RD}$ low	t_7	7/, See figure 6	9, 10, 11	All	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RD}$ pulse width	t_8	7/, See figures 6 and 7	9, 10, 11	All	100		ns
$\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low	t_9	7/, See figures 6 and 7	9, 10, 11	All	100		ns
ALE low to $\overline{WR}$ low	t_{10}	7/, See figure 6	9, 10, 11	All	20		ns
$\overline{WR}$ pulse width	t_{11}	7/, See figures 6 and 7	9, 10, 11	All	60		ns
$\overline{WR}$ high to next ALE high	t_{12}	7/, See figure 6	9, 10, 11	All	75		ns
$\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low	t_{13}	7/, See figures 6 and 7	9, 10, 11	All	140		ns
Data valid to $\overline{WR}$ high set-up time	t_{14}	7/, See figures 6 and 7	9, 10, 11	All	40		ns
Data valid to $\overline{WR}$ high hold time	t_{15}	7/, See figures 6 and 7	9, 10, 11	All	30		ns
$\overline{RD}$ low to data bus out of TRI-STATE	t_{16}	7/, See figures 6 and 7	9, 10, 11	All	10	70	ns
$\overline{RD}$ high to TRI-STATE	t_{17}	R_L = 1 kΩ 7/ See figures 6 and 7	9, 10, 11	All	10	110	ns
$\overline{RD}$ low to data valid (access time)	t_{18}	7/, See figures 6 and 7	9, 10, 11	All	10	80	ns
Address invalid from $\overline{RD}$ or $\overline{WR}$ high (hold time)	t_{19}	7/, See figure 7	9, 10, 11	All	10		ns
$\overline{CS}$ low or address valid to $\overline{RD}$ low	t_{20}	7/, See figure 7	9, 10, 11	All	20		ns
$\overline{CS}$ low or address valid to $\overline{WR}$ low	t_{21}	7/, See figure 7	9, 10, 11	All	20		ns
$\overline{INT}$ high from $\overline{RD}$ low	t_{22}	7/, See figure 8	9, 10, 11	All	10	60	ns
DMARQ low from $\overline{RD}$ low	t_{23}	7/, See figure 8	9, 10, 11	All	10	60	ns

1/ $V_{A+} = V_{D+} = 5$ V, $V_{REF+} = 5$ V, $V_{REF-} = 0$ V, $R_S = 25\ \Omega$, 12-bit +sign conversion mode, source impedance for V_{REF+} and $V_{REF-} \le 25\ \Omega$, fully-differential input with fixed 2.5 V common-mode voltage, and minimum acquisition time. f_{CLK} = 5.0 MHz device for device type 01, f_{CLK} = 8.0 MHz for device type 02.

2/ DC common-mode error is measured with both inputs shorted together and driven from 0 V to 5 V. The measured value is referred to the resulting output value when the inputs are driven with a 2.5 V signal.

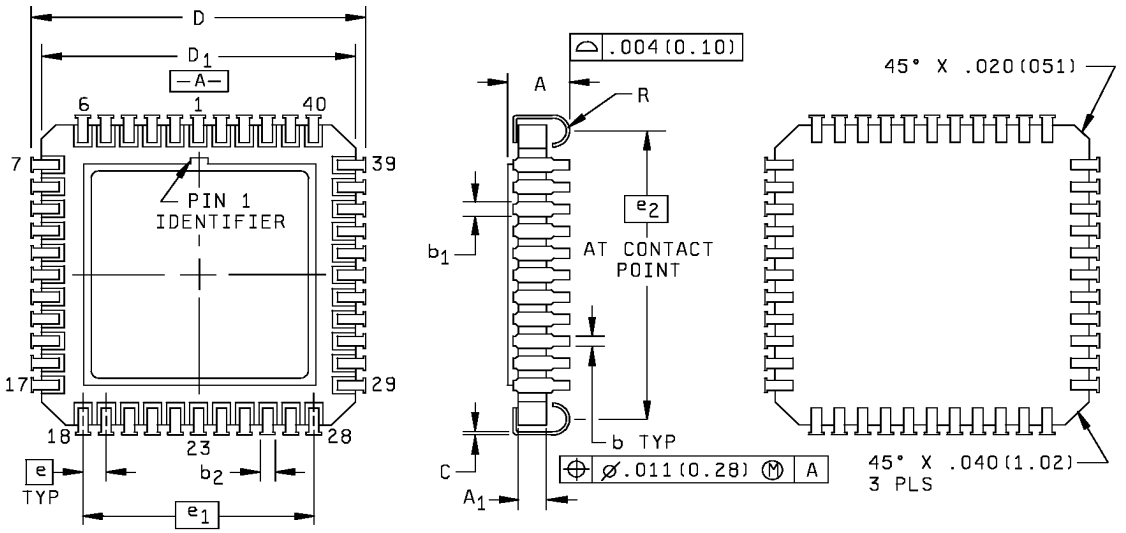
3/ Power supply sensitivity is measured after auto-zero and/or auto-calibration cycle has been completed with V_{A+} and V_{D+} at the specified extremes.

4/ $V_{REF+} = 5$ V, $V_{REF-} = 0$ V, $V_{A+} = V_{D+} = 5$ V, minimum acquisition time, f_{CLK} = 5.0 MHz for device type 01, f_{CLK} = 8.0 MHz for device type 02.

5/ Limit is ± 4%.

6/ $V_{REF+} = 5$ V, $V_{REF-} = 0$ V, $V_{A+} = V_{D+} = 5$ V, f_{CLK} = 5.0 MHz for device type 01, f_{CLK} = 8.0 MHz for device type 02.

7/ $V_{A+} = V_{D+} = +5$ V, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0-D15 outputs.

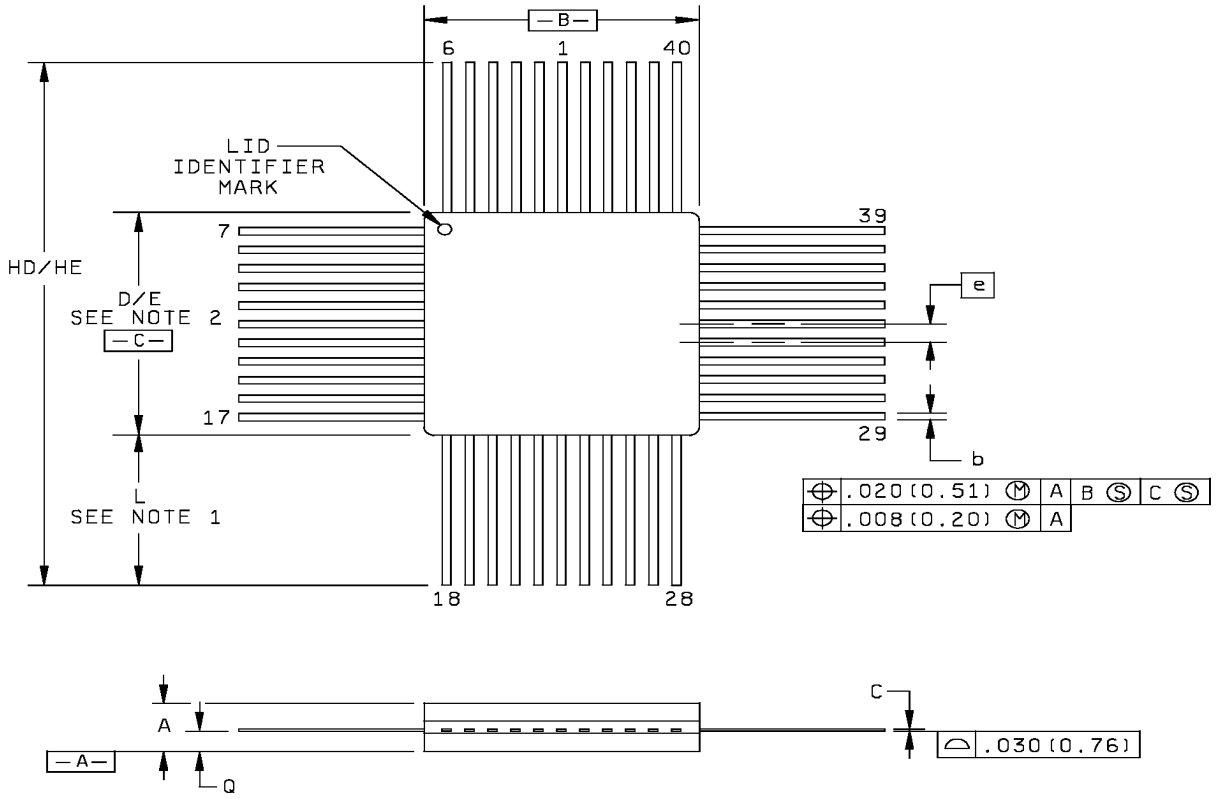


Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.101	.140	2.57	3.56
A_1	.054	.078	1.37	1.98
b	.013	.023	0.33	0.58
b_1	---	.030	---	0.76
b_2	---	.020	---	0.51
C	.006	.010	0.15	0.25
D	.680	.700	17.27	17.78
D_1	.640	.662	16.26	16.81
e	---	.050	---	1.27
e_1	---	.500	---	12.70
e_2	---	.630	---	16.00
R	---	.030	---	0.76

NOTES:

1. All exposed metal and metalized areas to be gold plated 60 microinches/1.5 micrometers minimum over 100 microinches/2.54 micrometers minimum nickel.
2. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline X.



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.108	.132	2.74	3.35
HD/HE	1.365	1.435	34.67	36.45
C	.005	.009	0.13	0.23
D/E	.575	.605	14.61	15.37
e	.050 BSC		1.27 BSC	
L	.395	.415	10.03	10.54
Q	.044	.060	1.12	1.52
b	.017	.023	.43	.58

NOTES:
1. Leadframe to be solder dipped 200 microinches/5.08 micrometers minimum, measured at crest of the major flats.
2. Dimension includes the offset of base and lid.
3. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 2. Case outline Y.

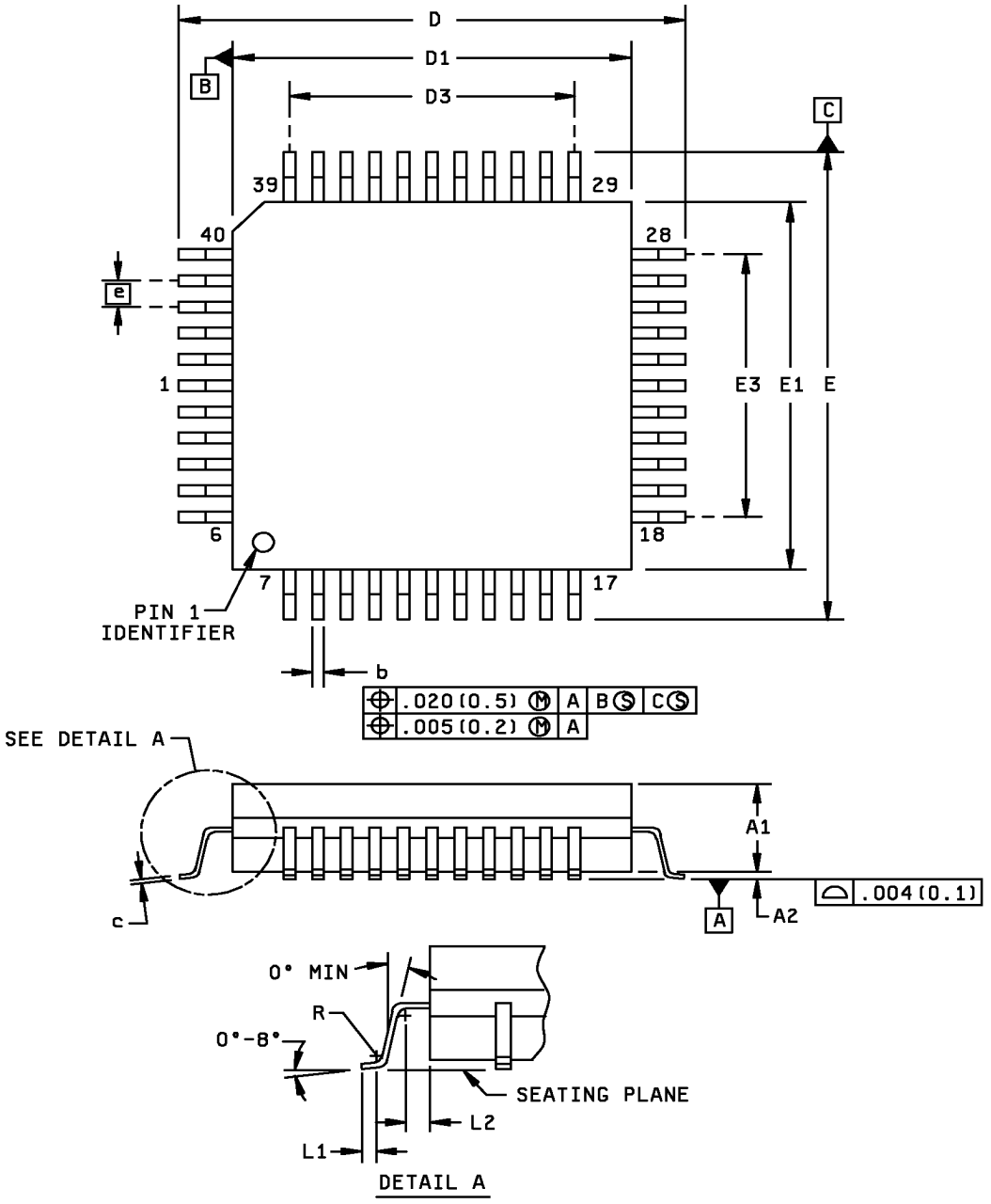


FIGURE 3. Case outline Z.

Symbol	Inches			Millimeters		
	Min	Max	Note	Min	Max	Note
A1	.108	.132		2.74	3.35	
A2	.020	.040		0.51	1.02	
b	.018	.022	2	0.46	0.56	2
c	.004	.008	2	0.10	0.20	2
D/E	.770	.790		19.56	20.07	
D1	.580	.600	3	14.73	15.24	3
D3/E3	.500 BSC			12.70 BSC		
e	.050 BSC			1.27 BSC		
E1	.500	.520	3	12.70	13.21	3
L1	.020	.030		0.51	0.76	
L2	.025	---		0.64	---	
R	.006 REF			0.15 REF		

NOTES:

1. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Lead finish: Solder dipped with Sn60 or Sn63 solder conforming to MIL-PRF-38535 to a minimum thickness of 200 microinches/5.08 micrometers. Solder may be applied over lead basis metal of Sn plate. Maximum limit may be increased by .003 in/0.08 mm after lead finish applied.
3. Dimension includes the offset of base and lid.

FIGURE 3. Case outline Z – Continued

Device type	All
Case outlines	X, Y, and Z
Terminal number	Terminal symbol
1	V_{A+}
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	D8
11	D9
12	V_{D+}
13	D10
14	D11
15	D12
16	D13
17	D14
18	D15
19	RD
20	WR
21	CS
22	ALE
23	CLK
24	A0
25	A1
26	A2
27	A3
28	A4
29	SYNC
30	BW
31	INT
32	DMARQ
33	GND
34	IN0
35	IN1
36	IN2
37	IN3
38	IN4
39	IN5
40	IN6
41	IN7
42	V_{REF-}
43	V_{REF+}
44	V_{REFOUT}

FIGURE 4. Terminal connections.

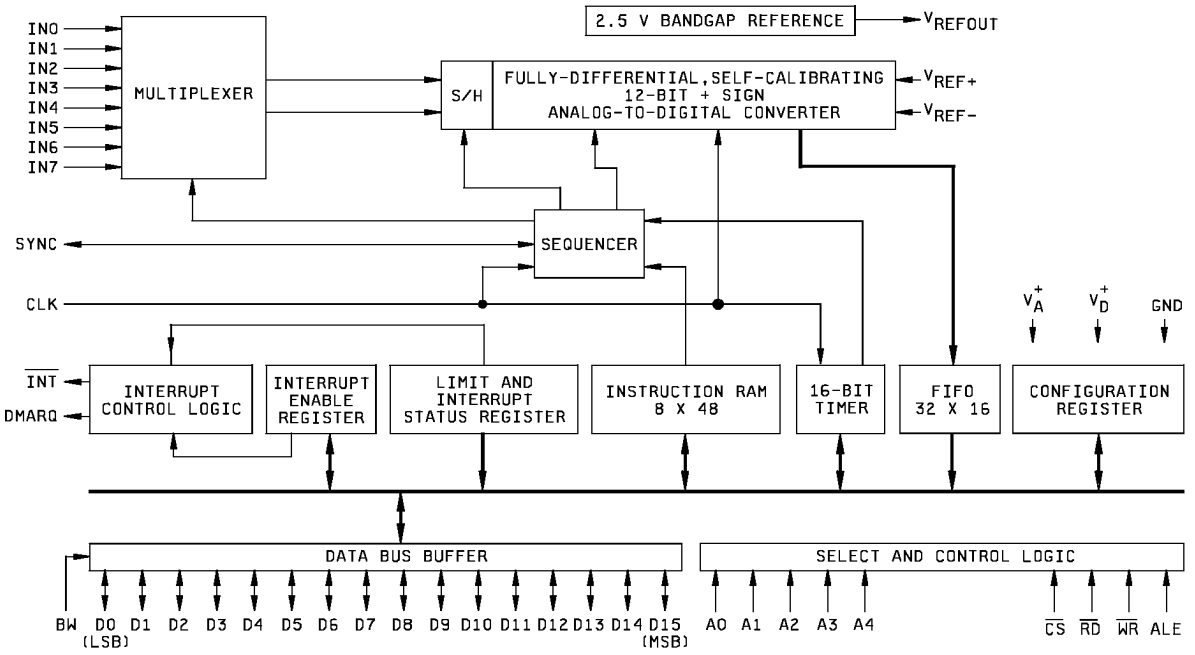


FIGURE 5. Block diagram.

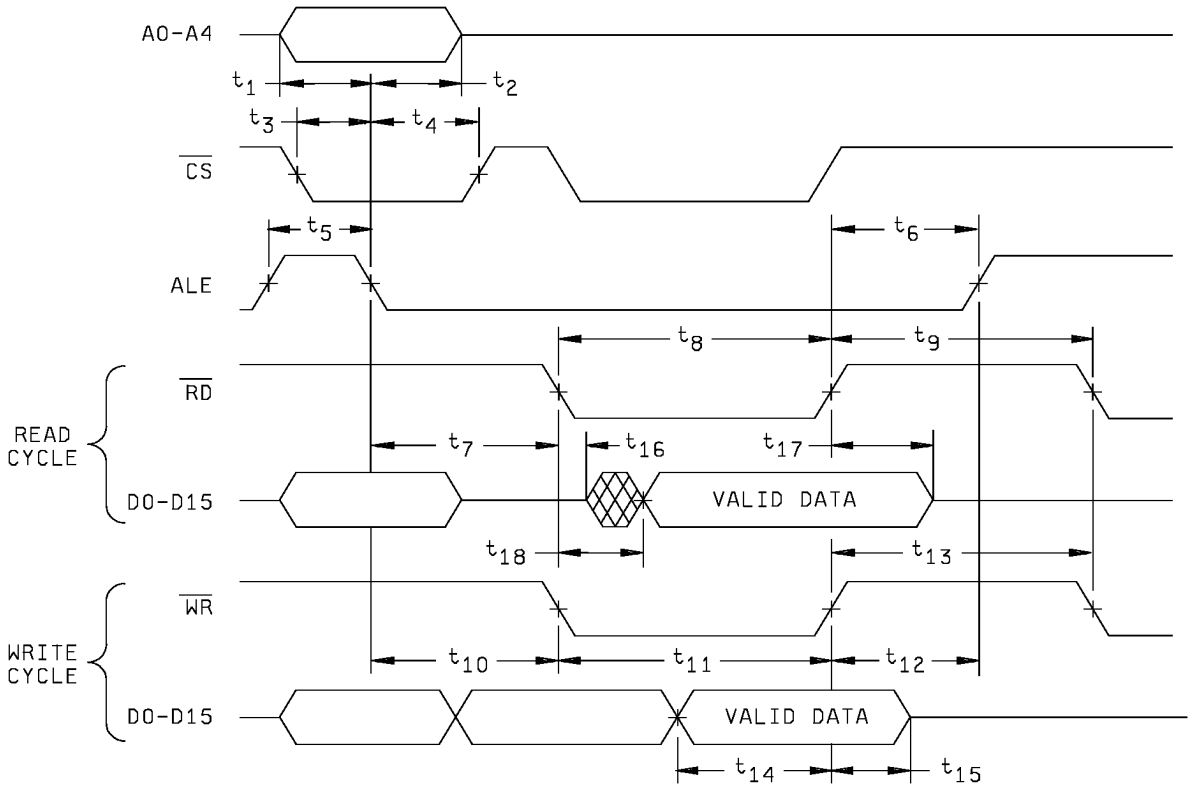


FIGURE 6. Multiplexed data bus.

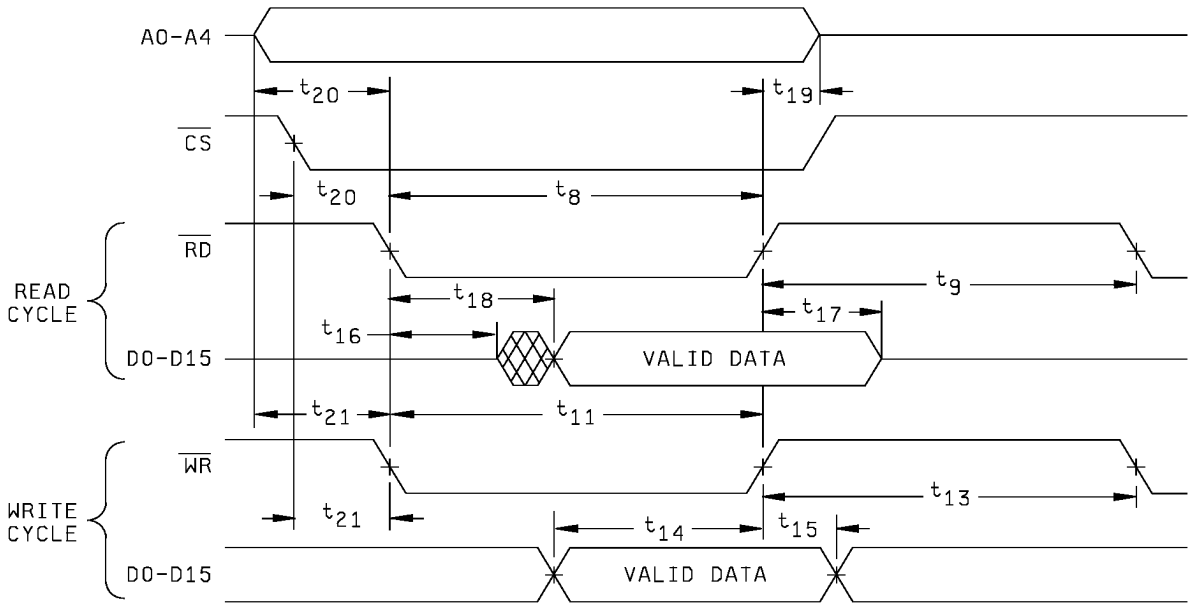


FIGURE 7. Non-multiplexed data bus (ALE = 1).

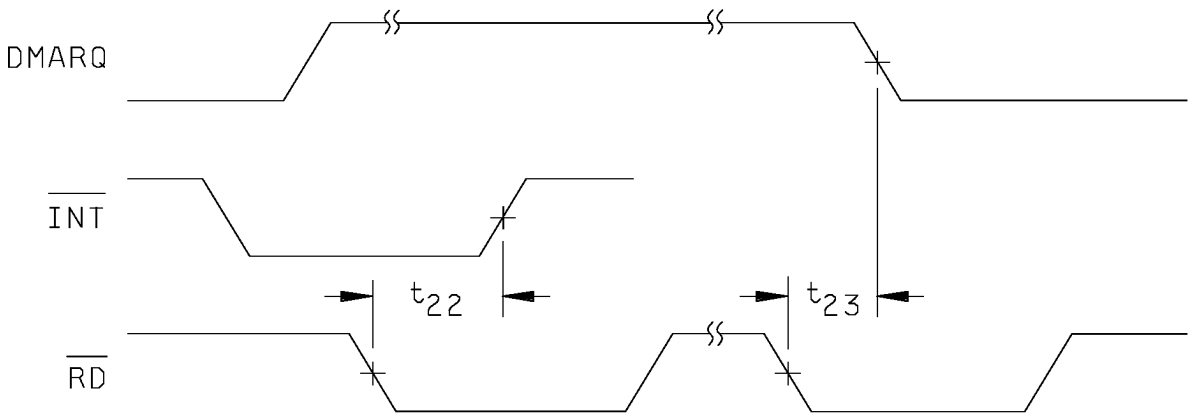


FIGURE 8. Interrupt and DMARQ.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 9, 10, 11 1/	1, 2, 3, 9, 10, 11 1/	1, 2, 3, 9, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-07-21

Approved sources of supply for SMD 5962-93195 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9319501MXC	3/	LM12458MEL/883
5962-9319501MYA	3/	LM12458MW/883
5962-9319502QZA	27014	LM12H458MWG/883
5962-9319502MXC	27014	LM12H458MEL/883
5962-9319502MYA	3/	LM12H458MW/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor Corporation 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.