MTM55N10
MTM60N06

Designer's Data Sheet

55 and 60 AMPERE

N-CHANNEL TMOS POWER FETs

$R_{DS(on)}$ = 0.04 OHM
100 VOLTS

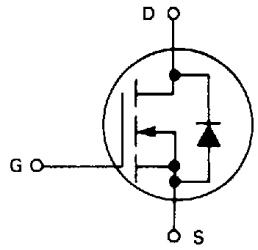
$R_{DS(on)}$ = 0.028 OHM
60 VOLTS

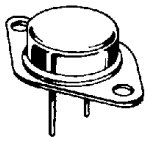
N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS®





CASE 197A-03
(TO-204AE)

MAXIMUM RATINGS

Rating	Symbol	MTM 60N06	MTM 55N10	Unit
Drain-Source Voltage	V_{DSS}	60	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 60 300	 55 275	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM60N06	$V_{(BR)DSS}$	60	—	Vdc
	MTM55N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
T_C = 125°C			—	100	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA), V_{DS} = V_{GS}		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 30 Adc)	MTM60N06	$R_{DS(on)}$	—	0.028	Ohm
(V_{GS} = 10 Vdc, I_D = 27.5 Adc)	MTM55N10		—	0.04	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 60 Adc)	MTM60N06		—	1.98	
(I_D = 30 Adc, T_J = 100°C)	MTM60N06		—	1.68	
(I_D = 55 Adc)	MTM55N10		—	2.6	
(I_D = 27.5 Adc, T_C = 100°C)	MTM55N10		—	2.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 30 A)	MTM60N06	g_{FS}	10	—	mhos
(V_{DS} = 15 V, I_D = 27.5 A)	MTM55N10		10	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 8	C_{iss}	—	5000	pF
Output Capacitance		C_{oss}	—	2500	
Reverse Transfer Capacitance		C_{rss}	—	1000	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figure 16	$t_{d(on)}$	—	70	ns
Rise Time		t_r	—	350	
Turn-Off Delay Time		$t_{d(off)}$	—	350	
Fall Time		t_f	—	400	
Total Gate Charge	V_{DS} = 0.8 Rated, I_D = Rated, V_{GS} = 10 V See Figure 15	Q_g	105 (Typ)	120	nC
		Q_{gs}	74 (Typ)	—	
		Q_{gd}	31 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	3.5	4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

MTM60N05, MTM60N06

FIGURE 1 — ON-REGION CHARACTERISTICS

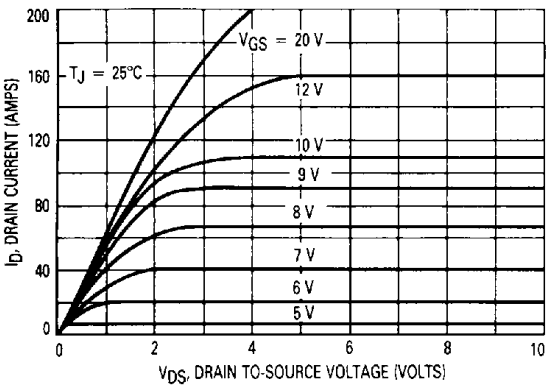


FIGURE 3 — TRANSFER CHARACTERISTICS

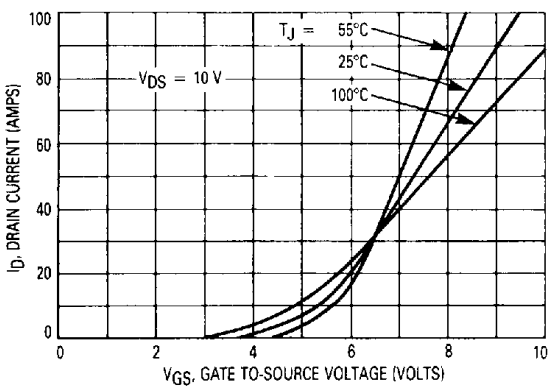
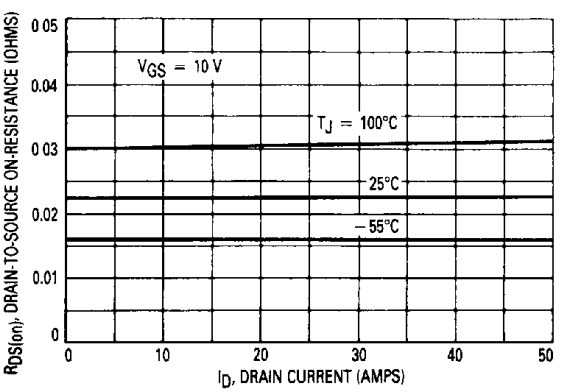


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT



MTM55N08, MTM55N10

FIGURE 2 — ON-REGION CHARACTERISTICS

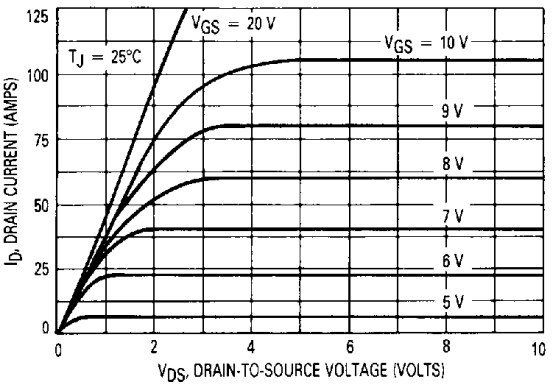


FIGURE 4 — TRANSFER CHARACTERISTICS

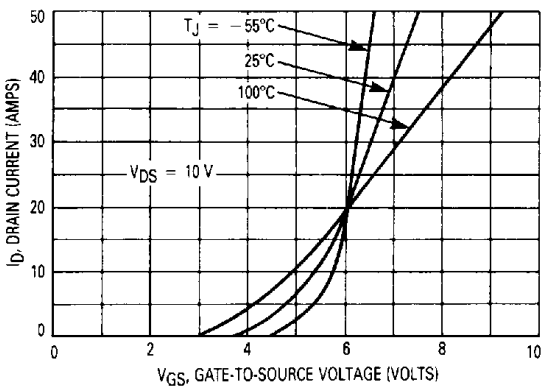


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT

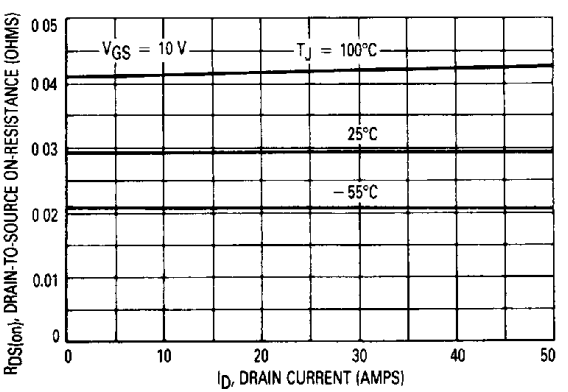


FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

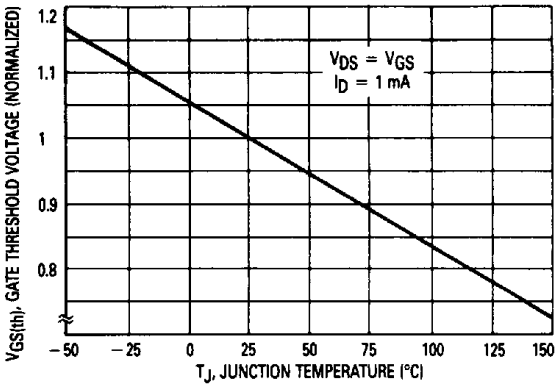


FIGURE 8 — CAPACITANCE VARIATION

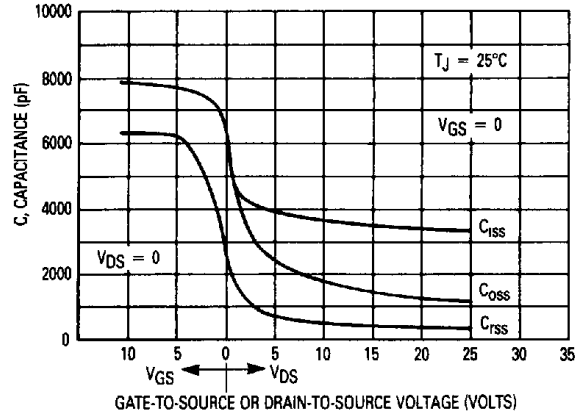


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

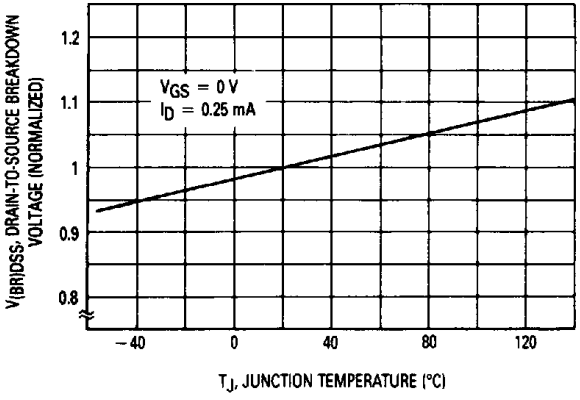


FIGURE 10 — ON-RESISTANCE VARIATION WITH TEMPERATURE

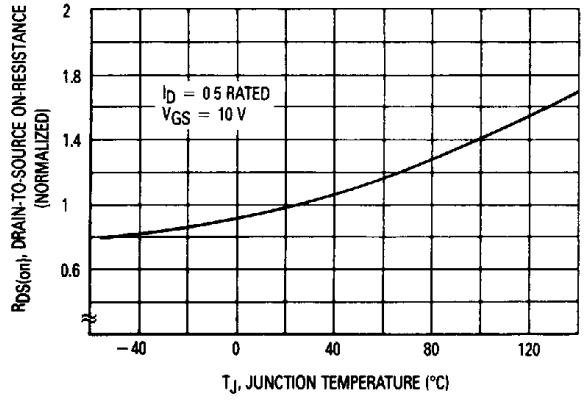
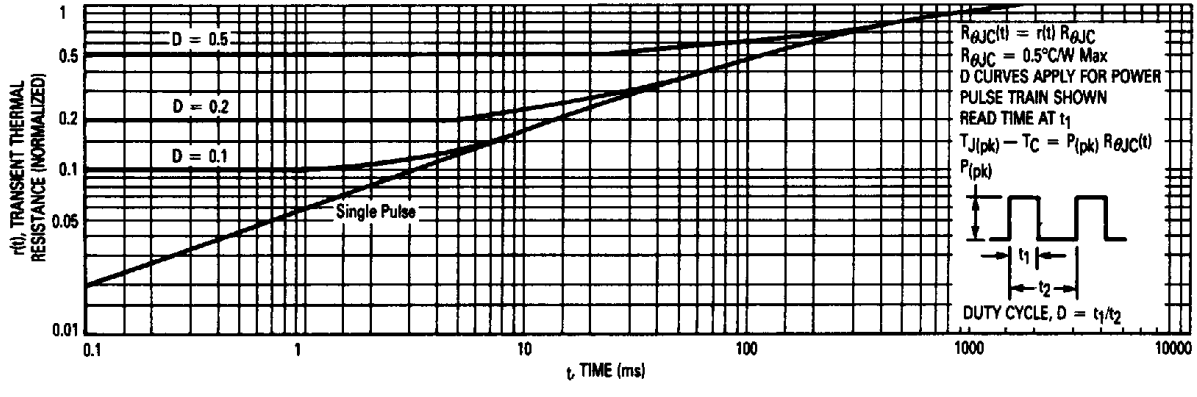


FIGURE 11 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 — MTM60N06

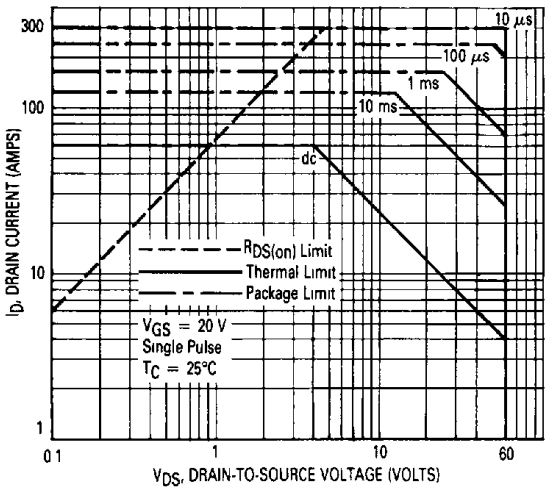
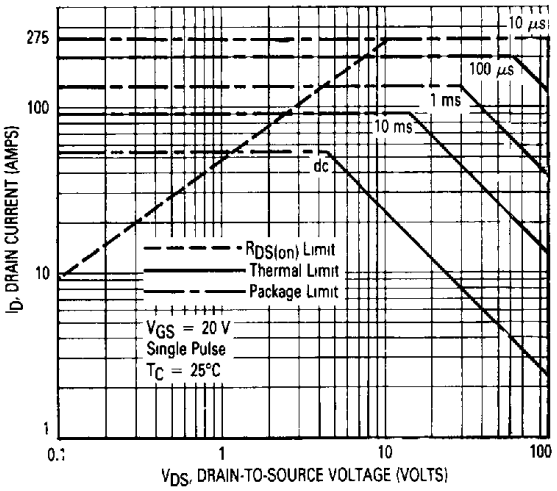


FIGURE 13 — MTM55N10



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

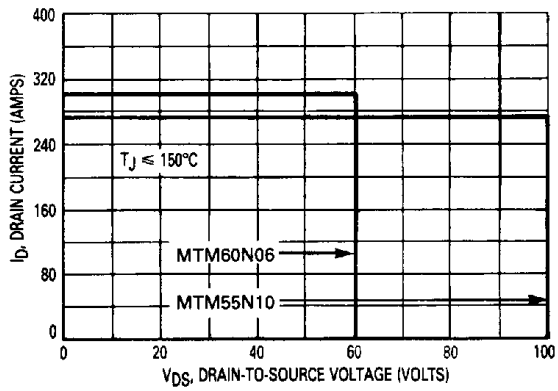


FIGURE 15 — STORED CHARGE versus GATE-TO-SOURCE VOLTAGE

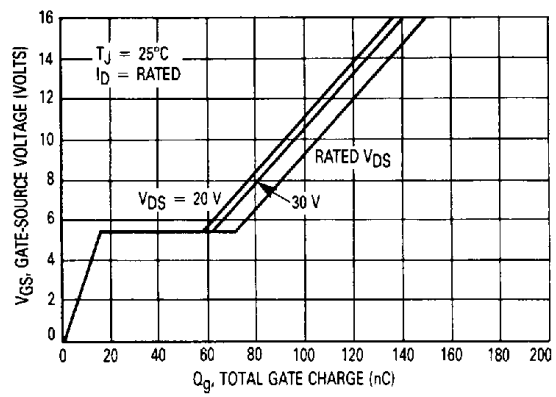


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE