TCP-3068H

Advance Information

6.8 pF Passive Tunable Integrated Circuits (PTIC)

ON Semiconductor®

http://onsemi.com

WLCSP
12 pillar
CASE TBD

QFN
6 pin
CASE TBD

Introduction

ON Semiconductor's PTICs have excellent RF performance and power consumption, making them suitable for any mobile handset or radio application. The fundamental building block of our PTIC product line is a tunable material called ParaScan™, based on Barium Strontium Titanate (BST). PTICs have the ability to change their capacitance from a supplied bias voltage generated by the Control IC. The 6.8 pF PTICs are available as wafer-level chip scale packages (WLCSP) and in QFN packages for easy mounting directly on printed circuit boards.

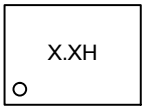
Key Features

- High Tuning Range and Operation up to 20 V
- Usable Frequency Range: from 700 MHz to 2.7 GHz
- High Quality Factor (Q) for Low Loss
- High Power Handling Capability
- Compatible with PTIC Control IC TCC-103
- WLCSP Package: 0.722 x 1.179 x 0.611 mm (12 pillar)
- QFN Package: 1.200 x 1.600 x 0.950 mm
- QFN: MSL−2 Moisture Sensitivity Level (per J−STD−020)
- Pb−Free and RoHS Compliant

Typical Applications

- Multi-band, Multi-standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Tunable RF Filters
- Active Antennas

QFN MARKING DIAGRAM



X.X = 6.8
H = High Tuning

FUNCTIONAL BLOCK DIAGRAM

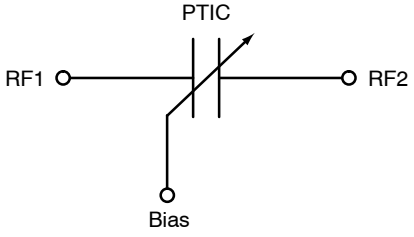


Figure 1. PTIC Functional Block Diagram

ORDERING INFORMATION

Device	Package	Shipping
TCP−3068H−DT	WLCSP (Pb−Free)	4000 Units / 7" Reel
TCP−3068H−QT	QFN (Pb−Free)	8000 Units / 13" Reel

For detailed ordering information, including part number definition and capacitance (pF) see the package dimensions section on page 7 of this datasheet.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TYPICAL SPECIFICATIONS

Representative Performance Data at 25°C

Table 1. PERFORMANCE DATA

Parameter	Min	Typ	Max	Units
Operating Bias Voltage	2.0		20	V
Capacitance (V_{bias} = 2 V)	6.12	6.80	7.48	pF
Capacitance (V_{bias} = 20 V)	1.70	1.79	1.88	pF
Tuning Range (2 V - 20 V)	3.40	3.80	4.20	
Tuning Range (20 V - 2 V)		3.60		
Leakage Current (WLCSP)			2.0	μA
Operating Frequency	700		2700	MHz
Quality Factor @ 700 MHz, 10 V		100		
Quality Factor @ 2.4 GHz, 10 V		75		
IP3 (V_{bias} = 2 V) [1,3]		70		dBm
IP3 (V_{bias} = 20 V) [1,3]		85		dBm
2nd Harmonic (V_{bias} = 2 V) [2,3]		-70		dBm
2nd Harmonic (V_{bias} = 20 V) [2,3]		-80		dBm
3rd Harmonic (V_{bias} = 2 V) [2,3]		-40		dBm
3rd Harmonic (V_{bias} = 20 V) [2,3]		-70		dBm
Transition Time (Cmin → Cmax) [4]		80		μs
Transition Time (Cmax → Cmin) [4]		70		μs

1. f_1 = 850 MHz, f_2 = 860 MHz, Pin 25 dBm/Tone
2. 850 MHz, Pin +34 dBm
3. IP3 and Harmonics are measured in the shunt configuration in a 50 Ω environment
4. RF_{IN} and RF_{OUT} are both connected to DC ground

Representative performance data at 25°C for 6.8 pF WLCSP Package

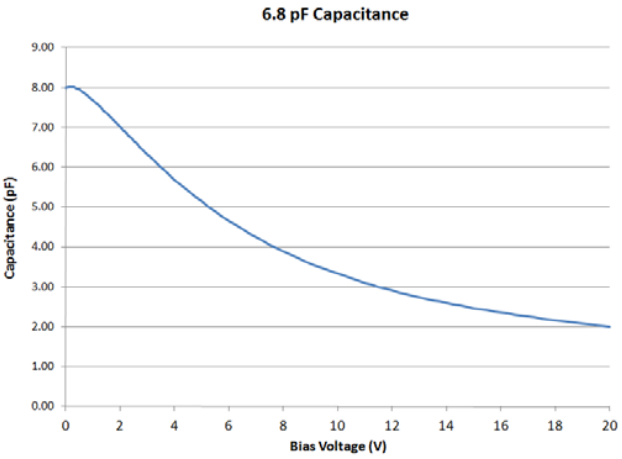


Figure 2. Capacitance

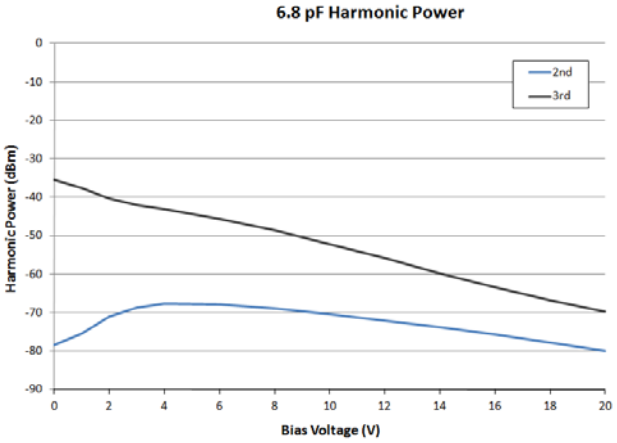


Figure 3. Harmonic Power*

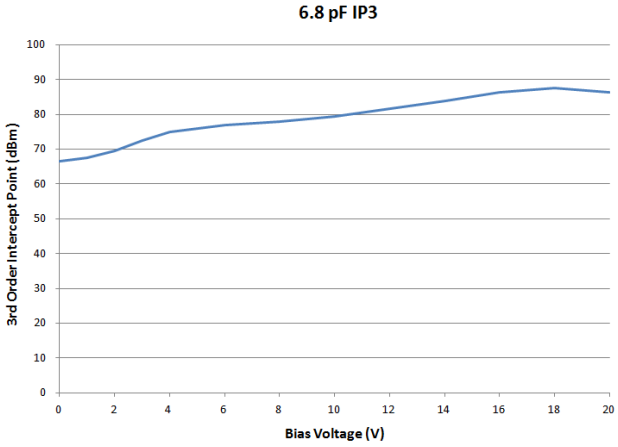


Figure 4. IP3*

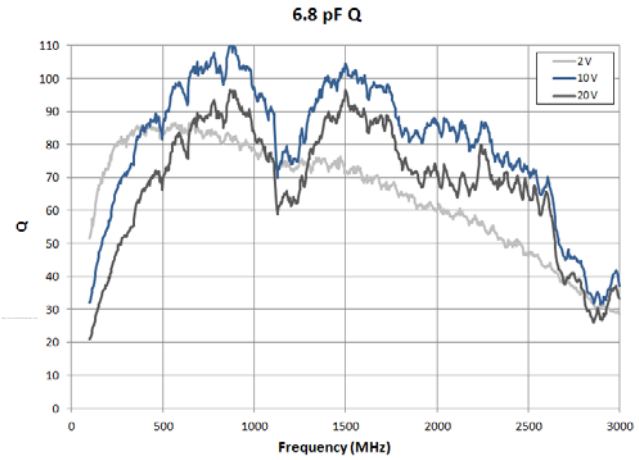


Figure 5. Q*

*The data shown is based on the TCP−3068N device performance, for reference only. The TCP−3068H performance data will be available in the Production Datasheet.

Table 2. ABSOLUTE MAXIMUM RATINGS

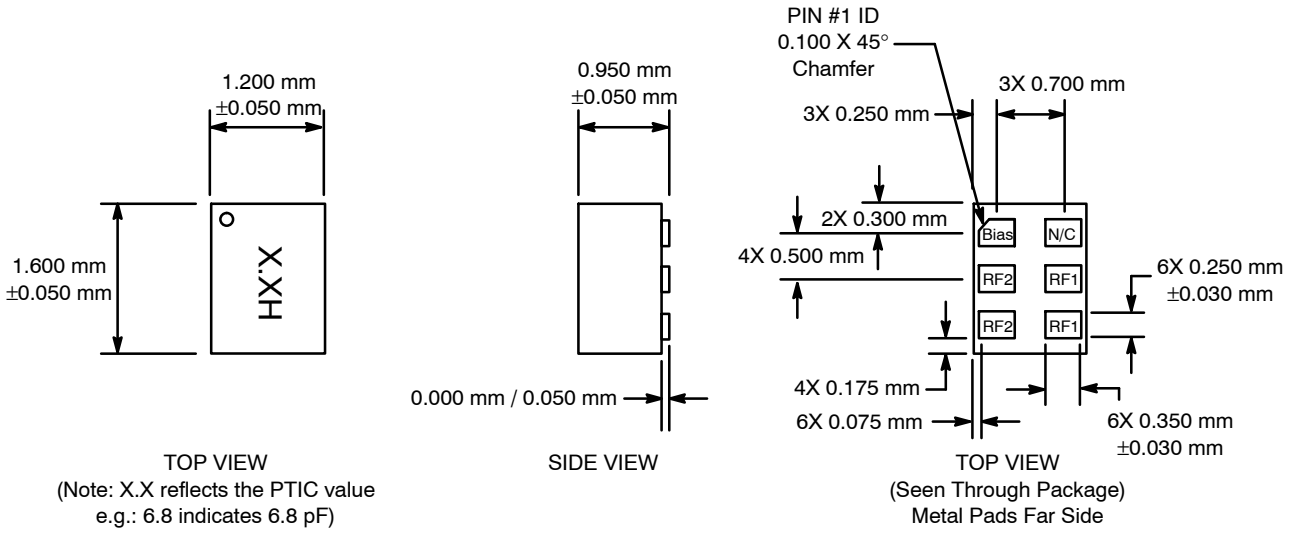
Parameter	Rating	Units
Input Power	+40	dBm
Bias Voltage	+25 (Note 5)	V
Operating Temperature Range	−30 to +85	°C
Storage Temperature Range	−55 to +125	°C
ESD − Human Body Model	Class 1A JEDEC HBM Standard (Note 6)	

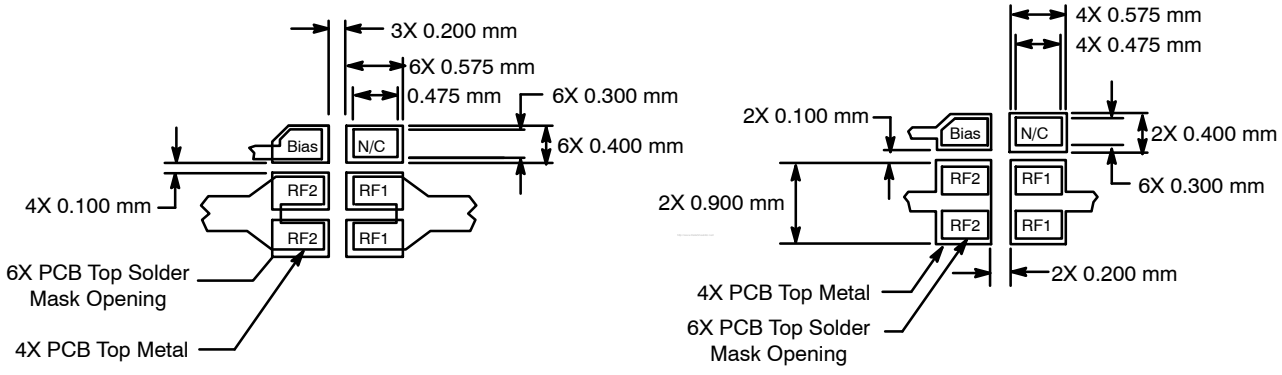
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. WLCSP: Recommended Bias Voltage not to exceed 20 V
6. Class 1A defined as passing 250 V, but may fail after exposure to 500 V ESD pulse

PACKAGE INFORMATION

QFN Package Layout and Dimensional Information

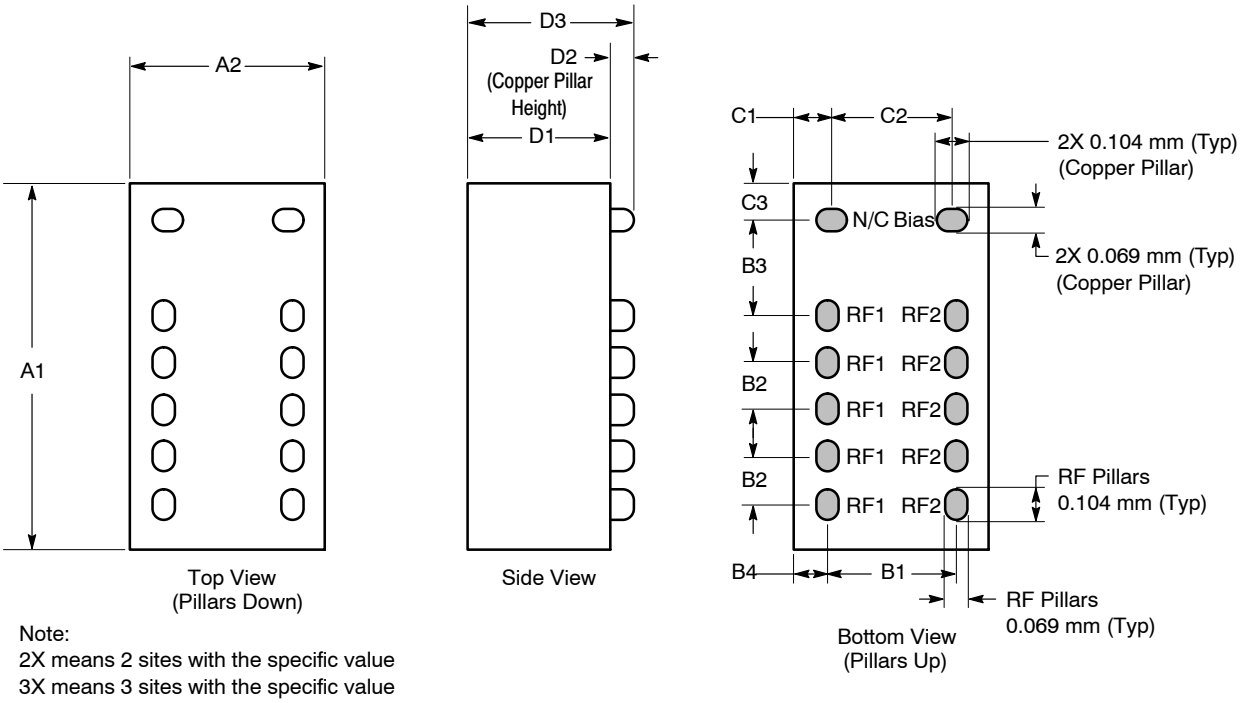




Note:
2X means 2 sites with the specific value
3X means 3 sites with the specific value
4X means 4 sites with the specific value
0.9 mm pad layout is standard for all products. Shorter pad layouts can be considered for smaller products.

Figure 6. QFN Pin Markers and Dimensions

Wafer Level Chip Scale Package (WLCSP) Layout and Dimensional Information



Note:
2X means 2 sites with the specific value
3X means 3 sites with the specific value
4X means 4 sites with the specific value

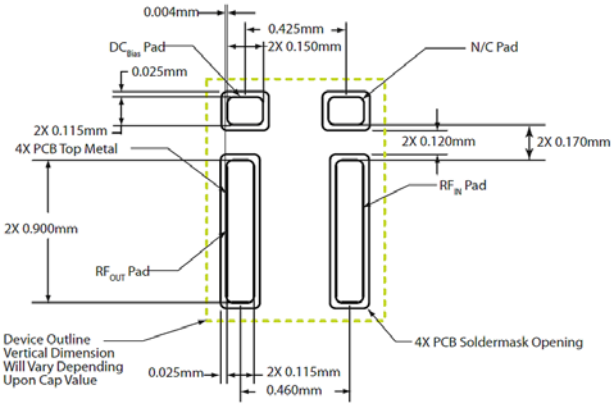
Figure 7. WLCSP Pin Markers and Dimensions

Table 3. PACKAGE DIMENSIONS
(All dimensions are in milimeters)

WLCSP *	DIM	Nominal	Max	Device
8P	A1	0.879		1.2, 2.7 pF
10P	A1	1.029		3.3, 3.9 pF
12P	A1	1.179		4.7, 5.6, 6.8, 8.2 pF
14P	A1	1.329		
ALL	A2	0.722		
ALL	B1	0.460		
ALL	B2	0.150		
ALL	B3	0.300		
ALL	B4	0.130		
ALL	C1	0.148		
ALL	C2	0.425		
ALL	C3	0.130		
ALL	D1	0.530		
ALL	D2	0.081		

*Total number of pillars

Top View Recommended PCB Pad Layout (Metal Defined Pad)



Note:
0.9 mm pad layout is standard for all products. Shorter pad layouts can be considered for smaller products.

Figure 8. Recommended Pad Layout

ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE

The following assembly considerations should be observed:

Cleanliness

These chips should be handled in a clean environment.

Electro-static Sensitivity

ON Semiconductor's PTICs are ESD Class 1A sensitive. The proper ESD handling procedures should be used.

Mounting

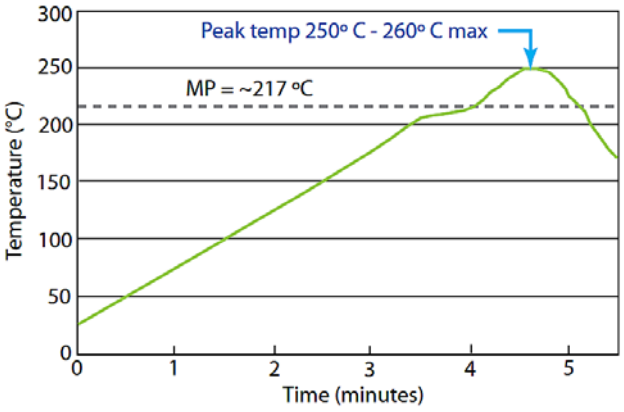
The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through copper pillar posts (53 μm nominal height) topped with lead-free SAC351 solder caps (28 μm nominal height). The PTIC die is RoHS-compliant and compatible with lead-free soldering profile.

Post-reflow Cleaning

Use of ultrasonic cleaning is not recommended for pillared devices as it may lead to premature fatigue failure of the pillars.

Molding

The PTIC die is compatible for over-molding or under-fill.



This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density.
Not to exceed 260° C for 5 seconds.

Figure 9. Reflow Profile

ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.

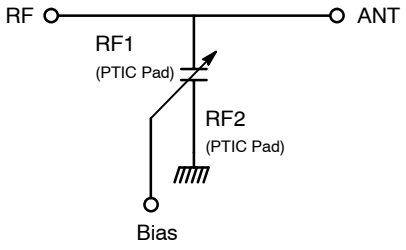


Figure 10. PTIC Orientation Functional Block Diagram

PART NUMBER DEFINITION

Example: TCP−3068H−DT

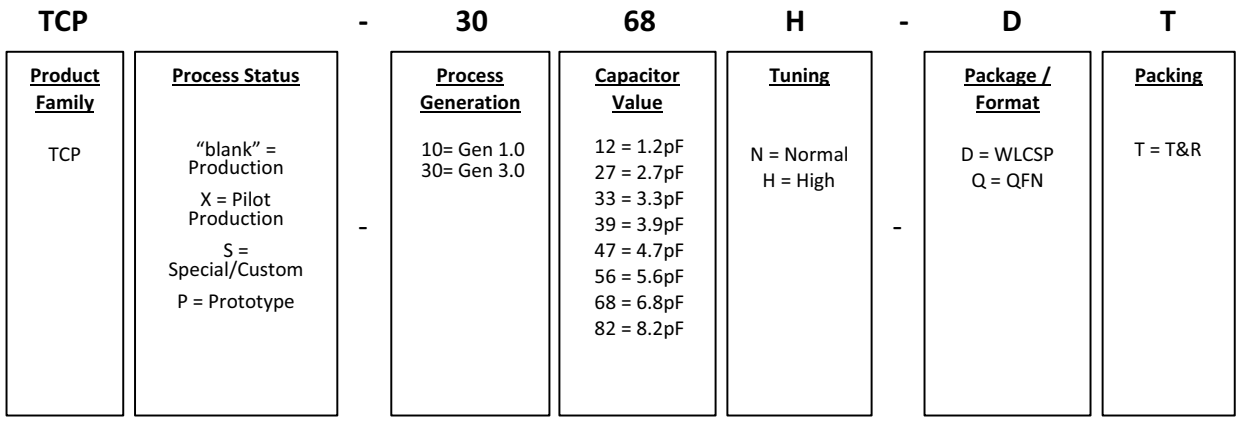
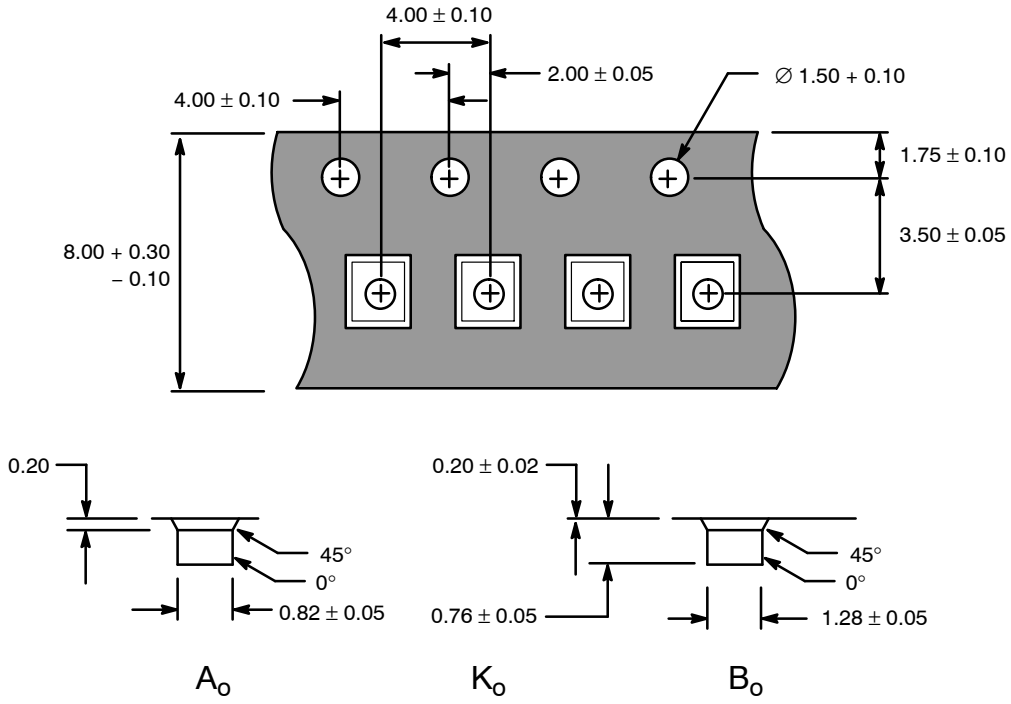


Table 4. PART NUMBERS

Part Number	Capacitance		Package*
	2 V	20 V	
TCP−3068H-DT	6.80	1.79	12-Pillar WLCSP
TCP−3068H-QT	6.80	1.79	6-Pin QFN

*See PTIC package dimensions on page 5

TAPE & REEL DIMENSIONS



Note: The reel size is 7”
Pocket may have a hole 0.2 mm to 0.4 mm ± 0.05 mm

Figure 11. 12 Pillar WLCSP Carrier Tape Drawing

TAPE & REEL DIMENSIONS (Cont'd)

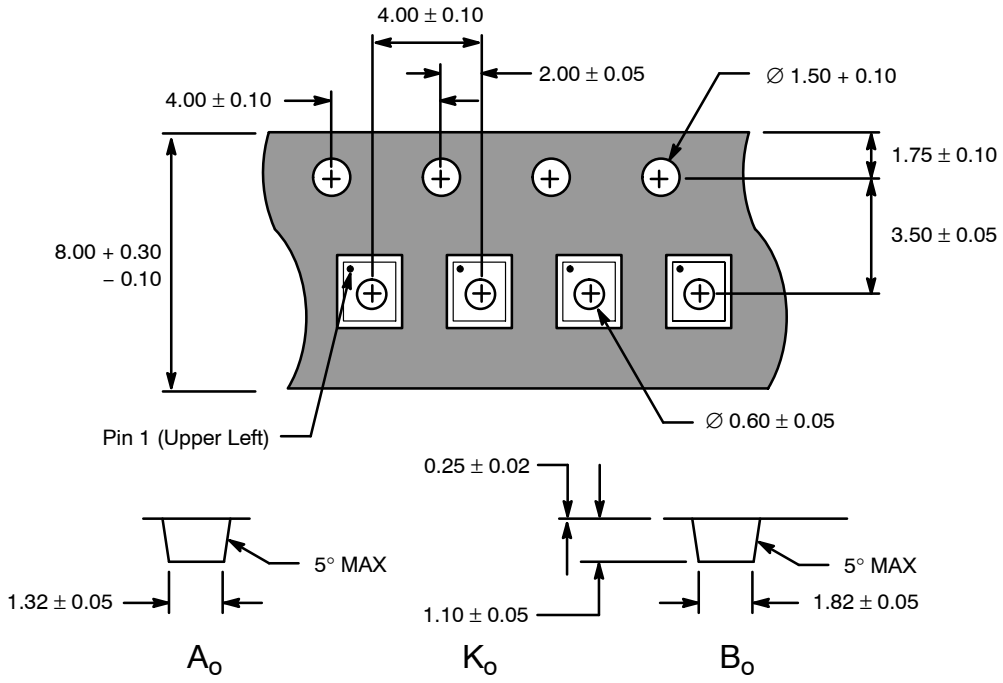


Figure 12. QFN Carrier Tape Drawing

POCKET DIMENSION

Pocket Dimension (mm)				Unit Dimension (mm)			
	Spec	Max	Min		Spec	Max	Min
Ao	1.32 ± 0.05	1.37	1.27	A	1.2 ± 0.05	1.25	1.15
Bo	1.82 ± 0.05	1.87	1.77	B	1.6 ± 0.05	1.65	1.55
Ko	1.1 ± 0.05	1.15	1.05	K	0.95 ± 0.05	1.00	0.90

NOTE: The reel size is 13"

ParaScan is a trademark of Paratek Microwave, Inc.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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