

# DATA SHEET

## **GTL2001**

22-bit GTL processor voltage clamp

Product specification

2000 Sep 11

## 22-bit GTL processor voltage clamp

## GTL2001

## FEATURES

- Direct interface with TTL level
- 6.5Ω ON-state connection between port  $S_n$  and  $D_n$

## DESCRIPTION

The GTL2001 provides twenty-two bits of high-speed voltage clamps. The low ON-state resistance of the clamp allows connections to be made with minimal propagation delay.

The device is organized as one 22-bit voltage clamp. When S or D is low the clamp is in the ON-state and a low resistance connection exists between the S and D ports. When S port and D port are high, the clamp is in the OFF-state and a very high impedance exists between the S and D ports. When the D port is high, the voltage on the S port is clamped to the applied reference voltage on the  $G_{REF}$  port.

## FUNCTION TABLE

$G_{REF}$	$D_{REF}$	$S_{REF}^4$	Switch	Driven Input	Output of Driven Input
H	H	0 V	off	X	X
H	H	$V_{TT}$	on	H	$V_{TT}^1$
H	H	$V_{TT}$	nearly off	$V_{TT}$	$H^2$
L	L	$V_{TT}$	on	L	$L^3$
L	L	$0 - V_{TT}$	off	X	X

H = High voltage level

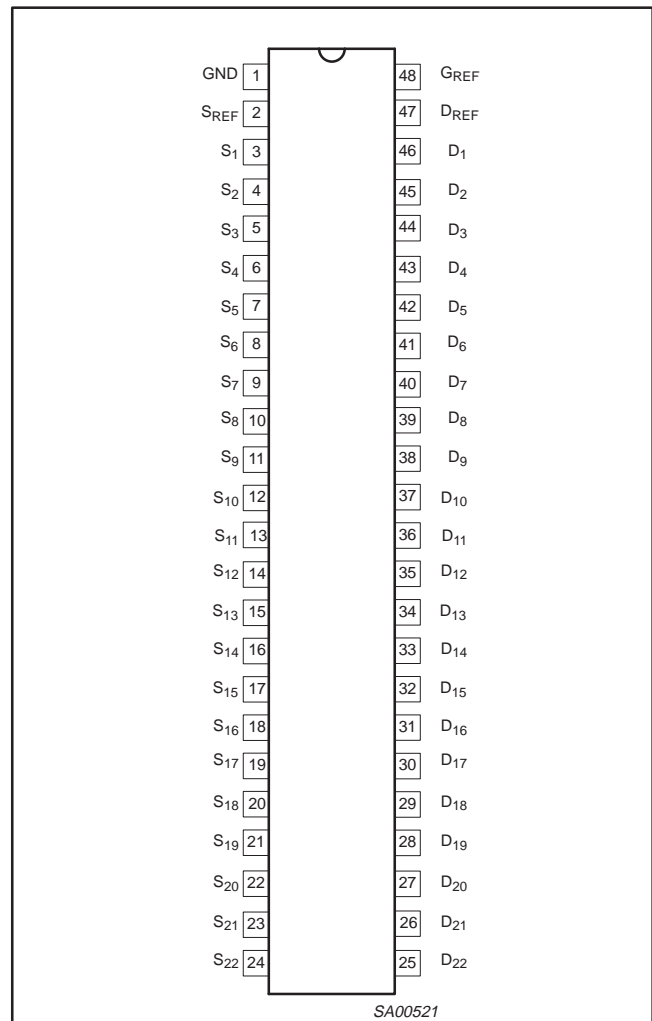
L = Low voltage level

X = Don't Care

## NOTES:

1. The output is not pulled up or pulled down.
2. The output is pulled up to  $V_{CC}$  through an external resistor.
3. The driven output can be  $S_n$  or  $D_n$ ; the output of driven input follows the input low.
4.  $G_{REF}$  must be at least 1.5 V higher than  $S_{REF}$  for proper switch operation.

## PIN CONFIGURATION



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
		$T_{amb} = 25^{\circ}\text{C}; GND = 0V$			
$t_{PLH}$	Propagation delay $S_n$ to $D_n$	$V_{DD1} = 3.3 V; V_{DD2} = 2.5 V;$ $V_{REF} = 1.5 V; \text{unloaded}$		1.5	ns
$C_{OFF}$	Channel capacitance (OFF-state)	$V_S = 1.5 V$		7.5	pF

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic SSOP Type II	$0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	GTL2001 DL	SOT370-1

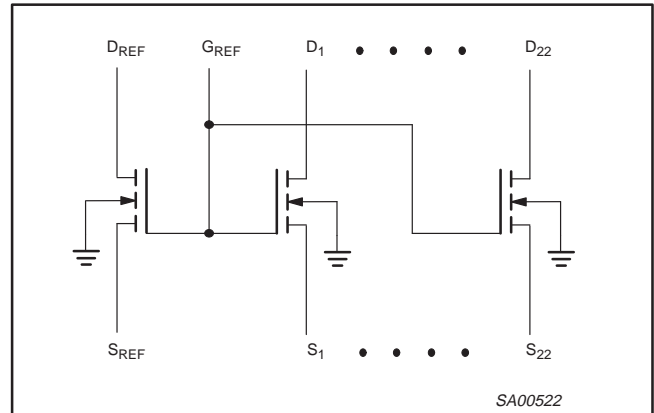
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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	GND	Ground (0V)
2	S <sub>REF</sub>	Source of reference transistor
3 – 24	S <sub>n</sub>	Port S <sub>1</sub> to Port S <sub>22</sub>
25 – 46	D <sub>n</sub>	Port D <sub>1</sub> to Port D <sub>22</sub>
47	D <sub>REF</sub>	Drain of reference transistor
48	G <sub>REF</sub>	Gate of reference transistor

## CLAMP SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>S_REF</sub>	DC source reference voltage		-0.5 to +7.0	V
V <sub>D_REF</sub>	DC drain reference voltage		-0.5 to +7.0	V
V <sub>G_REF</sub>	DC gate reference voltage		-0.5 to +7.0	V
V <sub>S<sub>n</sub></sub>	DC voltage Port S <sub>n</sub>		-0.5 to +7.0	V
V <sub>D<sub>n</sub></sub>	DC voltage Port D <sub>n</sub>		-0.5 to +7.0	V
I <sub>REFK</sub>	DC reference diode current	V <sub>I</sub> < 0	-50	mA
I <sub>SK</sub>	DC diode current Port S <sub>n</sub>	V <sub>I</sub> < 0	-50	mA
I <sub>DK</sub>	DC diode current Port D <sub>n</sub>	V <sub>I</sub> < 0	-50	mA
I <sub>MAX</sub>	DC clamp current per channel	Channel in ON-state	±35	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			Min	Max	
V <sub>S_REF</sub>	DC source reference voltage		1.0	4.4	V
V <sub>D_REF</sub>	DC drain reference voltage		V <sub>S_REF</sub> + 0.6	5	V
V <sub>G_REF</sub>	DC gate reference voltage		V <sub>S_REF</sub> + 0.6	5	V
V <sub>S<sub>n</sub></sub>	DC voltage Port S <sub>n</sub> (OFF-state)		V <sub>S_REF</sub>	5	V
V <sub>S<sub>n</sub></sub>	DC voltage Port S <sub>n</sub> (ON-state)		0	0.2	V
V <sub>D<sub>n</sub></sub>	DC voltage Port D <sub>n</sub> (OFF-state)		V <sub>S_REF</sub>	5	V
V <sub>D<sub>n</sub></sub>	DC voltage Port D <sub>n</sub> (ON-state)		0	0.4	V
I <sub>S</sub>	Switch input leakage current (OFF-state) for S <sub>n</sub> and D <sub>n</sub> I/O	V <sub>S</sub> , V <sub>D</sub> = 5 V		15	μA
I <sub>I</sub>	G <sub>REF</sub> input leakage current	V <sub>G</sub> = 5 V		2.5	μA
T <sub>amb</sub>	Operating ambient temperature range	In free air	0	+85	°C

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## DC CHARACTERISTICS for $V_{DD1} = 3.0$ to $3.6$ V; $V_{DD2} = 2.36$ to $2.64$ V; $V_{REF} = 1.365$ to $1.635$ V range

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V). Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = 0^{\circ}\text{C to } +85^{\circ}\text{C}$			
			MIN	TYP <sup>1</sup>	MAX	
$V_{OL}$	LOW level output voltage	$V_S = 0.175$ V; $I_{CLAMP} = 15.2$ mA		260	350	mV

**NOTE:**

1. All typical values are measured at  $V_{DD1} = 3.3$  V,  $V_{DD2} = 2.5$  V,  $V_{REF} = 1.5$  V and  $T_{amb} = 25^{\circ}\text{C}$

## AC CHARACTERISTICS for $V_{DD1} = 3.0$ to $3.6$ V; $V_{DD2} = 2.36$ to $2.64$ V; $V_{REF} = 1.365$ to $1.635$ V range

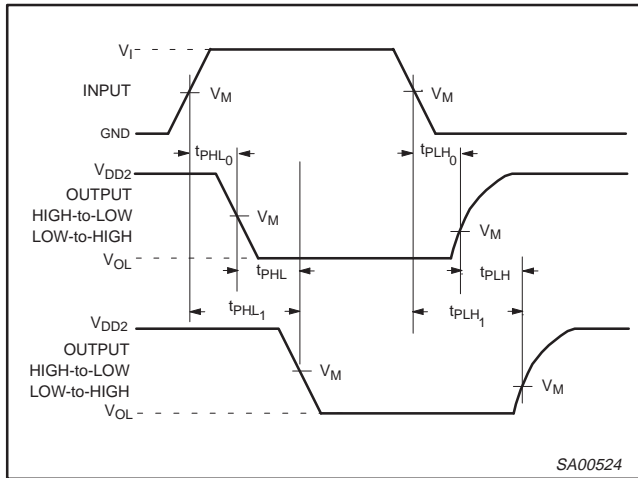
$GND = 0V$ ;  $t_r = t_f \leq 3.0$  ns. Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = 0^{\circ}\text{C to } +85^{\circ}\text{C}$			
			MIN	TYP <sup>1</sup>	MAX	
$t_{PLH}^2$	Propagation delay Sn to Dn; Dn to Sn		0.5	1.5	5.5	ns

**NOTES:**

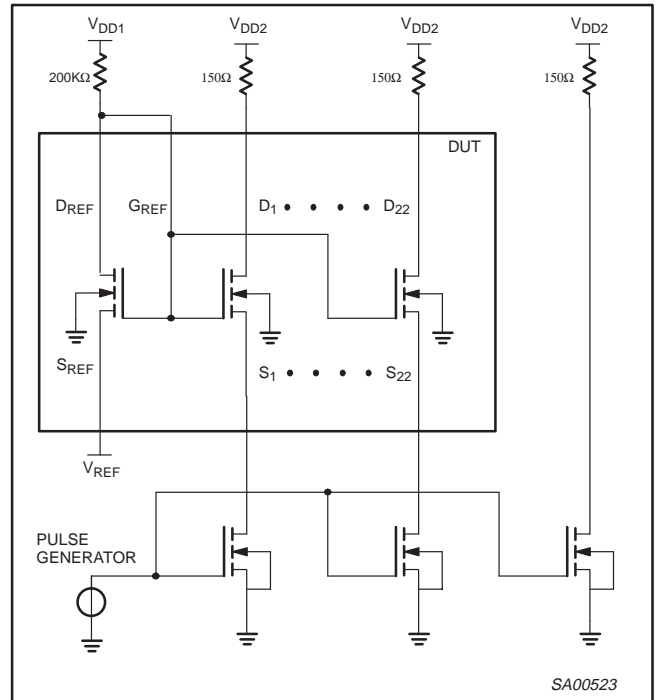
1. All typical values are measured at  $V_{DD1} = 3.3$  V,  $V_{DD2} = 2.5$  V,  $V_{REF} = 1.5$  V and  $T_{amb} = 25^{\circ}\text{C}$ .
2. Propagation delay guaranteed by characterization.
3.  $C_{ON,MAX}$  of 30 pF and a  $C_{OFF,MAX}$  of 15 pF is guaranteed by design.

### AC WAVEFORMS



Waveform 1. The Input ( $S_n$ ) to Output ( $D_n$ ) Propagation Delays

### TEST CIRCUIT



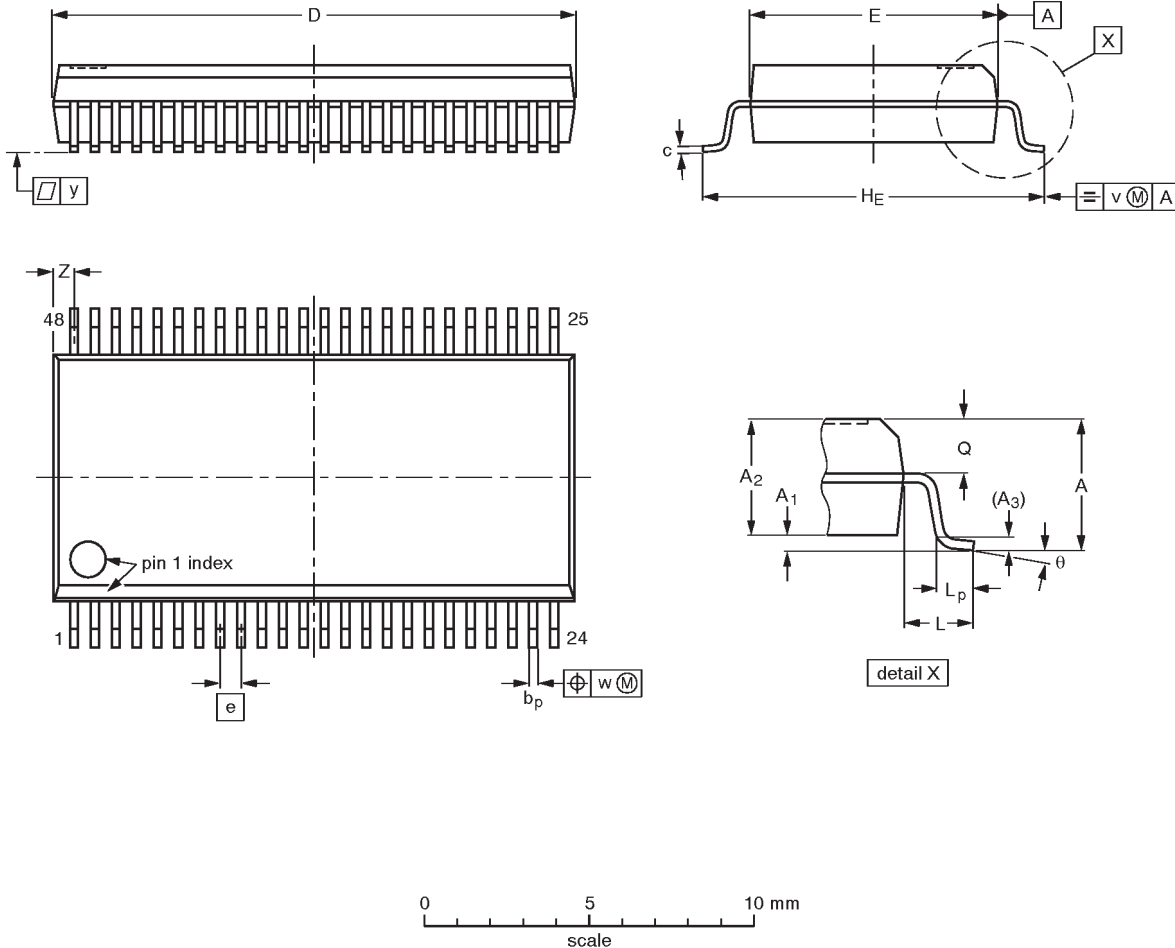
Waveform 2. Load circuit

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**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm**

**SOT370-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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