TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

33,554,432-WORD BY 18-BIT (64M Bytes) Direct Rambus DRAM MODULE

DESCRIPTION

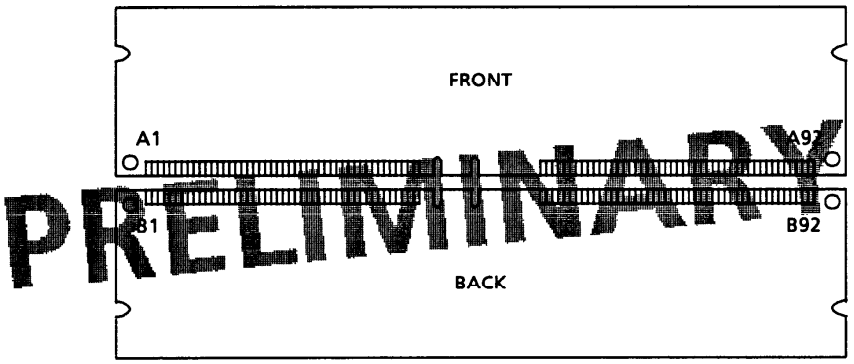
The THMR1E4 is a 33,554,432-word by 18-bit direct rambus dynamic RAM module consisting of 4 TC59RM718MB Direct Rambus DRAMs on a printed circuit board.

FEATURES

	-6	-7	-8
Organization	32M-word×18 bit	32M-word×18 bit	32M-word×18 bit
I/O Frequency	600MHz	711MHz	800MHz
t_{RAC} (Row Access time)	53ns (16cycles)	45ns (16cycles)	40ns (16cycles)
Part Designator	144M (×18) -4CSP	144M (×18) -4CSP	144M (×18) -4CSP

- Single power supply of 2.5V (±5%)
- Low power dissipation (max)
  - Operating T.B.D.
  - Standby T.B.D.
- 64MB Direct RDRAM storage
- Each RDRAM has 32 banks for 128 banks total on module
- Separate Row and Column buses for higher efficiency
- Package: 184pin DIMM
- Gold contacts
- Serial Presence Detect suport

PIN ASSIGNMENT (TOP VIEW)



A1	Gnd	B1	Gnd	A24	LCOL0	B24	LDQB0	A47	NC	B47	NC	A70	Gnd	B70	Gnd
A2	LDQA8	B2	LDQA7	A25	Gnd	B25	Gnd	A48	NC	B48	NC	A71	RCOL2	B71	RCOL1
A3	Gnd	B3	Gnd	A26	LDQB1	B26	LDQB2	A49	NC	B49	NC	A72	Gnd	B72	Gnd
A4	LDQA6	B4	LDQA5	A27	Gnd	B27	Gnd	A50	NC	B50	NC	A73	RCOL4	B73	RCOL3
A5	Gnd	B5	Gnd	A28	LDQB3	B28	LDQB4	A51	Vref	B51	Vref	A74	Gnd	B74	Gnd
A6	LDQA4	B6	LDQA3	A29	Gnd	B29	Gnd	A52	Gnd	B52	Gnd	A75	RROW1	B75	RROW0
A7	Gnd	B7	Gnd	A30	LDQB5	B30	LDQB6	A53	SCL	B53	SA0	A76	Gnd	B76	Gnd
A8	LDQA2	B8	LDQA1	A31	Gnd	B31	Gnd	A54	Vdd	B54	Vdd	A77	NC	B77	RROW2
A9	Gnd	B9	Gnd	A32	LDQB7	B32	LDQB8	A55	SDA	B55	SA1	A78	Gnd	B78	Gnd
A10	LDQA0	B10	LCFM	A33	Gnd	B33	Gnd	A56	SVdd	B56	SVdd	A79	RCTM	B79	NC
A11	Gnd	B11	Gnd	A34	LSCK	B34	LCMD	A57	SWP	B57	SA2	A80	Gnd	B80	Gnd
A12	LCTMN	B12	LCFMN	A35	Vcmos	B35	Vcmos	A58	Vdd	B58	Vdd	A81	RCTMN	B81	RCFMN
A13	Gnd	B13	Gnd	A36	SOUT	B36	SIN	A59	RSCK	B59	RCMD	A82	Gnd	B82	Gnd
A14	LCTM	B14	NC	A37	Vcmos	B37	Vcmos	A60	Gnd	B60	Gnd	A83	RDQA0	B83	RCFM
A15	Gnd	B15	Gnd	A38	NC	B38	NC	A61	RDQB7	B61	RDQB8	A84	Gnd	B84	Gnd
A16	NC	B16	LROW2	A39	Gnd	B39	Gnd	A62	Gnd	B62	Gnd	A85	RDQA2	B85	RDQA1
A17	Gnd	B17	Gnd	A40	NC	B40	NC	A63	RDQB5	B63	RDQB6	A86	Gnd	B86	Gnd
A18	LROW1	B18	LROW0	A41	Vdd	B41	Vdd	A64	Gnd	B64	Gnd	A87	RDQA4	B87	RDQA3
A19	Gnd	B19	Gnd	A42	Vdd	B42	Vdd	A65	RDQB3	B65	RDQB4	A88	Gnd	B88	Gnd
A20	LCOL4	B20	LCOL3	A43	NC	B43	NC	A66	Gnd	B66	Gnd	A89	RDQA6	B89	RDQA5
A21	Gnd	B21	Gnd	A44	NC	B44	NC	A67	RDQB1	B67	RDQB2	A90	Gnd	B90	Gnd
A22	LCOL2	B22	LCOL1	A45	NC	B45	NC	A68	Gnd	B68	Gnd	A91	RDQA8	B91	RDQA7
A23	Gnd	B23	Gnd	A46	NC	B46	NC	A69	RCOL0	B69	RDQB0	A92	Gnd	B92	Gnd

961001EBA1

PIN NAMES

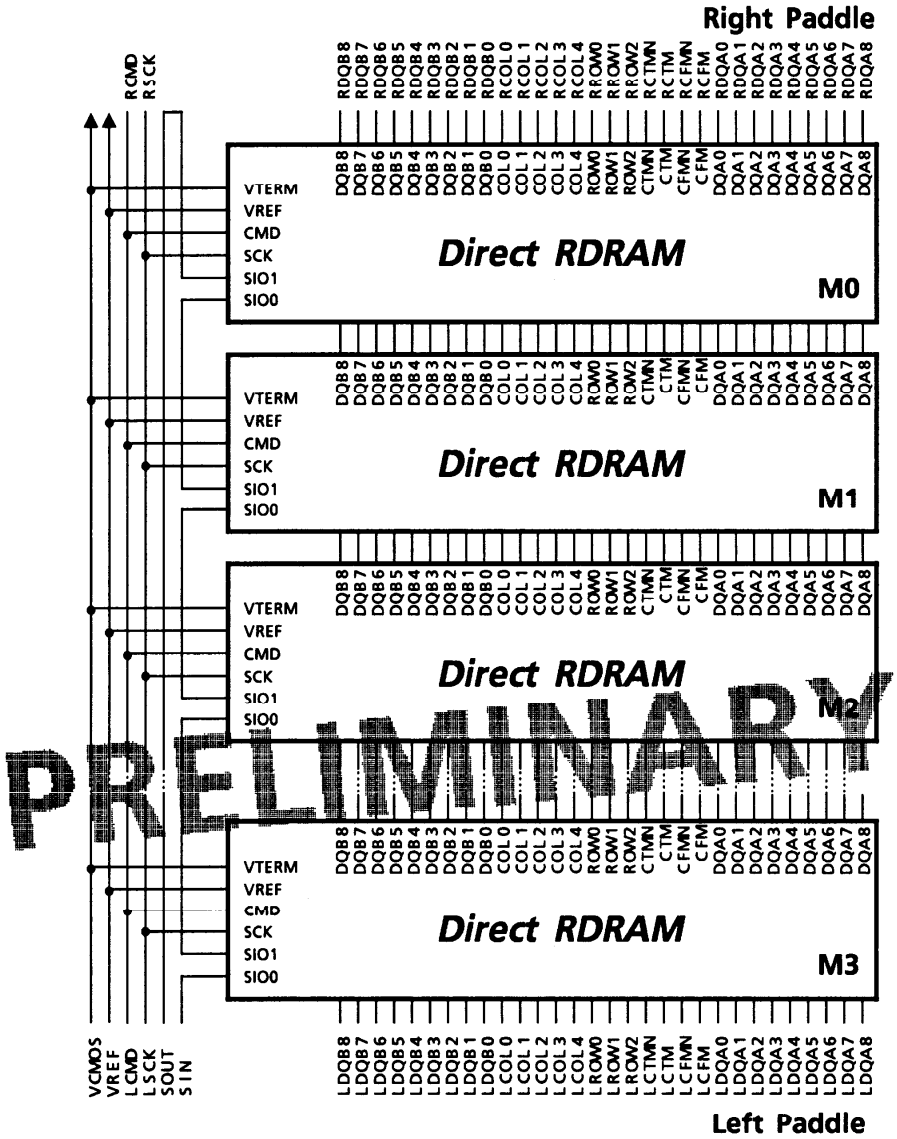
Signal	I/O	Type	Description	Pins
SIN	I/O	CMOS	Serial I/O. Pin for reading from and writing to the control registers.	B36
SOUT	I/O	CMOS	Serial I/O. Pin for reading from and writing to the control registers.	A36
VDD			Supply voltage for the RDRAM core and interface logic.	A41, B41, A42, B42,A54, B54, A58, B58
GND			Ground reference for RDRAM core and interface.	A1, B1, A3, B3, A5, B5, A7, B7, A9, B9, A11, B11, A13, B13, A15, B15, A17, B17, A19 B19, A21, B21, A23, B23, A25 B25, A27, B27, A29, B29, A31 B31, A33, B33, A39, B39, A52, B52, A60, B60,A62, B62, A64, B64, A66, B66, A68, B68 A70, B70, A72, B72, A74, B74 A76, B76, A77, A78, B78, A80, B80, A82, B82, A84, B84 A86, B86, A88, B88, A90, B90 A92, B92
LDQA8 to 0	I/O	RSL	Data bus A. A 9-pin bus carrying a byte of read or write data between the Channel and the RDRAM.	A2, B2, A4, B4, A6, B6, A8, B8, A10
LCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.	B10
LCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.	B12
	VREF		Logic threshold reference voltage for RSL signals.	A51, B51
LCTMN	I	RSL	Clock to master. Interface clock used for taransmitting RSL signals to the Channel. Negative polarity.	A12
LCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positibe polarity.	A14
LROW2 to 0	I	RSL	Row bus. 3-pin bus containing control and address information for row accesse.	B16, A18, B18
LCOL4 to 0	I	RSL	Column bus. 5-pin bus containing control and address information for column accesses.	A20, B20, A22, B22, A24
LDQB8 to 0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.	B32, A32, B30, A30, B28, A28, B26, A26, B24
LCMD	I	CMOS	Serial Command Pin. Pin used to read from and write to the control registers. Also used for power management.	B34
LSCK	I	CMOS	Clock input. Pin used to read from and write to the control registers.	A34
RDQA8 to 0	I/O	RSL	Data bus A. A 9-pin bus carrying a byte of read or write data between the Channel and the RDRAM.	A91, B91, A89, B89, A87, B87, A85, B85, A83
RCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.	B83
RCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.	B81
RCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.	A79
RROW2 to 0	I	RSL	Row bus. 3-pin bus containing control and address information for row accesses.	B77, A75, B75
RCOL4 to 0	I	RSL	Column bus. 5-pin bus containing control and address information for column accesses.	A73, B73, A71, B71, A69
RDQB8 to 0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.	B61, A61, B63, A63, B65, A65 B67, A67, B69
RCMD	I	CMOS	Serial Command Input. Pin used to read from and write to the control registers. Also used for power manegement.	B59
RSCK	I	CMOS	Clock input. Pin used to read from and write to the control registers.	A59
SCL	I	CMOS	Serial Presence Detect Clock.	A53
SDA	I/O	CMOS	Serial Presence Detect Data (Open Collector I/O).	A55
SA0	I	CMOS	Serial Presence Detect Address 0.	B53
SA1	I	CMOS	Serial Presence Detect Address 1.	B55
SA2	I	CMOS	Serial Presence Detect Adderss 2.	B57
SWP	I	CMOS		A57
VCMOS			Termination Voltage.	A37, B37, A35, B35
SVDD			Supply voltage for the E^2PROM (SPD).	A56, B56
N.C.				B14, A16, A38, B38, A40, B40 A43, B43, A44, B44, A45, B45 A46, B46, A47, B47, A48, B48 A49, B49, A50, B50, B79,

SERIAL PRESENCE DETECT (Protocol Ver.1 (5tTR))

Byte Number	Function	THMR1E4-6		THMR1E4-7		THMR1E4-8	
		32Mx18 (64MB + ECC), 600MHz-53ns		32Mx18 (64MB + ECC), 711MHz-45ns		32Mx18 (64MB + ECC), 800MHz-40ns	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
0	SPD revision level	2	02h	2	02h	2	02h
1	Total number of bytes in the SPD	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Device type	DRDRAM	01h	DRDRAM	01h	DRDRAM	01h
3	Module type	RIMM	01h	RIMM	01h	RIMM	01h
4	Row address bit, Column address bit	9.6	96h	9.6	96h	9.6	96h
5	Bank address bits and byte	32s	C5h	32s	C5h	32s	C5h
6	Refresh bank bit	5	05h	5	05h	5	05h
7	tREF-Refresh interval	32	20h	32	20h	32	20h
8	Protocol version	2	02h	2	02h	2	02h
9	Miscellaneous device configuration field (Low Power/no-Low Power)	1tSCK	05h	1tSCK	05h	1tSCK	05h
10	tRP-R, Min	8Cycle	08h	8Cycle	08h	8Cycle	08h
11	tRAS-R, Min	20Cycle	14h	20Cycle	14h	20Cycle	14h
12	tRCD-R, Min	8Cycle	08h	8Cycle	08h	8Cycle	08h
13	tRR-R, Min	8Cycle	08h	8Cycle	08h	8Cycle	08h
14	tPP-R, Min	8Cycle	08h	8Cycle	08h	8Cycle	08h
15	Min tCYCLE for range A	3.33ns	1Ah	2.67ns	15h	2.43ns	13h
16	Max tCYCLE for range A	3.71ns	1Eh	3.45ns	1Bh	3.45ns	1Bh
17	tCDLY range for A	4-9	49h	5-9	59h	5-9	59h
18	tCLS and tCAS range for A	tCLS = 2 tCAS = 2	AAh	2, 3tCLS = 2 tCAS = 2	AAh	2, 3tCLS = 2 tCAS = 2	AAh
19	Min tCYCLE for range B	0	00h	0	1Ah	0	1Ah
20	Max tCYCLE for range B	0	00h	0	1Eh	0	1Bh
21	tCDLY range for range B	0	00h	0	49h	0	49h
22	tCLS and tCAS range for range B	0	00h	0	AAh	0	AAh
23	Min tCYCLE range for C	0	00h	0	00h	0	00h
24	Max tCYCLE for range C	0	00h	0	00h	0	00h
25	tCDLY range for range C	0	00h	0	00h	0	00h
26	tCLS and tCAS range for range C	0	00h	0	00h	0	00h
27	Min tCYCLE for range D	0	00h	0	00h	0	00h
28	Max tCYCLE for range D	0	00h	0	00h	0	00h
29	tCDLY range for range D	0	00h	0	00h	0	00h
30	tCLS and tCAS range for range D	0	00h	0	00h	0	00h
31	tPDNXA, Min	4us	04h	4us	04h	4us	04h
32	tPDNXA, Max	9000Cycles	8D	9000Cycles	8D	9000Cycles	8D
33	tNAPXA, Min	50ns	32h	50ns	32h	50ns	32h
34	tNAPXB, Min	40ns	28h	40ns	28h	40ns	28h
35	fIMIN [11:8] , fIMAX [11:8]	1.1	11h	1.1	11h	1.1	11h
36	fIMIN [7:0]	0A	0Ah	0A	0Ah	2C	2Ch
37	fIMAX [7:0]	2C	2Ch	65	65h	90	90h
38	Reserved		00h		00h		00h
39	tCCTRL, MAX	100ms	64h	100ms	64h	100ms	64h
40	tTEMP, MAX	100ms	64h	100ms	64h	100ms	64h
41	tTCEN, MIN	150tCYCLE	96h	150tCYCLE	96h	150tCYCLE	96h
42	tRAS-R, MAX	64us	40h	64us	40h	64us	40h
43	tNLIMIT, MAX	10us	0Ah	10us	0Ah	10us	0Ah
44	ACTREFPT, PCHRERPT	6.6tCYCLE	66h	6.6tCYCLE	66h	6.6tCYCLE	66h
45	CPCHREFPT_DC, RDREFPT_DC	5.5tCYCLE	55h	5.5tCYCLE	55h	5.5tCYCLE	55h
46	RETREFPT_DC, WRREFPT_DC	5.13tCYCLE	5Dh	5.13tCYCLE	5Dh	5.13tCYCLE	5Dh
47-49	Reserved		00h		00h		00h
50	fRAS [11:8]	01	01h	01	01h	01	01h
51	fRAS [7:0]	2C	2Ch	65	65h	90	90h
52	PMAX, HI, PMAX, LO, TJ		24h		24h		24h
53	Heat Spreader, Tplate		9Ah		9Ah		9Ah

Byte Number	Function	THMR1E4-6 32Mx18 (64MB + ECC), 600MHz-53ns		THMR1E4-7 32Mx18 (64MB + ECC), 711MHz-45ns		THMR1E4-8 32Mx18 (64MB + ECC), 800MHz-40ns	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
54	PSTBY, HI		5Ah		5Fh		69h
55	PACTI, HI		3Fh		46h		4Bh
56	PACTRW, HI		40h		49h		50h
57	PSTBY, LO		55h		55h		55h
58	PACTI, LO		3Ah		3Ah		3Ah
59	PACTRW. LO		3Bh		3Bh		3Bh
60	PNAP		21h		21h		21h
61	PRESA		00h		00h		00h
62	PRESB		00h		00h		00h
63	Checksum for location 0-62		8Eh		48h		D6h
64		TOSHIBA	98h	TOSHIBA	98h	TOSHIBA	98h
65-71			00h		00h		00h
72	Module manufacturing location						
73-90	Module part number						
91-92	Module revision code		00h		00h		00h
93	Module manufacturing year						
94	Module manufacturing week						
95-98	Module serial number						
99	Number of devices on module	4	04h	4	04h	4	04h
100	Module data width	18	12h	18	12h	18	12h
101	Device enable	All 4 device enabled	0Fh	All 4 device enabled	0Fh	All 4 device enabled	0Fh
102			00h		00h		00h
103			00h		00h		00h
104			00h		00h		00h
105	Module Vdd, Module Voltage Interface level	2.5V,1.8V	10h	2.5V,1.8V	10h	2.5V,1.8V	10h
106	Module VDD tolerance	5% DC 2% AC	52h	5% DC 2% AC	52h	5% DC 2% AC	52h
107-113	Reserved		00h		00h		00h
114	CDLY0/1 for tCDLY = 3	–	00h	–	00h	–	00h
115	CDLY0/1 for tCDLY = 4	2/0	20h	2/0	20h	2/0	20h
116	CDLY0/1 for tCDLY = 5	3/0	30h	3/0	30h	3/0	30h
117	CDLY0/1 for tCDLY = 6	3/1	31h	3/1	31h	3/1	31h
118	CDLY0/1 for tCDLY = 7	3/2	32h	3/2	32h	3/2	32h
119	CDLY0/1 for tCDLY = 8	4/2	42h	4/2	42h	4/2	42h
120	CDLY0/1 for tCDLY = 9	5/2	52h	5/2	52h	5/2	52h
121	CDLY0/1 for tCDLY = 10	–	00h	–	00h	–	00h
122	CDLY0/1 for tCDLY = 11	–	00h	–	00h	–	00h
123	CDLY0/1 for tCDLY = 12	–	00h	–	00h	–	00h
124	CDLY0/1 for tCDLY = 13	–	00h	–	00h	–	00h
125	CDLY0/1 for tCDLY = 14	–	00h	–	00h	–	00h
126	CDLY0/1 for tCDLY = 15	–	00h	–	00h	–	00h
127	Checksum for location 99-126		00h		00h		00h

BLOCK DIAGRAM



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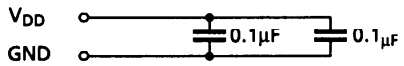

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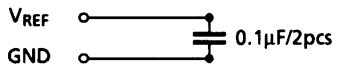

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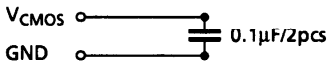

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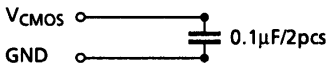
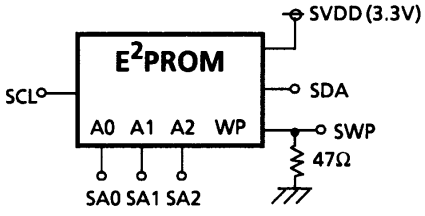


Serial Presence Detect



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{I, ABS}$	Voltage applied to any RSL pin with respect to Gnd	-0.3	$V_{DD}+0.3$	V
$V_{I, CMOS, ABS}$	Voltage applied to any CMOS pin with respect to Gnd	-0.3	$V_{DD}+0.3$	V
$V_{DD, ABS}$	Voltage on VDD with respect to Gnd	-0.5	$V_{DD}+1.0$	V
$T_{J, ABS}$	Junction temperature under bias	T. B. D	T. B. D	°C
T_{STORE}	Storage temperature	-50	100	°C

THERMAL PARAMETERS

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
T_J	Junction operating temperature	0	100	°C
θ_{JA}	Jution-to-Ambient thermal resistance		T.B.D.	°C/Watt

I_{DD}-SUPPLY CURRENT PROFILE

POWER STATE	RDRAM BLOCKS CONSUMING POWER	-8 MAX[a]	UNIT
RESET	Refresh only	T.B.D.	mA
REG	Refresh only	T.B.D.	mA
PDN	Refresh only	T.B.D.	mA
NAP	Refresh, T/RCLK-Npa	T.B.D.	mA
STBY	Refresh, T/RCLK-Fast, ROW-demux	T.B.D.	mA
ATTN	Refresh, T/RCLK-Fast, ROW-demux, COL-demux	T.B.D.	mA
ATTNW	Refresh, T/RCLK-Fast, ROW-demux, COL-demux, DQ-demux, 1 ·WR-SenseAmp, 4 ·ACT-Bank	T.B.D.	mA
ATTNR	Refresh, T/RCLK-Fast, ROW-demux, DQ-mux, COL-demux, 1 ·RD-SenseAmp, 4 ·ACT-Bank	T.B.D.[b]	mA

a. These I_{DD} numbers are manufacturer-dependent ; the numbers shown are representative maximum current levels at 1600MB/s.
b. This does not include the I_{OL} sink current. The RDRAM disipates $I_{OL} \cdot V_{OL}$ in each ouput driver when a logic one is driven.

RECOMMENDED CONDITIONS

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
V_{DD}, V_{DDA}	Supply Voltage	2.50-0.13	2.50 + 0.13	V
V_T	Termination Voltage	1.80-0.09	1.80 + 0.09	V
V_{REF}	Reference Voltage	1.40-0.2	1.40 + 0.2	V
V_{IL}	RSL input low Voltage	V_{REF}-0.5	V_{REF}-0.2	V
V_{IH}	RSL input high Voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL, COMS}$	CMOS input low Voltage	-0.3	$0.5V_{DD}$ - 0.25	V
$V_{IH, CMOS}$	CMOS input high Voltage	$0.5V_{DD}$ + 0.25	V_{DD} + 0.3	V

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
I_{REF}	VREF current @ $V_{REF, MAX}$	T. B. D.	T. B. D.	μA
I_{OH}	RSL output high current @ ($0 \leq V_{OUT} \leq V_{DD}$)	T. B. D.	T. B. D.	μA
I_0 (auto)	RSL I_{OL} current @ V_{OUT} = 1.7V @ Z_{OUT} = large[a]	T. B. D.	T. B. D.	mA
I_{20} (auto)	RSL I_{OL} current @ V_{OUT} = 1.7V @ Z_{OUT} = 40Ω	T. B. D.	T. B. D.	mA
I_{40} (auto)	RSL I_{OL} current @ V_{OUT} = 1.7V @ Z_{OUT} = 20Ω	T. B. D.	T. B. D.	mA
DI_{OL}	RSL I_{OL} current resolution step	-	T. B. D.	mA
r_{OUT}	Dynamic output impedance	T. B. D.	-	Ohm
$I_{I, CMOS}$	CMOS input leakage current @ ($0 \leq V_{I, CMOS} \leq V_{DD}$)	T. B. D.	T. B. D.	μA
$V_{OL, CMOS}$	CMOS output Voltage @ $I_{OL, CMOS}$ = 1.0mA	-	0.3	V
$V_{OH, CMOS}$	CMOS output high Voltage @ $I_{OH, CMOS}$ = -0.25mA	VDD - 0.3	-	V

a. Z_{OUT} is the load on the output used for CAL/SAM calibration ; output pin under test is unloaded. V_{TERM} = 1.8V and V_{REF} = 1.4V.

CAPACITANCE AND INDUCTANCE

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
C_I	RSL input parasitic capacitance	T.B.D.	T.B.D.	pF
L_I	RSL input parasitic inductance		T.B.D.	nH
$C_{I, CMOS}$	CMOS input parasitic capacitance		T.B.D.	pF

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	-6 MIN	-6 MAX	-8 MIN	-8 MAX	UNIT
t_Q	CTM-to-DQA/DQB output time	T. B. D.	T. B. D.	T. B. D.	T. B. D.	ns
t_{QR}, t_{QF}	DQA/DQB output rise and fall times	T. B. D.	T. B. D.	T. B. D.	T. B. D.	ns
t_{Q1}	SCK-to-SIO_{OUT}[a] delay @ C_{LOAD} = 40pf	-	T. B. D.	-	T.B.D.	ns
t_{QR1}, t_{QF1}	SIO_{OUT} rise/fall @ C_{LOAD} = 40pF	-	T. B. D.	-	T. B. D.	ns
t_{PROP1}	SIO_{IN}-to-SIO_{OUT} delay @ C_{LOAD} = 40pF	-	T. B. D.	-	T. B. D.	ns
t_{NXB}	NAP exit delay-phase B	-	T. B. D.	-	T. B. D.	ns
t_{PXB}	PDN exit delay-phase B	-	T. B. D.	-	T. B. D.	µs
t_{AS}	ATTN-to-STBY power state delay	T. B. D.	T. B. D.	T. B. D.	T. B. D.	t_{CYCLE}
t_{SA}	STBY-to-ATTN power state delay	-	T. B. D.	-	T. B. D.	t_{CYCLE}
t_{ASN}	ATTN/STBY-to-NAP power state delay	-	T. B. D.	-	T.B.D.	t_{CYCLE}
t_{ASP}	ATTN/STBY-to-PDN power state delay	-	T. B. D.	-	T.B.D.	t_{CYCLE}

a. SIO_{OUT} refers to the SIO0 or SIO1 pin when used as an output.

RECOMMENDED TIMING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CR}, t_{CF}	CTM and CFM input rise and fall times	0.2	0.5	ns
t_{CYCLE}	CTM and CFM cycle times (600) (711) (800)	3.33 2.80 2.50	3.83	ns
t_{CH}, t_{CL}	CTM and CFM high and low times	40%	60%	t_{CYCLE}
t_{TR}	CTM-CFM differential (MSE/MS = 0/0) (MSE/MS = 1/1)	0.0 0.9	1.0 1.0	t_{CYCLE}
t_{DR}, t_{DF}	DQA/DQB/ROW/COL input rese/fall times	0.3	0.6	ns
t_S, t_H	DQA/DQB/ROW/COL-to-CFM set/hold @ tCYCLE = 3.33ns	0.275	-	ns
	DQA/DQB/ROW/COL-to-CFM set/hold @ tCYCLE = 2.81ns	0.240	-	ns
	DQA/DQB/ROW/COL-to-CFM set/hold @ tCYCLE = 2.50ns	0.200	-	ns
t_{DR1}, t_{DF1}	SIO_{IN}[a], CMD, SCK input rise and fall times	-	5.0	ns
t_{CYCLE1}	SCK cycle time-Serial control register transactions	1000	-	ns
	SCK cycle time-Power transitions	10	-	ns
t_{CH1}, t_{CL1}	SCK high and low times	4.2	-	ns
t_{S1}	CMD setup time	1	-	ns
t_{H1}	CMD hold time	1	-	ns
t_{S2}	SIO_{IN} setup time	40	-	ns
t_{H2}	SIO_{IN} hold time	40	-	ns
t_{S3}	PDEV setup time on DQA5..0	0	-	ns
t_{H3}	PDEV hold time on DQA5..0	5.5	-	ns
t_{S4}	ROW2..0, COL4..0 setup time for quiet window	-1	-	t_{CYCLE}
t_{H4}	ROW2..0, COL4..0 hold time for quiet window	5	-	t_{CYCLE}
t_{CE}	CTM/CFM stable before NAP/PDN exit	2	-	t_{CYCLE}
t_{CD}	CTM/CFM stable after NAP/PDN entry	100	-	t_{CYCLE}
t_{FRM}	ROW packet to COL packet ATTN framing delay	7	-	t_{CYCLE}
t_{NLIMIT}	Maximum time in NAP mode		10.0	µs
t_{REF}	Refresh interval		32	ms
t_{RAS}	RAS interval (time a row may stay activated)		64	µs
t_{PAUSE}	RDRAM substrate bias generator delay		200.0	µs

a. SIO_{IN} refers to the SIO0 or SIO1 pin when used as an input.

RECOMMENDED TIMING CONDITIONS

SYMBOL	PARAMETER	MIN-6	MIN-7	MIN-8			MAX	UNIT
t_{RC}	Row CYcle time of RDRAM banks-the interval betwee ROWA packets with ACT commands to the same bank.	28	28	28			-	t_{CYCLE}
t_{RAS}	RAS-asserted time of RDRAM bank-the interval between ROWA packet with ACT command and next ROWR packet with PRER command to the same bank.	20	20	20			-	t_{CYCLE}
t_{RP}	Row Precharge time of RDRAM banks-the interbal between ROWR packet with PRER command and next ROWA packet with ACT command to the same bank.	8	8	8			-	t_{CYCLE}
t_{PP}	Precharge-to-precharge time of RDRAM device-the interval between successive ROWR packets with PRER commands to different banks of the same device.	8	8	8			-	t_{CYCLE}
t_{RR}	RAS-to-RAS time of RDRAM device-the interbal between successive ROWA packets with ACT commands to different banks of the same device.	8	8	8			-	t_{CYCLE}
t_{RCD}	RAS-toCAS Delay-the interval from ROWA packet with ACT command to COLC paket with RD or WR command). Note-the RAS-to-CAS delay seen by the RDRAM core ($t_{RCD, CORE}$) is equal to $t_{RCD, CORE} = 0$ + t_{RCD} because of differences in the row and column paths through the RDRAM interface.	7	7	7			-	t_{CYCLE}
t_{RAC}	RAS Access delay-effective interval from ROWA packet with ACT command to Q read data. This is equal to: $t_{RAC} = 1 + t_{RCD} + t_{CAC}$.	16	16	16			-	t_{CYCLE}
t_{CAC}	CAS Access delay-the minimum interval from RD command to Q read data.	8	8	8			12	t_{CYCLE}
t_{CWD}	CAS Write Delay (interval from WR command to D write data.	6	6	6			6	t_{CYCLE}
t_{CC}	CAS-to-CAS time of RDRAM bank-the interval between successive COLC commands.	4	4	4			-	t_{CYCLE}
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4			4	t_{CYCLE}
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to optional COLM packet with bytemask.	8	8	8			-	t_{CYCLE}
t_{OFFP}	Interval from last COLC packet with RD or automatic retier command to ROWR packet with PRER. Also, the interval (offset) from COLC packet with RDA command, or from COLC packet with retire command(after WRA automatic precharge), or from COLX packet with PREX command to the equivalent ROWR packet with PRER.	4	4	4				t_{CYCLE}

RSL CLOCKING AND BIT TRANSPOT

Figure 2 shows the timing required to receive or transmit a pair of RSL bits. A single clock cycle T_2 from the central figure is expanded to show the details associated with a falling edg e and rising edge of the CFM and CTM clock inputs (the CTFN and CTMN inputs will always be at the opposite signal level). Note that RSL signals are low-true ; a high voltage is logic zero.

Figure 2a shows the rise/fall requirements of RSL input signals, and the rise/fall characterisitics of RSL output signals.

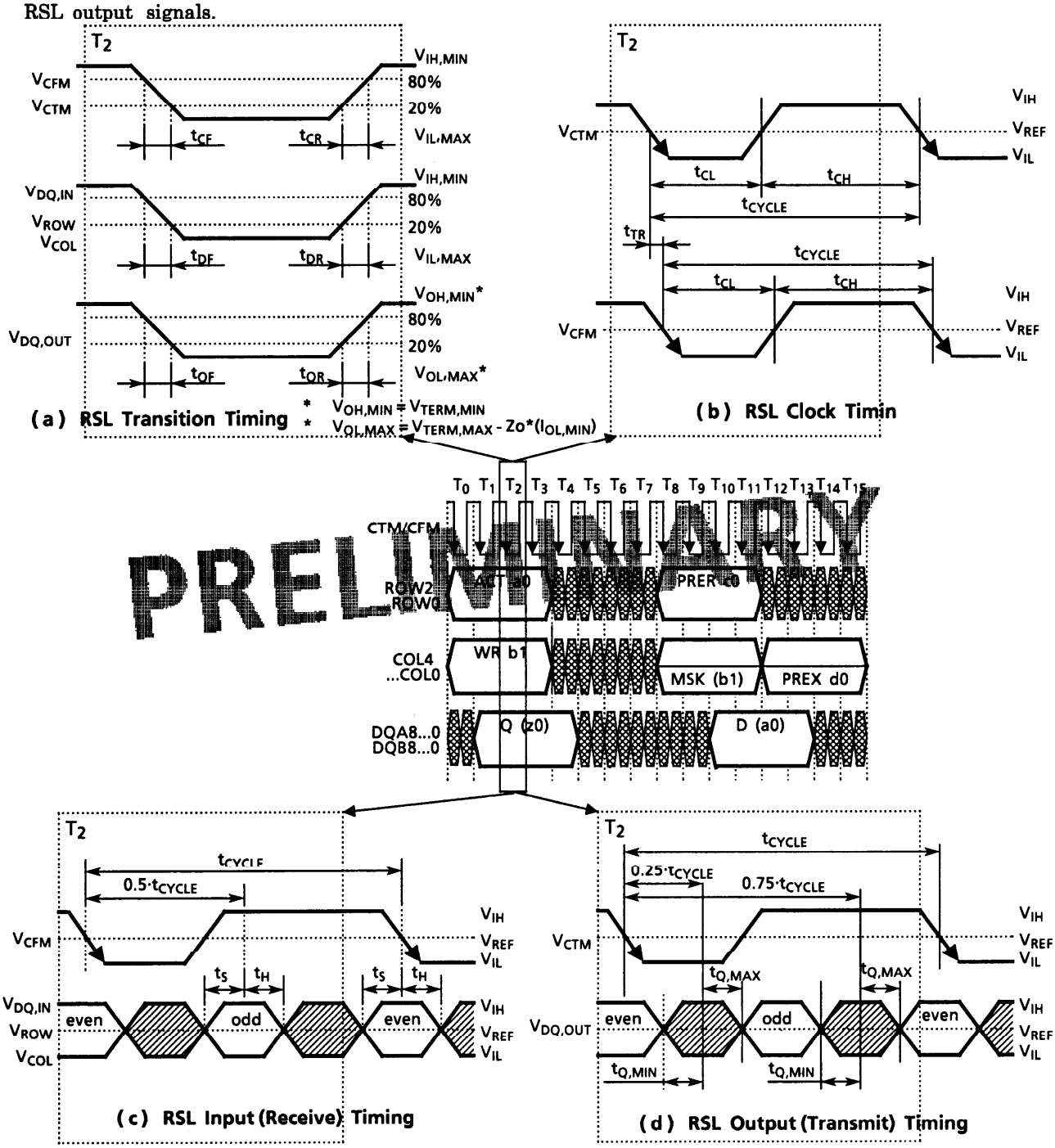


Figure 2: RSL Timing - Clocking and Bit Transport

Figure 2b shows the duty cycle requirements of the RSL clock inputs. It also shows the t_{TR} skew parameter (the amount of time by which CTM may lead CFM).

Figure 2c shows the setup and hold requirements of RSL inputs. Even bits are sampled on the falling edge of CFM and odd bits are sampled at the half-cycle (50%) point. The RDRAM synthesizes the 25%, 50%, and 75% timing points so that tow bits may be received or transmitted per clock cycle per signal wire.

Figure 2d shows the valid window of RSL outputs. Even bits are driven from the 75% point and odd bits from the 25% point.

CMOS CLOCKING AND BIT TRANSPORT

Figure 3 shows the timing required to receive or transmit a CMOS bit. A single clock cycle is expanded to show the details associated with a falling edge of the SCK clock input. Note that all CMOS signals are lowtrue ; a high voltage is logic zero.

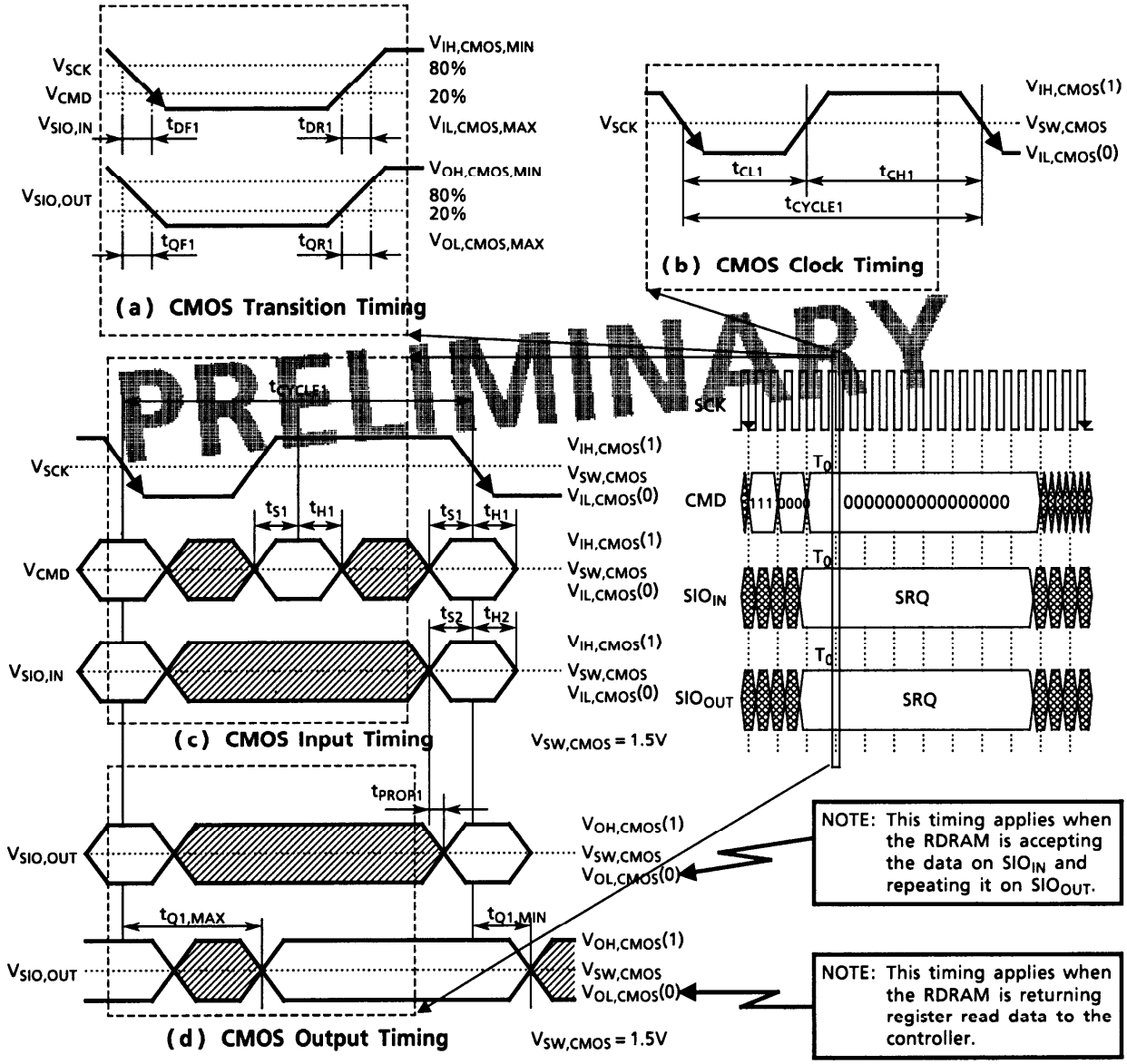
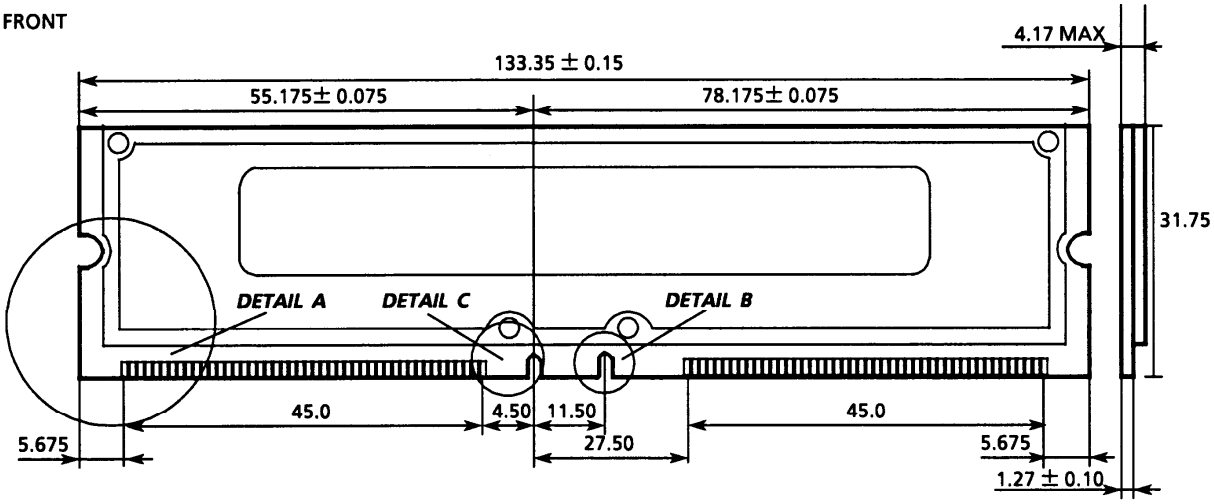
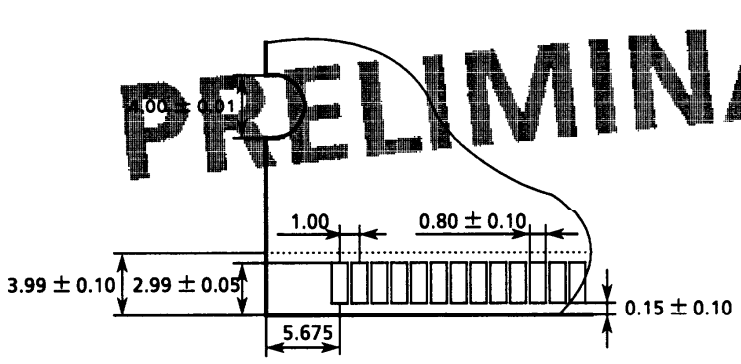


Figure 3: CMOS Timing-Clocking and Bit Transpot

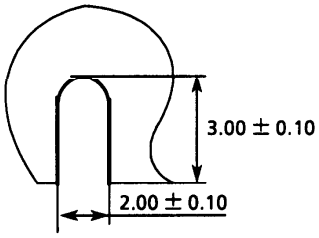
PACKAGE DIMENSIONS (THMR1E4)

Unit: mm

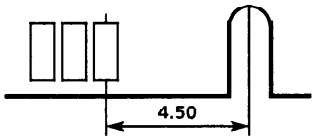




DETAIL A



DETAIL B



DETAIL C