

PACKAGE OUTLINE

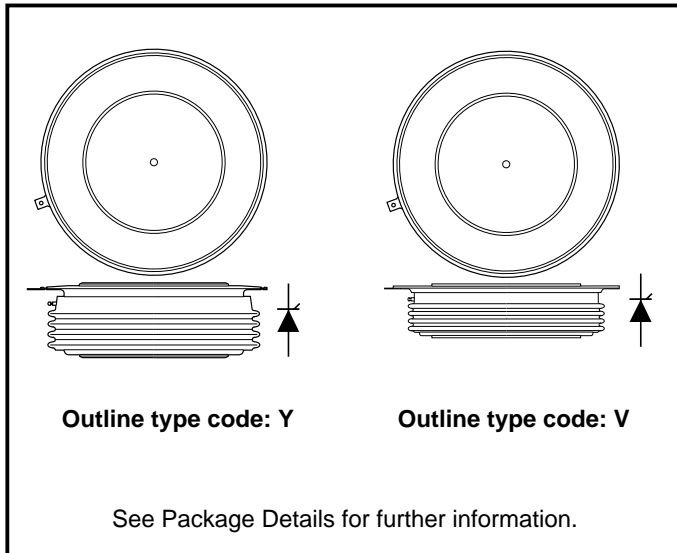


Fig. 1 Package outline

KEY PARAMETERS

V_{DRM}	2800V
$I_{T(AV)}$	3419A
I_{TSM}	54500A
dV/dt	1000V/μs
dI/dt	300A/μs

VOLTAGE RATINGS

Part Number	Repetitive Peak Voltages	Conditions
	V_{DRM} V_{RRM}	
	V	
DCR1574SY28 or DCR1574SV28	2800	$T_{vj} = 0^\circ$ to 125°C . $I_{DRM} = I_{RRM} = 300\text{mA}$. $V_{DRM}, V_{RRM} = 10\text{ms } 1/2 \text{ sine}$. $V_{DSM} \ \& \ V_{RSM} = V_{DRM} \ \& \ V_{RRM} + 100\text{V}$ respectively.

Lower voltage grades available.

ORDERING INFORMATION

When ordering select the required part number shown in the Voltage Ratings selection table.

For example:

DCR1574SY28 for a 2800V 'Y' outline variant

or

DCR1574SV28 for a 2800V 'V' outline variant

If a lower voltage grade is required, then use $V_{DRM}/100$ for the grade required e.g.:

DCR1574SY26 for a 2600V 'Y' outline variant etc.

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS $T_{\text{case}} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3419	A
$I_{T(RMS)}$	RMS value	-	5370	A
I_T	Continuous (direct) on-state current	-	4836	A
Single Side Cooled (Anode side)				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2197	A
$I_{T(RMS)}$	RMS value	-	3451	A
I_T	Continuous (direct) on-state current	-	2857	A

CURRENT RATINGS $T_{\text{case}} = 80^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2667	A
$I_{T(RMS)}$	RMS value	-	4189	A
I_T	Continuous (direct) on-state current	-	3680	A
Single Side Cooled (Anode side)				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1680	A
$I_{T(RMS)}$	RMS value	-	2640	A
I_T	Continuous (direct) on-state current	-	2140	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine; $T_{case} = 125^{\circ}C$ $V_R = 50\% V_{RRM} - 1/4$ sine	43.8	kA
I^2t	I^2t for fusing		9.59×10^6	A ² s
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine; $T_{case} = 125^{\circ}C$ $V_R = 0$	54.5	kA
I^2t	I^2t for fusing		14.85×10^6	A ² s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.0095	$^{\circ}C/W$
		Single side cooled	Anode dc	-	0.019	$^{\circ}C/W$
			Cathode dc	-	0.019	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 50kN with mounting compound	Double side	-	0.002	$^{\circ}C/W$
			Single side	-	0.004	$^{\circ}C/W$
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	$^{\circ}C$
		Reverse (blocking)		-	125	$^{\circ}C$
T_{stg}	Storage temperature range			-55	150	$^{\circ}C$
-	Clamping force			45	55	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Conditions	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	300	mA	
dV/dt	Maximum linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$.	1000	V/ μ s	
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1000A Gate source 20V, 10 Ω $t_r \leq 0.5\mu$ s, $T_j = 125^{\circ}C$	Repetitive 50Hz	250	A/ μ s
			Non-repetitive	500	A/ μ s
$V_{T(TO)}$	Threshold voltage	At $T_{vj} = 125^{\circ}C$	0.883	V	
r_T	On-state slope resistance	At $T_{vj} = 125^{\circ}C$	0.11	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, Gate source 30V, 15 Ω , $t_r \leq 0.5\mu$ s, $T_j = 25^{\circ}C$	2	μ s	
t_q	Turn-off time	$I_T = 4000A$, $t_p = 3ms$, $T_j = 125^{\circ}C$, $V_{RM} = 200V$, $dl_{RR}/dt = 6A/\mu$ s, $V_{DR} = 67\% V_{DRM}$, $dV_{DR}/dt = 20V/\mu$ s linear	400	μ s	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	1000	mA	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{g-k} = \infty$	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V$, $T_{case} = 25^{\circ}C$	3.0	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V$, $T_{case} = 25^{\circ}C$	300	mA
V_{GD}	Gate non-trigger voltage	At V_{DRM} , $T_{case} = 125^{\circ}C$	0.25	V
V_{FGM}	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V_{FGN}	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V_{RGM}	Peak reverse gate voltage		5	V
I_{FGM}	Peak forward gate current	Anode positive with respect to cathode	30	A
P_{GM}	Peak gate power	See figs. 7 and 8, gate characteristics table	150	W
$P_{G(AV)}$	Mean gate power		10	W

CURVES

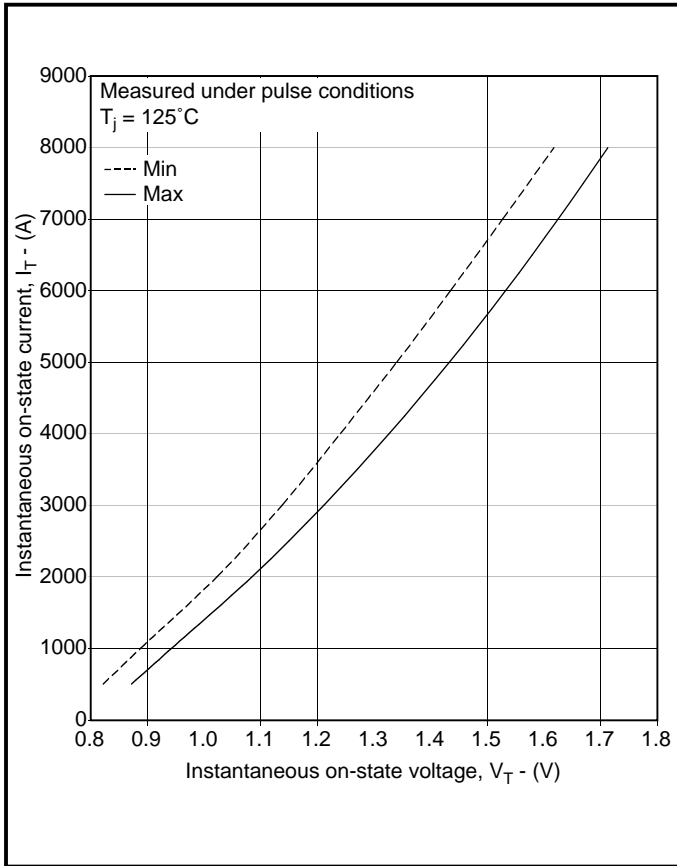


Fig.2 Maximum (limit) on-state characteristics

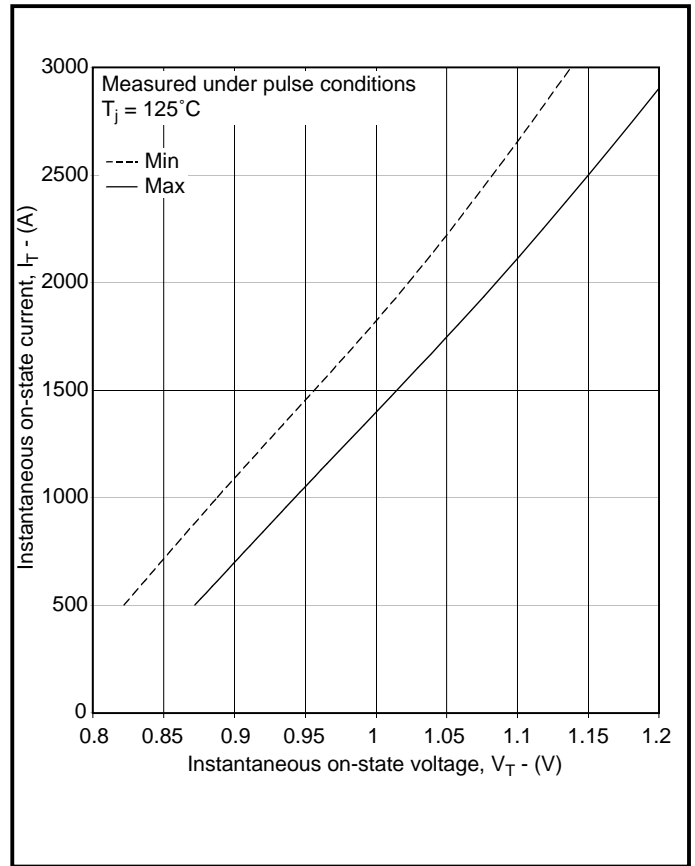


Fig.3 Maximum (limit) on-state characteristics

V_{TM} Equation:

$$V_{TM(max)} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where

- A = 1.328994
- B = -0.1381631
- C = 3.565973 x 10⁻⁶
- D = 0.01786171

These values are valid for T_j = 125°C for I_T 500A to 6000A

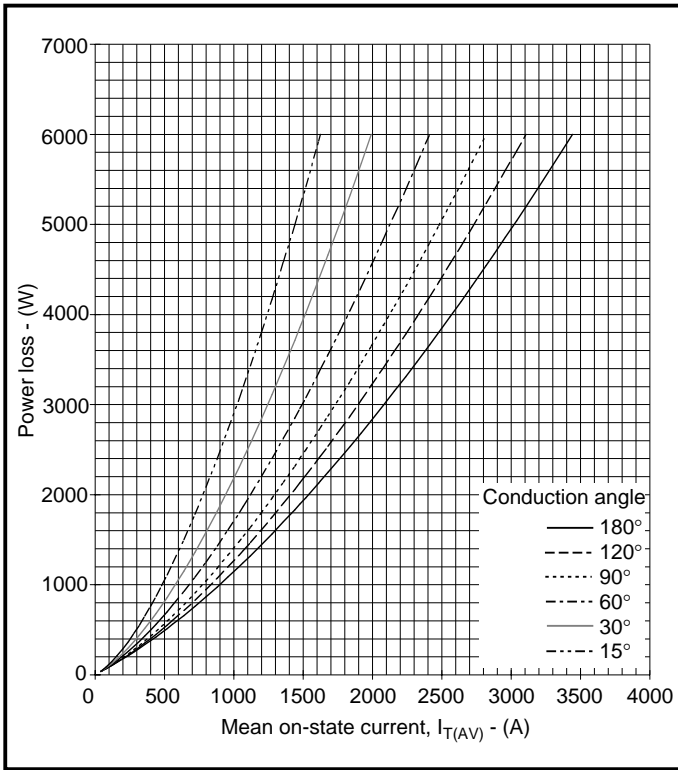


Fig.4 Sine wave power dissipation curves

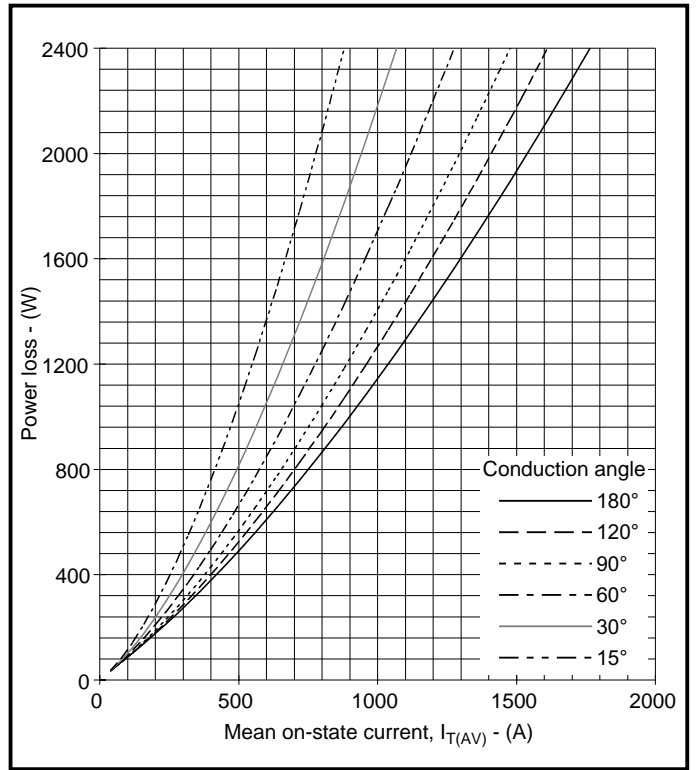


Fig.5 Sine wave power dissipation curves

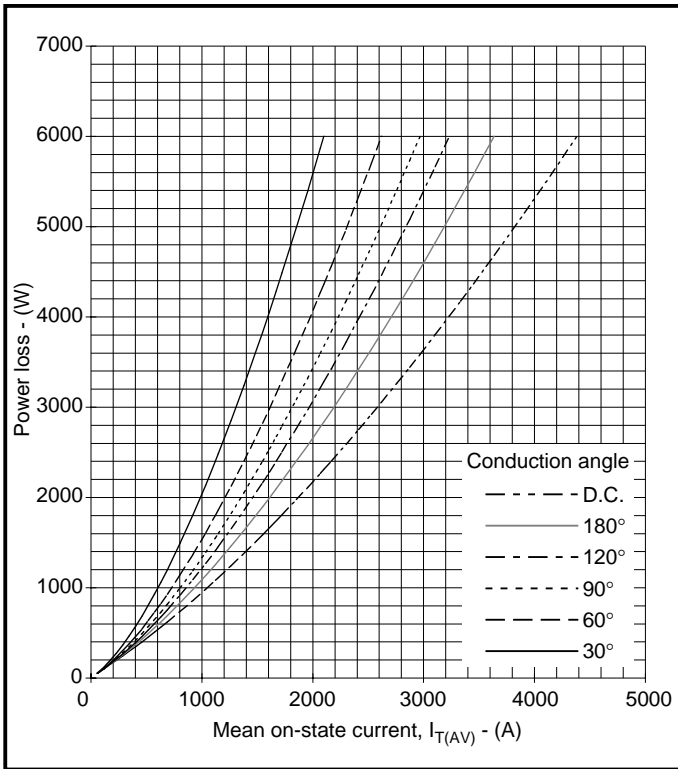


Fig.6 Square wave power dissipation curves

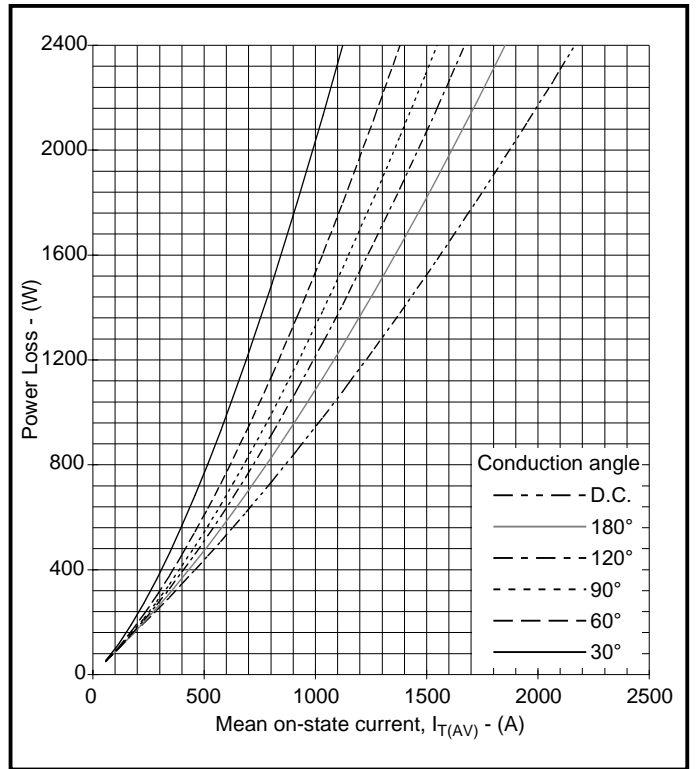


Fig.7 Square wave power dissipation curves

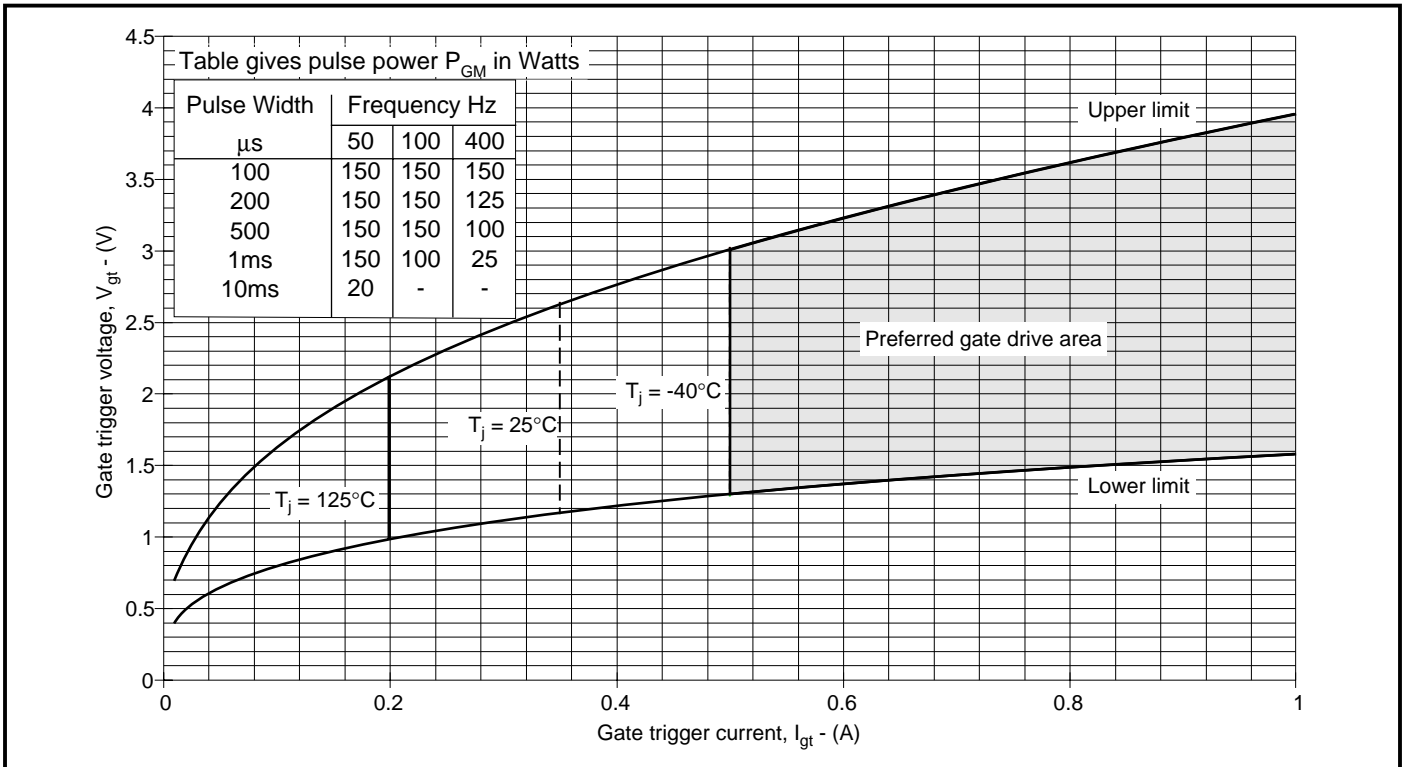


Fig.7 Gate characteristics

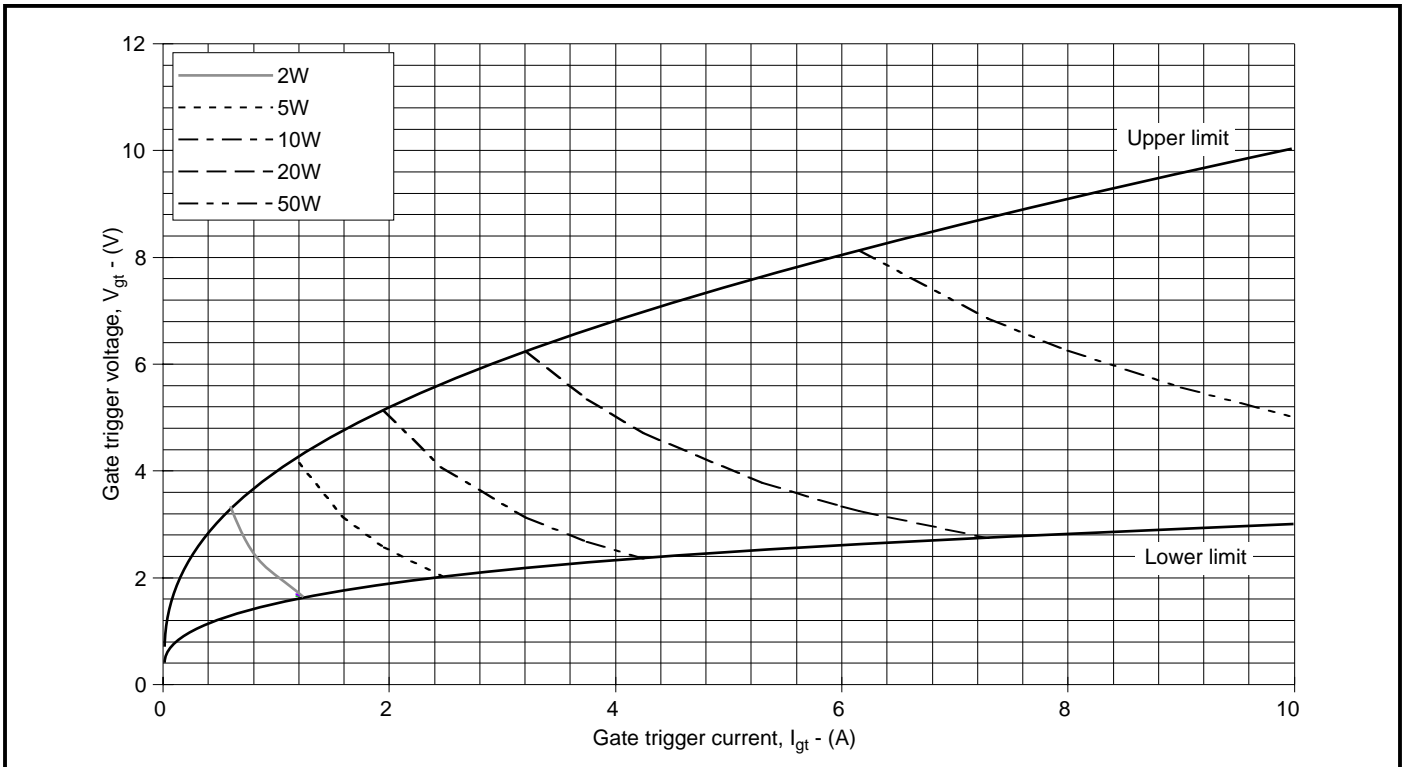


Fig.8 Gate characteristics

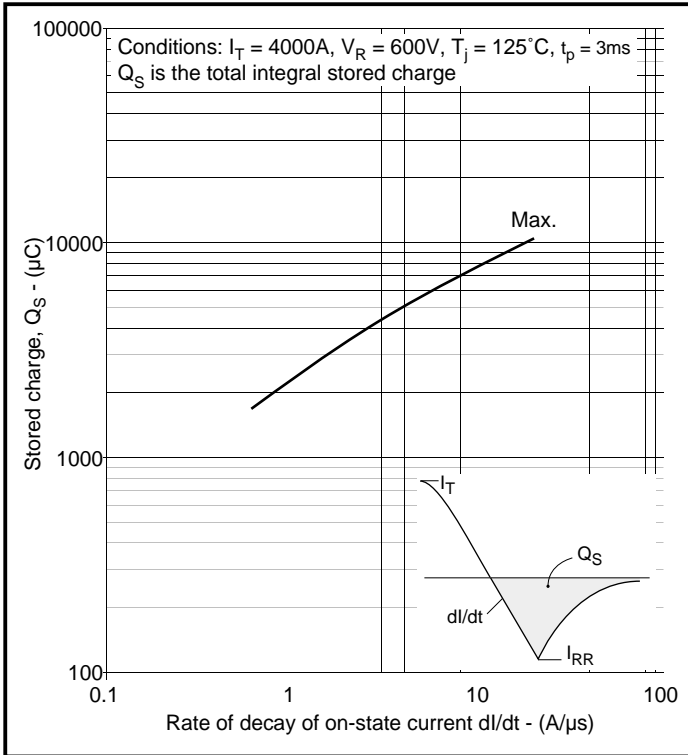


Fig.9 Stored charge

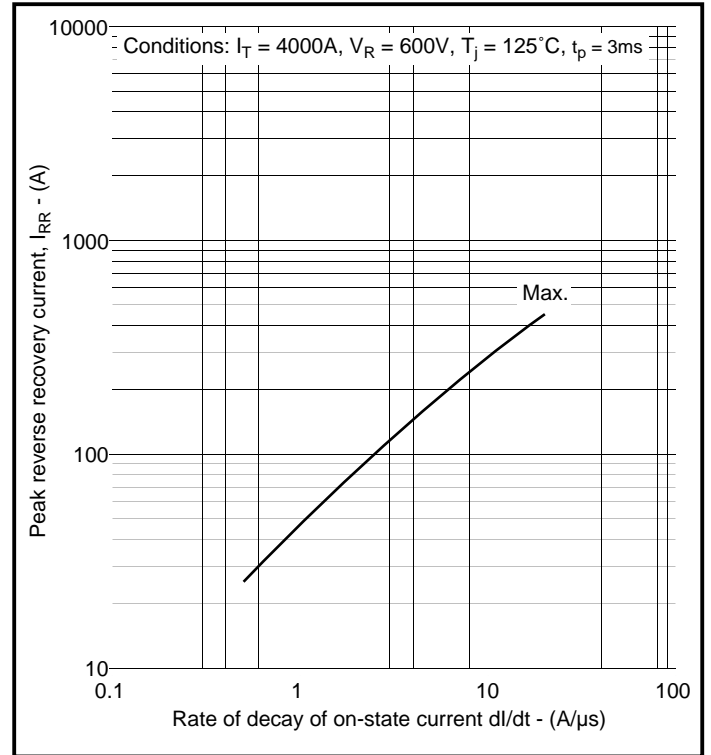


Fig.10 Reverse recovery current

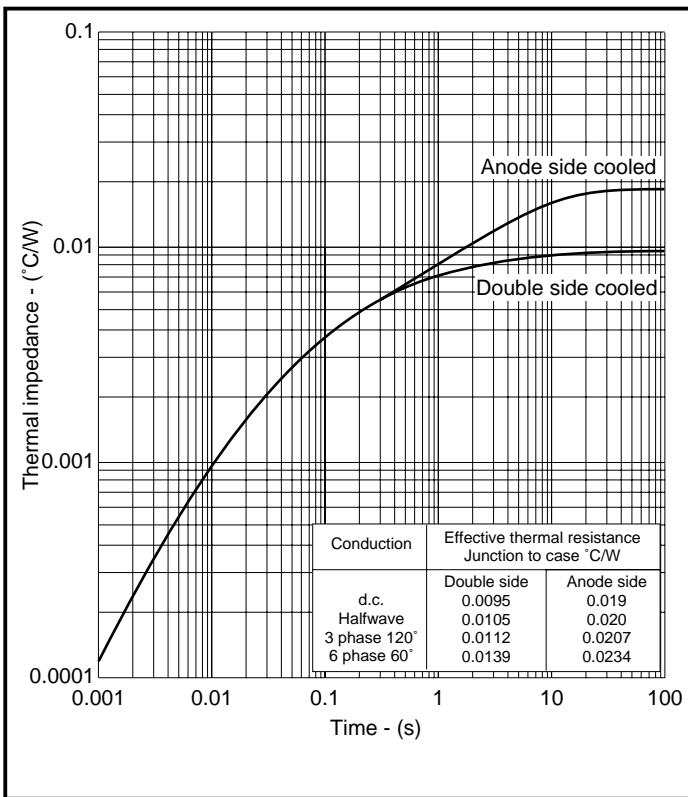


Fig.11 Maximum (limit) transient thermal impedance - junction to case

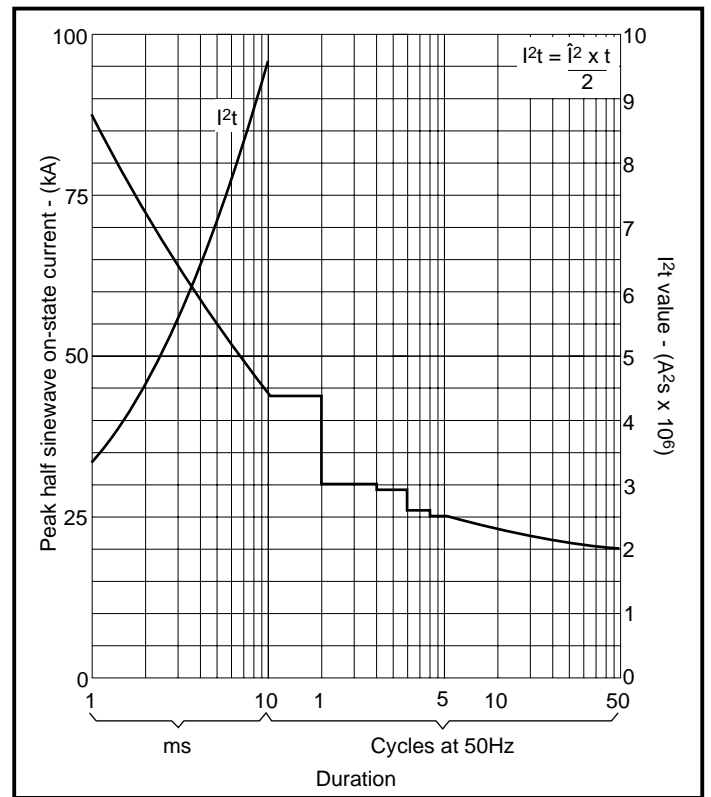


Fig.12 Surge (non-repetitive) on-state current vs time (with 50% V_{RRM} at $T_{case} = 125^\circ C$)

PACKAGE DETAILS

For further package information, please contact Customer Service. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

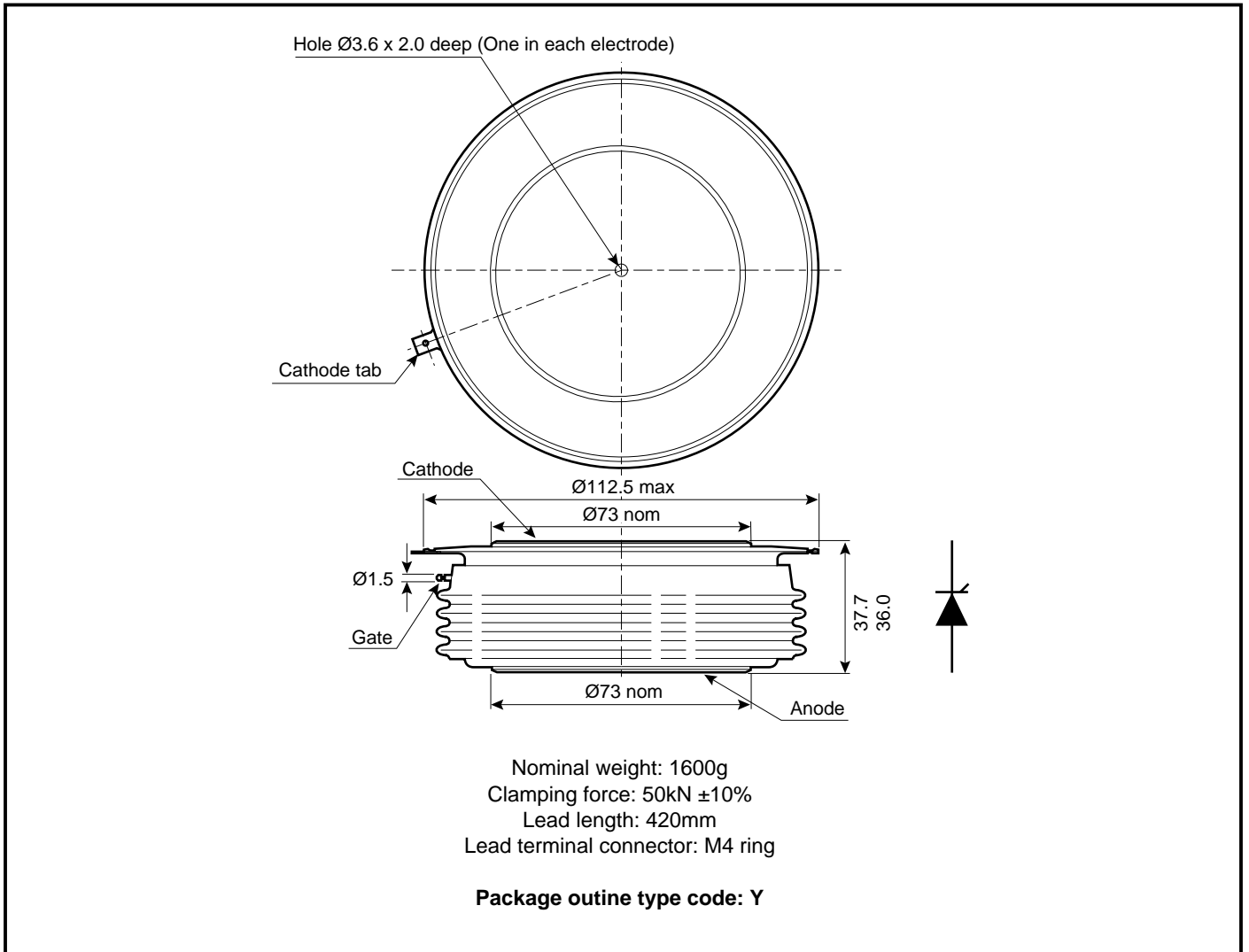


Fig.12 Package details

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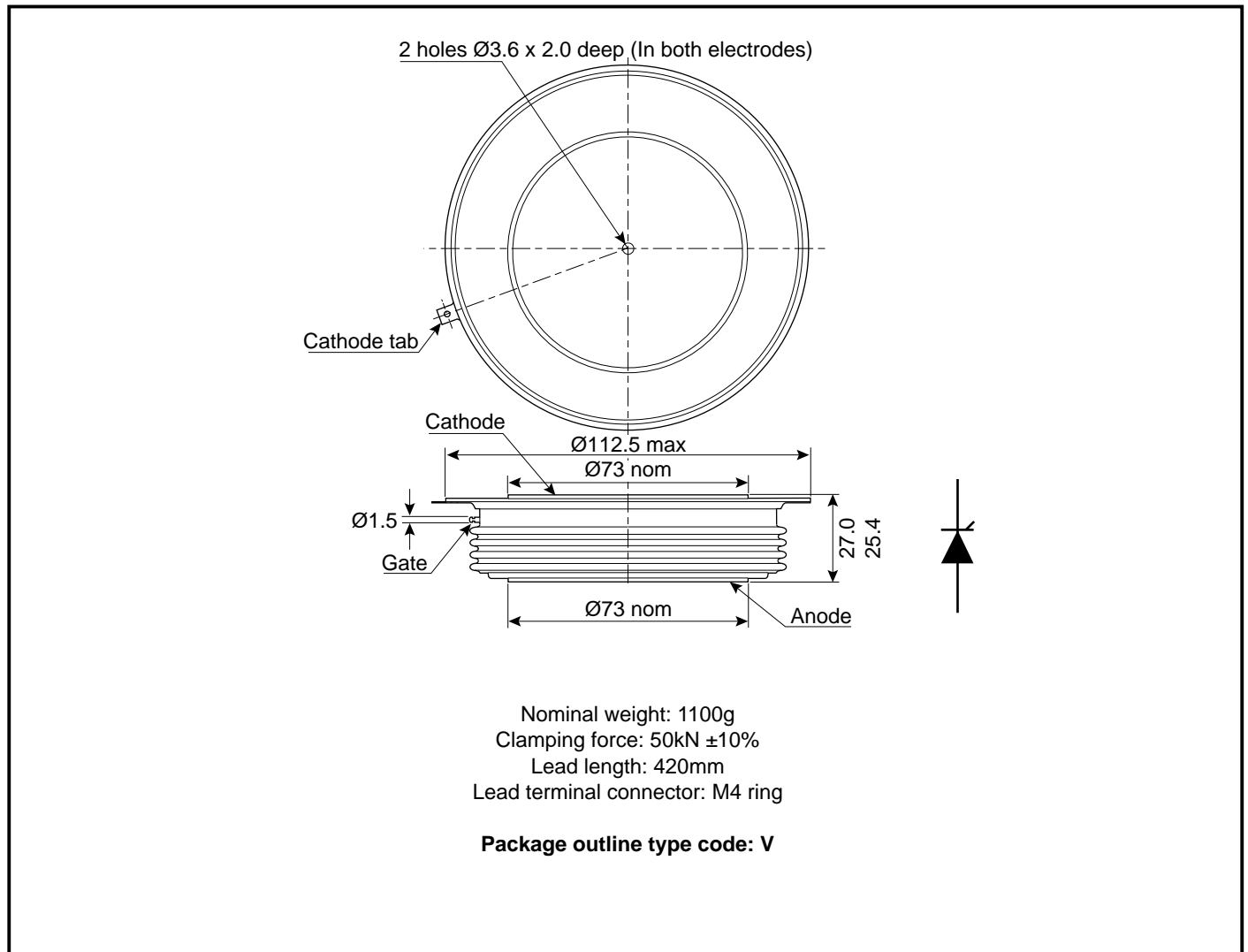


Fig.12 Package details

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.



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Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

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