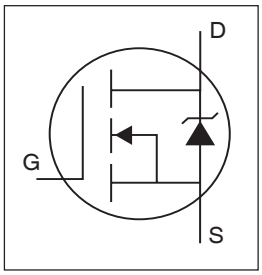
International
IOR Rectifier

PD - 95093A

# IRLR8103VPbF

- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications
- 100% $R_G$ Tested
- Lead-Free


**Description**

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRLR8103V has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and Cdv/dt-induced turn-on immunity. The IRLR8103V offers an extremely low combination of $Q_{sw}$ & $R_{DS(on)}$ for reduced losses in both control and synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.

DEVICE CHARACTERISTICS⑤

| | **IRLR8103V** |
|---|---|
| $R_{DS(on)}$ | 7.9 mΩ |
| $Q_G$ | 27 nC |
| $Q_{SW}$ | 12 nC |
| $Q_{OSS}$ | 29nC |

## Absolute Maximum Ratings

| Parameter | | Symbol | IRLR8103V | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain or Source Current | TC = 25°C | $I_D$ | 91 | A |
| ($V_{GS}$ > 10V) | TC= 90°C | | 63 | |
| Pulsed Drain Current ① | | $I_{DM}$ | 363 | |
| Power Dissipation ③ | TC = 25°C | $P_D$ | 115 | W |
| | TC = 90°C | | 60 | |
| Junction & Storage Temperature Range | | $T_J$ , $T_{STG}$ | -55 to 150 | °C |
| Continuous Source Current (Body Diode) | | $I_S$ | 91 | A |
| Pulsed Source Current ① | | $I_{SM}$ | 363 | |

## Thermal Resistance

| Parameter | Symbol | Typ. | Max. | Units |
|---|---|---|---|---|
| Maximum Junction-to-Ambient ③⑥ | $R_{\theta JA}$ | — | 50 | °C/W |
| Maximum Junction-to-Case ⑥ | $R_{\theta JC}$ | — | 1.09 | |



12/0604

## Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | 30 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | — | 6.9 | 9.0 | mΩ | $V_{GS}$ = 10V, $I_D$ = 15A ② |
| | | — | 7.9 | 10.5 | | $V_{GS}$ = 4.5V, $I_D$ = 15A ② |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | — | 3.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| Drain-to-Source Leakage Current | $I_{DSS}$ | — | — | 50 | µA | $V_{DS}$ = 30V, $V_{GS}$ = 0V |
| | | — | — | 20 | µA | $V_{DS}$ = 24V, $V_{GS}$ = 0 |
| | | — | — | 100 | | $V_{DS}$ = 24V, $V_{GS}$ = 0, $T_J$ = 100°C |
| Gate-Source Leakage Current | $I_{GSS}$ | — | — | ±100 | nA | $V_{GS}$ = ± 20V |
| Total Gate Charge, Control FET | $Q_G$ | — | 27 | — | nC | $V_{GS}$ = 5V, $I_D$ = 15A, $V_{DS}$ = 16V |
| Total Gate Charge, Synch FET | $Q_G$ | — | 23 | — | | $V_{GS}$ = 5V, $V_{DS}$ < 100mV |
| Pre-Vth Gate-Source Charge | $Q_{GS1}$ | — | 4.7 | — | | $V_{DS}$ = 16V, $I_D$ = 15A |
| Post-Vth Gate-Source Charge | $Q_{GS2}$ | — | 2.0 | — | | |
| Gate to Drain Charge | $Q_{GD}$ | — | 9.7 | — | | |
| Switch Charge ($Q_{gs2}$ + $Q_{gd}$) | $Q_{SW}$ | — | 12 | — | | |
| Output Charge | $Q_{OSS}$ | — | 29 | — | | $V_{DS}$ = 16V, $V_{GS}$ = 0 |
| Gate Resistance | $R_G$ | 0.8 | — | 3.1 | Ω | |
| Turn-On Delay Time | $t_{d(on)}$ | — | 10 | — | ns | $V_{DD}$ = 16V |
| Rise Time | $t_r$ | — | 9 | — | | $I_D$ = 15A |
| Turn-Off Delay Time | $t_{d(off)}$ | — | 24 | — | | $V_{GS}$ = 5.0V |
| Fall Time | $t_f$ | — | 18 | — | | Clamped Inductive Load |
| Input Capacitance | $C_{iss}$ | — | 2672 | — | pF | $V_{GS}$ = 16V, $V_{GS}$=0 |
| Output Capacitance | $C_{oss}$ | — | 1064 | — | | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 109 | — | | |

## Source-Drain Rating & Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | — | 0.9 | 1.3 | V | IS = 15A②, $V_{GS}$ = 0V |
| Reverse Recovery Charge ④ | $Q_{rr}$ | — | 103 | — | nC | di/dt ~ 700A/µs |
| | | | | | | $V_{DS}$ = 16V, $V_{GS}$ = 0V, $I_F$ = 15A |
| Reverse Recovery Charge (with Parallel Schottky) ④ | $Q_{rr(s)}$ | — | 96 | — | nC | di/dt = 700A/µs , (with 10BQ040) |
| | | | | | | $V_{DS}$= 16V, $V_{GS}$ = 0V, $I_F$ = 15A |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 400 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board, t < 10 sec.
④ Typ = measured - $Q_{oss}$
⑤ Typical values of $R_{DS}$(on) measured at $V_{GS}$ = 4.5V, $Q_G$, $Q_{SW}$ and $Q_{OSS}$ measured at $V_{GS}$ = 5.0V, $I_F$ = 15A.

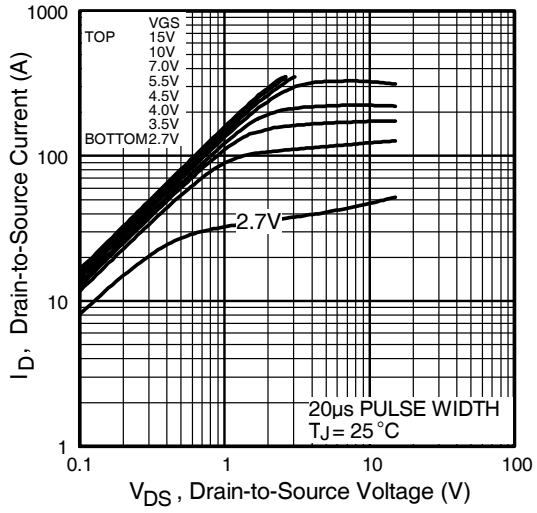



**Fig 1.** Typical Output Characteristics

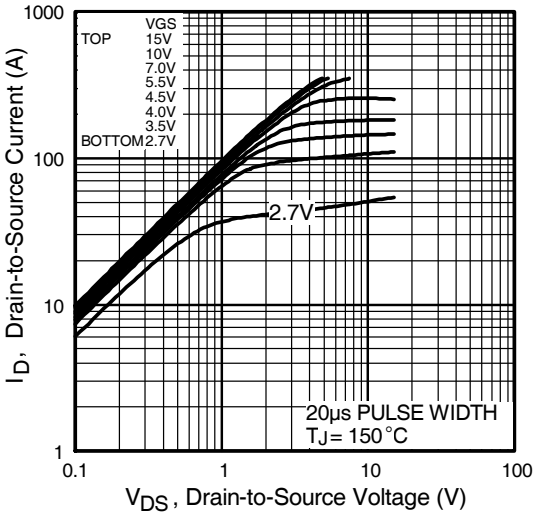



**Fig 2.** Typical Output Characteristics

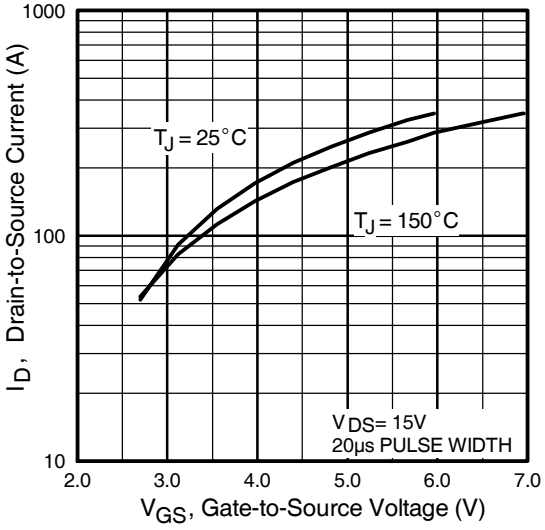



**Fig 3.** Typical Transfer Characteristics

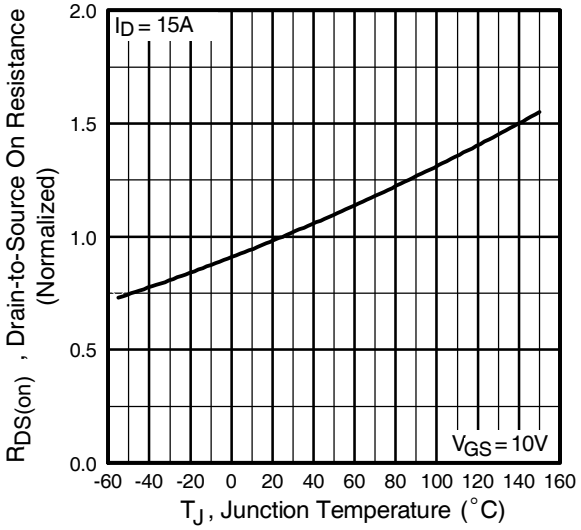



**Fig 4.** Normalized On-Resistance Vs. Temperature

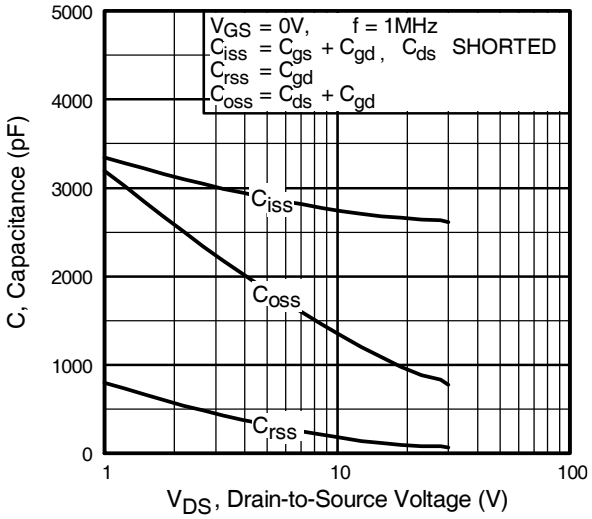



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

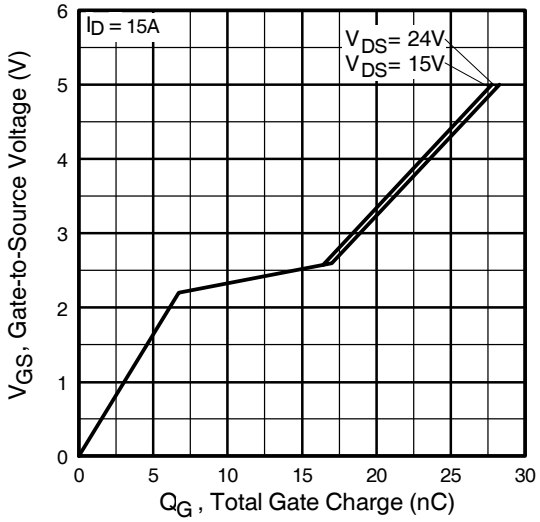



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

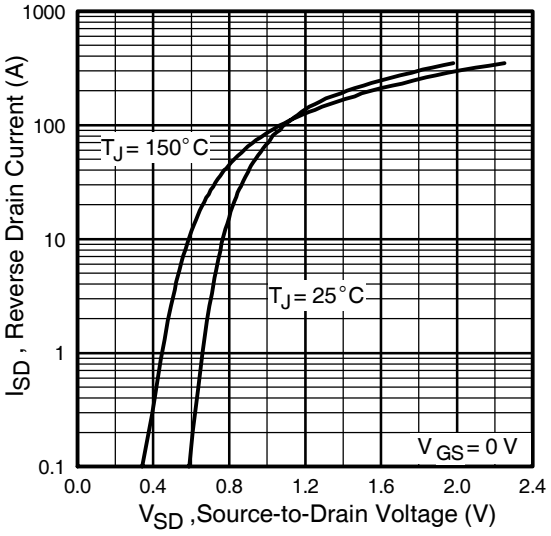



**Fig 7. Typical Source-Drain Diode Forward Voltage**

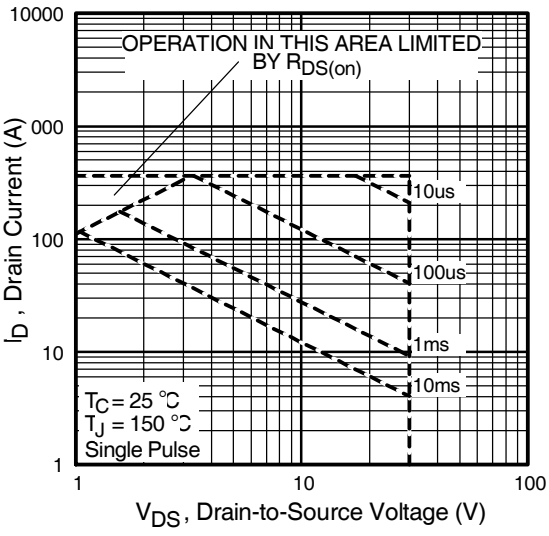



**Fig 8.** Maximum Safe Operating Area

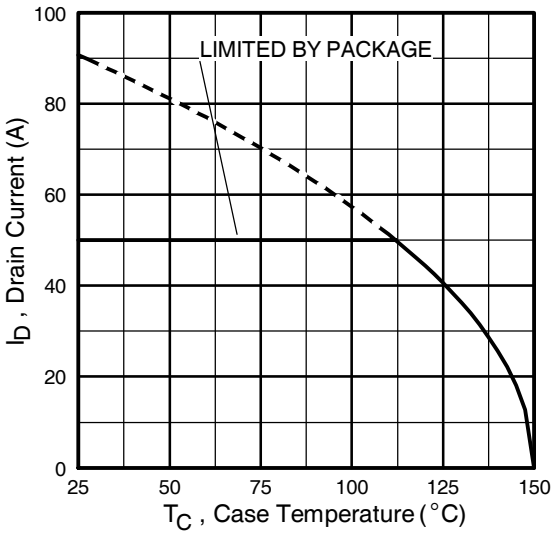



**Fig 9.** Maximum Drain Current Vs. Case Temperature

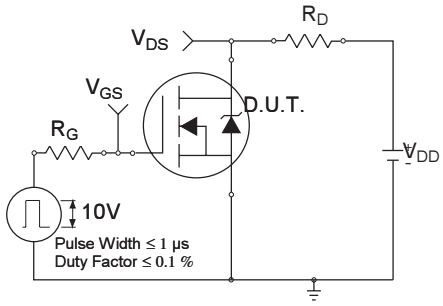



**Fig 10a.** Switching Time Test Circuit

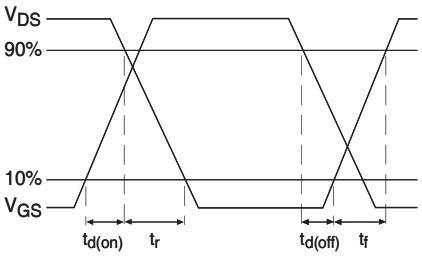



**Fig 10b.** Switching Time Waveforms

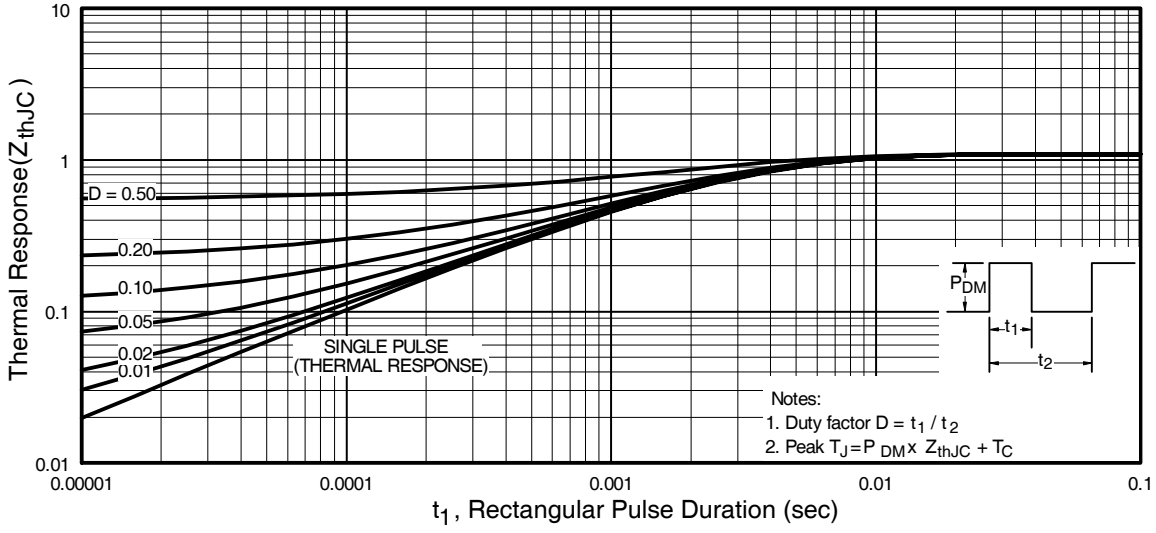



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

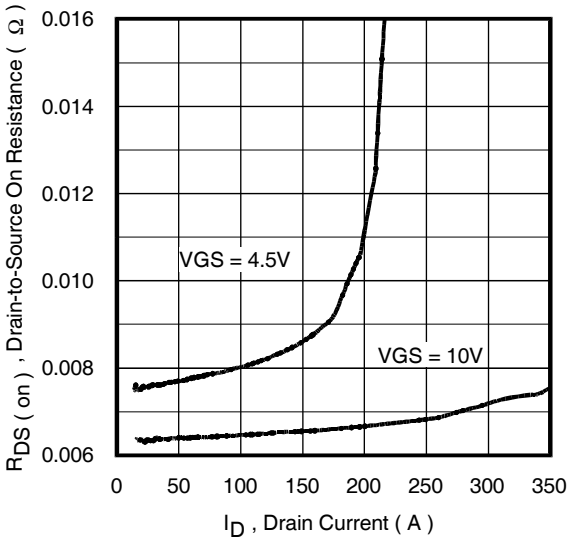



**Fig 12.** On-Resistance Vs. Drain Current

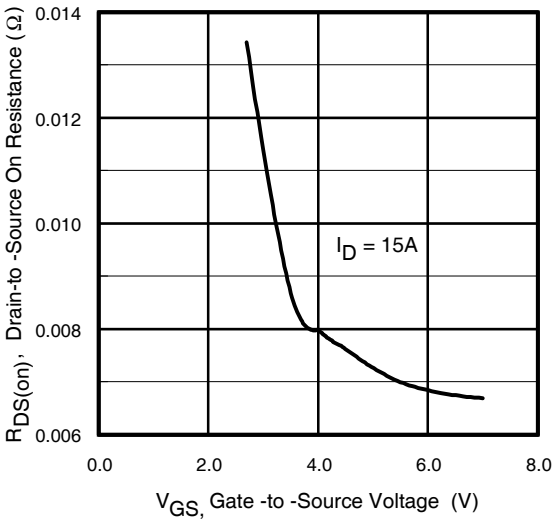
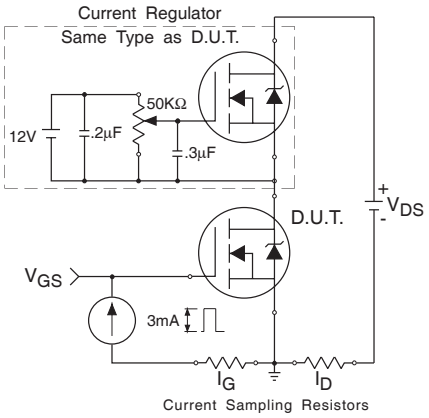



**Fig 13.** On-Resistance Vs. Gate Voltage



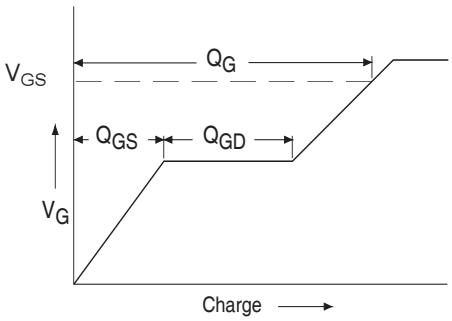
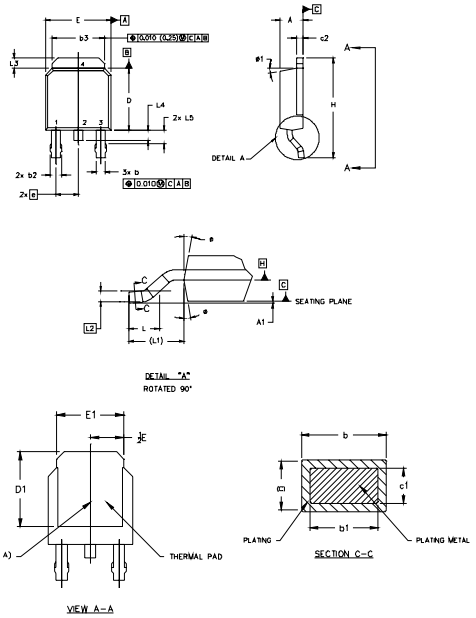




**Fig 14a&b.** Basic Gate Charge Test Circuit and Waveform

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)




NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.0 LEAD DIMENSION UNCONTROLLED IN L5.
4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | | 0.13 | | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | 5 |
| b1 | 0.64 | 0.79 | .025 | 0.031 | 5 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | |
| c | 0.46 | 0.61 | .018 | .024 | 5 |
| c1 | 0.41 | 0.56 | .016 | .022 | 5 |
| c2 | .046 | 0.89 | .018 | .035 | 5 |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | | 4 |
| e | 2.29 | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 REF. | | .108 REF. | | |
| L2 | 0.051 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | |
| L4 | | 1.02 | | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| ø | 0° | 10° | 0° | 10° | |
| ø1 | 0° | 15° | 0° | 15° | |

LEAD ASSIGNMENTS

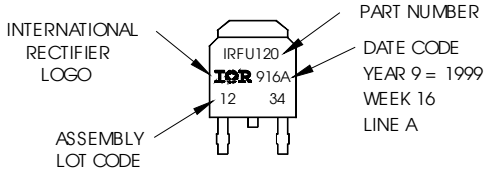
HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

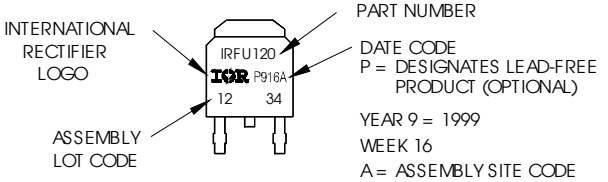
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

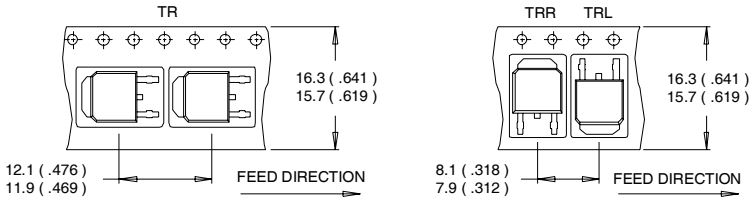



OR

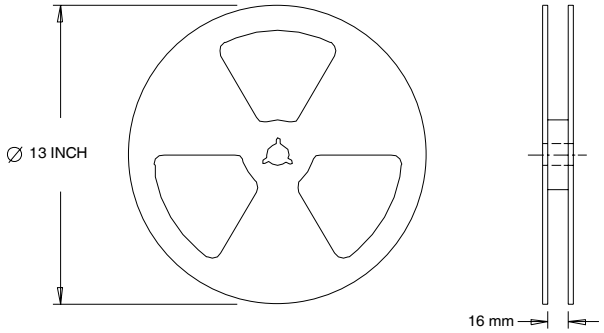


## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.



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