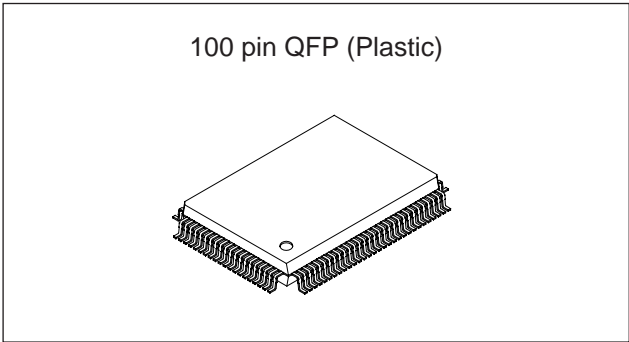


**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP82220/82224 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, fluorescent display tube controller/driver, remote control reception circuit, CTL duty detection circuit, 14-bit PWM output, high-speed output circuit and other servo systems besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP82220/82224 also provides power-on reset function and sleep/stop function that enables lower power consumption.



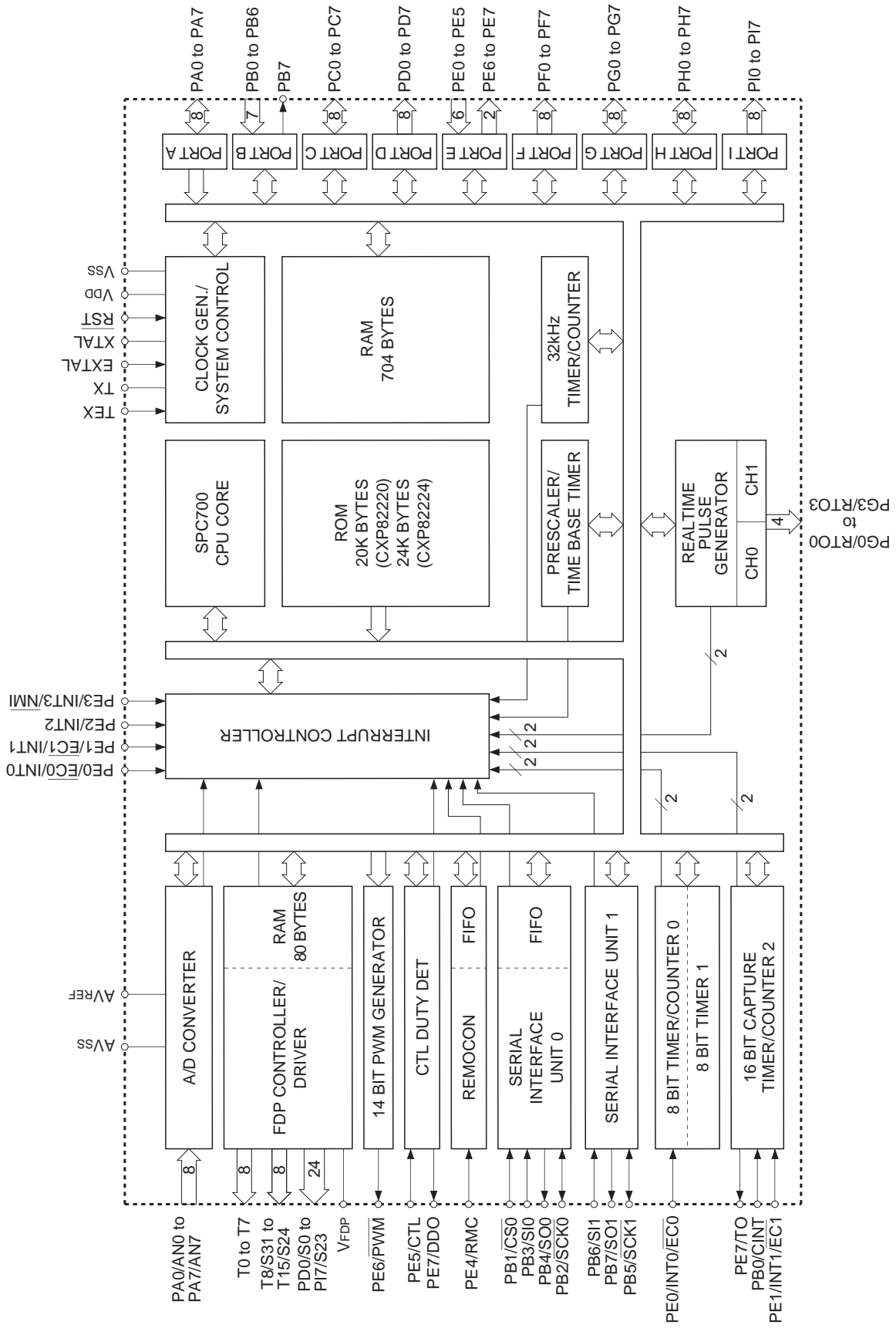
**Structure**  
Silicon gate CMOS IC

**Features**

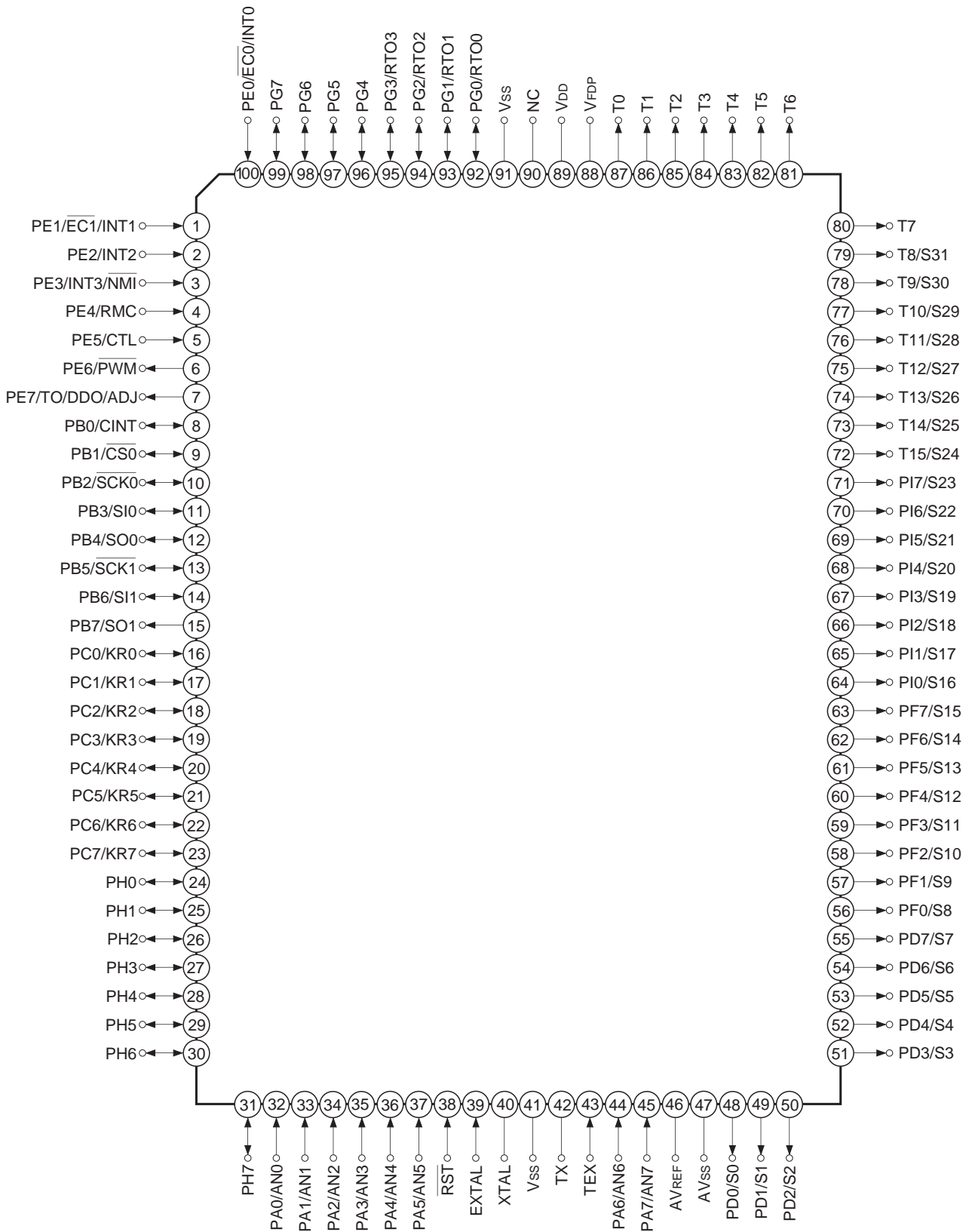
- Wide-range instruction system (213 instructions) to cover various types of data
  - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
  - 400ns at 10MHz operation
  - 122µs at 32kHz operation
- Incorporated ROM capacity
  - 20K bytes (CXP82220)
  - 24K bytes (CXP82224)
- Incorporated RAM capacity
  - 704 bytes (including fluorescent display area)
- Peripheral functions
  - A/D converter
    - 8 bits, 8 channels, successive approximation method (Conversion time of 32µs/10MHz)
  - Serial interface
    - SIO with 8-bit, 8-stage FIFO incorporated for data use (Auto transfer for 1 to 8 bytes), 1 channel
    - 8-bit standard SIO, 1 channel
  - Timer
    - 8-bit timer, 8-bit timer/counter, 19-bit time base timer
    - 16-bit capture timer/counter, 32kHz timer/counter
  - Fluorescent display tube controller/driver
    - Maximum of 384 segment display possible
    - 1 to 16-digit dynamic display
    - Dimmer function
    - High voltage drive output (40V)
    - Incorporated pull-down resistor (Mask option)
    - Hardware key scan function
    - Maximum of 16 × 8 key matrix compatible
    - Incorporated noise elimination circuit
    - Incorporated 8-bit, 6-stage FIFO for measurement data
    - 14 bits, 1 channel
  - Remote control reception circuit
    - Precision of 800ns at 10MHz, 4 outputs
  - PWM output circuit
    - 19 factors, 15 vectors, multi-interruption possible
  - CTL duty detection circuit
    - Sleep/stop
  - High-speed output circuit
    - 100-pin plastic QFP
- Interruption
  - 19 factors, 15 vectors, multi-interruption possible
- Standby mode
  - Sleep/stop
- Package
  - 100-pin plastic QFP
- Piggyback/evaluation chip
  - CXP82200 100-pin ceramic QFP

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Block Diagram



Pin Assignment (Top View)



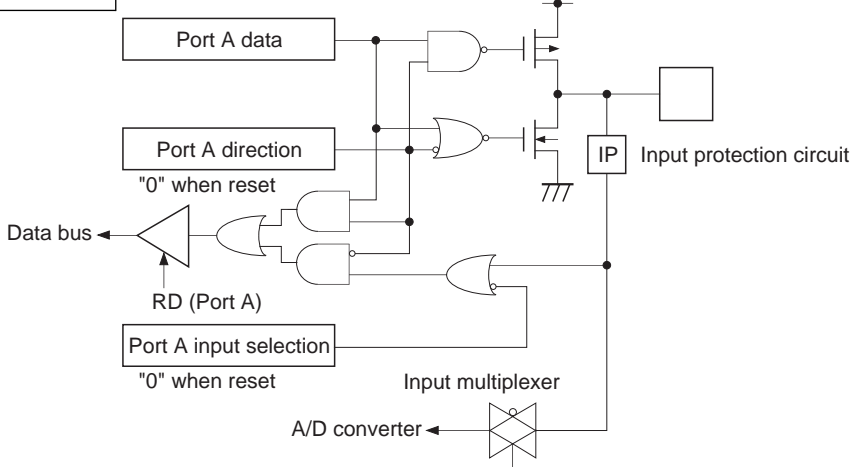
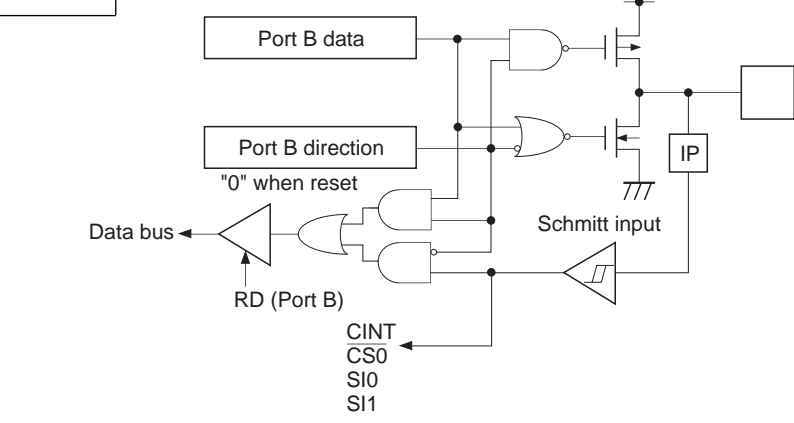
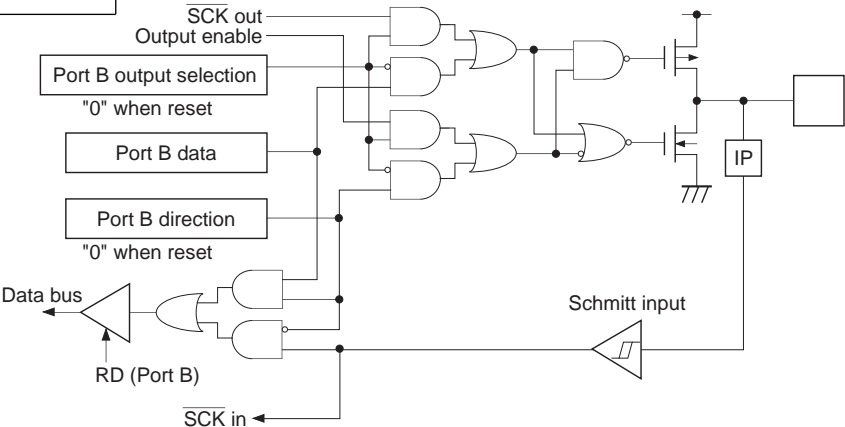
**Note** NC (Pin 90) must be connected to VDD.

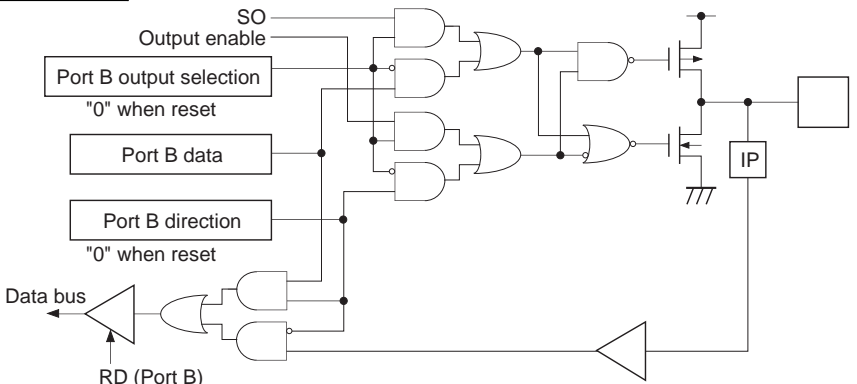
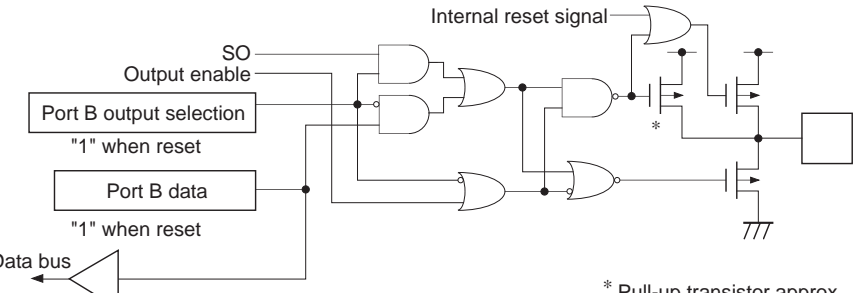
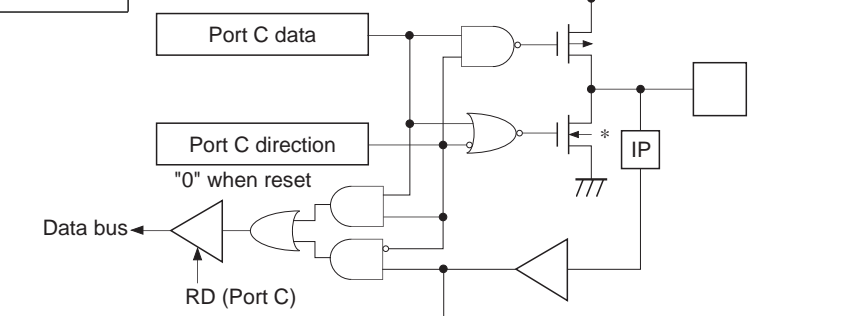
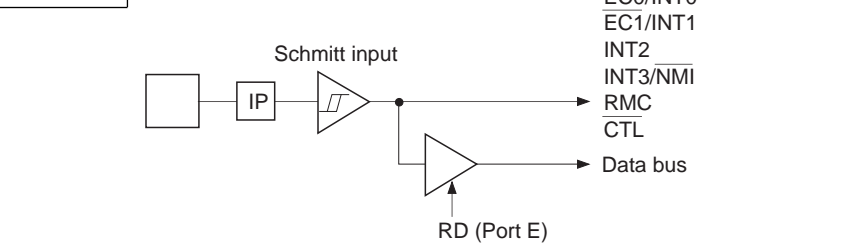
Pin Description

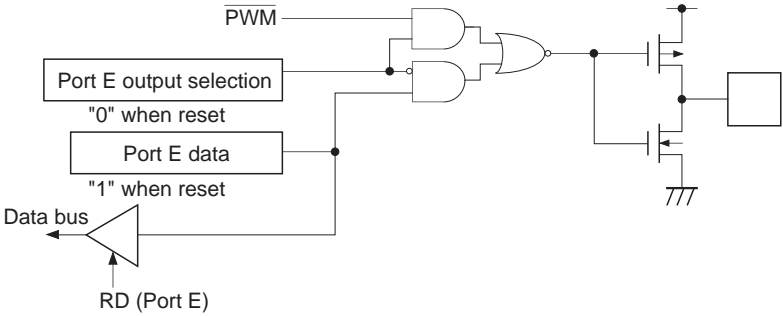
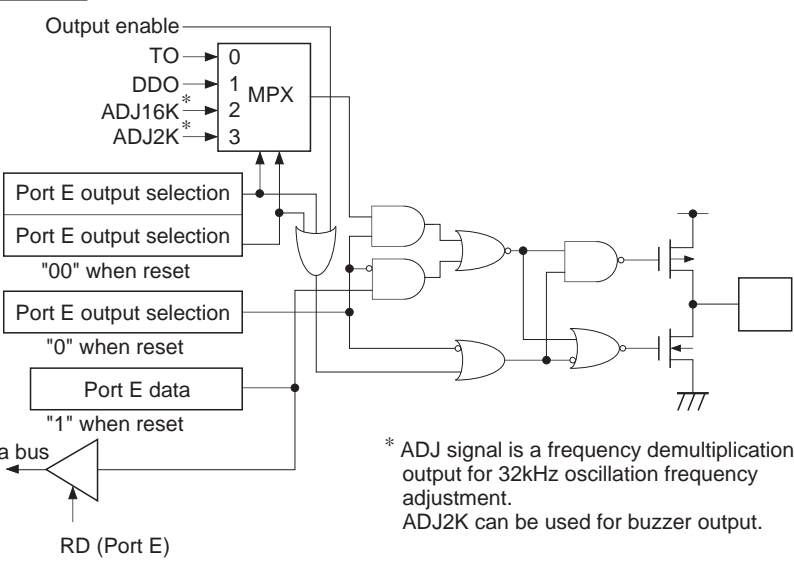
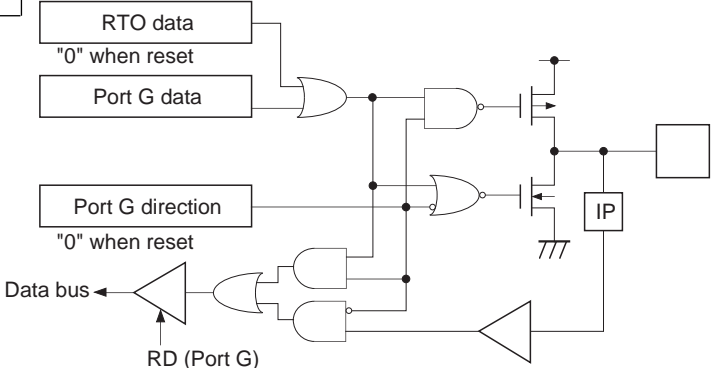
Symbol	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bit . (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O for lower 7 bits can be set in a unit of single bit. Uppermost bit (PB7) is for output only. (8 pins)	External capture input to 16bit timer/counter.	
PB1/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	Output/Output		Serial data output (CH1).	
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA synk current. (8 pins)	Serves as key return inputs when operating key scan with FDP segment signal.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PE0/INT0/ $\overline{\text{EC0}}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter. (2 pins)
PE1/INT1/ $\overline{\text{EC1}}$	Input/Input/Input			Remote control reception circuit input.
PE2/INT2	Input/Input			
PE3/INT3/ $\overline{\text{NMI}}$	Input/Input/Input			
PE4/RMC	Input/Input			
PE5/CTL	Input/Input		Input for CTL duty detection circuit.	
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output.	
PE7/TO/DDO/ ADJ	Output/Output/ Output/Output	Output for the 16-bit timer/counter rectangular waves, CTU duty detection, and 32kHz oscillation frequency demultiplication.		
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PG0/RTO0 to PG3/RTO3	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bit. Data for the lower 4 bits are gated with the contents of RTO or OR-gate output. (8 pins)	Outputs for real-time pulse generator (RTG). Functions as high-precision, real-time pulse output port. (4 pins)	
PG4 to PG7	I/O	(8 pins)		

Symbol	I/O	Functions	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bit. (8 pins)	
PI0/S16 to PI7/S23	Output/Output	(Port I) 8-bit output ports. (8 bits)	FDP segment signal outputs.
T8/S31 to T15/S24	Output/Output	Outputs for FDP timing (digit) signals/segment signals.	
T0 to T7	Output	FDP timing signal outputs.	
V <sub>FDP</sub>		FDP voltage supply when incorporated resistor is set by mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. Set 32kHz crystal oscillator between TEX and TX. For usage as event input, attach clock source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
NC		NC. Under normal operation, connect to V <sub>DD</sub> .	
AV <sub>REF</sub>	Input	Reference voltage input for A/D converter.	
AV <sub>SS</sub>		A/D converter GND.	
V <sub>DD</sub>		Positive power supply.	
V <sub>SS</sub>		GND.	

Input/Output Circuit Formats for Pins

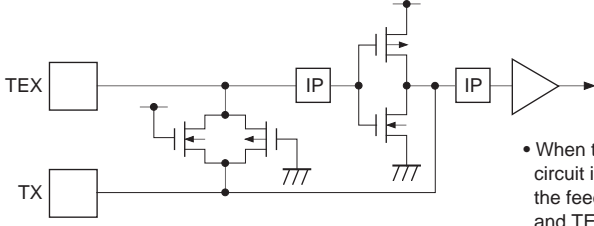
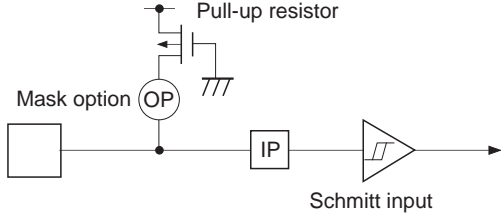
Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p>  <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP Input protection circuit</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p>  <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>IP</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p>  <p>SCK out Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p> 	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 10kΩ</p>	<p>High level</p>
<p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p>	<p>Port C</p>  <p>* Large current drive of 12mA possible</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{EC0}}</math>/INT0 PE1/<math>\overline{\text{EC1}}</math>/INT1 PE2/INT2 PE3/INT3/<math>\overline{\text{NMI}}</math> PE4/RMC PE5/CTL</p> <p>6 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE6/PWM</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PE7/TO/ DDO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>* ADJ signal is a frequency demultiplication output for 32kHz oscillation frequency adjustment. ADJ2K can be used for buzzer output.</p>	<p>High level</p>
<p>PG0/RTO0 to PG3/RTO3</p> <p>4 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>



Pin	Circuit format		When reset
PG4 to PG7 PH0 to PH7  12 pins	Port G Port H	<p>Port G or Port H data</p> <p>Port G or Port H direction "0" when reset</p> <p>Data bus</p> <p>RD (Port G or Port H)</p>	Hi-Z
PD0/S0 to PD7/S7  PF0/S8 to PF7/S15  PI0/S16 to PI7/S23 24 pins	Port D Port F Port I	<p>Segment output data</p> <p>Output selection control signal "0" when reset</p> <p>Port D, F, or I data "0" when reset</p> <p>Data bus</p> <p>RD (Port D, F, or I)</p> <p>* High voltage drive transistor</p> <p>Pull-down resistor</p> <p>Mask option</p> <p>VFD</p>	Hi-Z or Low level (when PD resistance is added)
T15/S24 to T8/S31  T0 to T7  16 pins	<p>Segment output data</p> <p>Output selection control signal "0" when reset</p> <p>Pull-down resistor</p> <p>Mask option</p> <p>VFD</p> <p>* High voltage drive transistor</p>		Hi-Z or Low level (when PD resistance is added)
EXTAL XTAL  2 pins	<p>EXTAL</p> <p>XTAL</p> <p>IP</p> <p>IP</p> <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>		Oscillation

Pin	Circuit format	When reset
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option (OP)</p> <p>Schmitt input</p>	<p>Low level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	A <sub>VSS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Display output voltage	V <sub>OD</sub>	V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V	As P channel transistor is open drain, V <sub>DD</sub> is reference.
High level output current	I <sub>OH</sub>	-5	mA	All pins excluding display outputs* <sup>2</sup> (value per pin)
	I <sub>ODH1</sub>	-15	mA	Display outputs S0 to S23 (value per pin)
	I <sub>ODH2</sub>	-35	mA	Display outputs T0 to T7, and T8/S31 to T15/S24 (value per pin)
High level total output current	∑I <sub>OH</sub>	-40	mA	Total for all pins excluding display outputs
	∑I <sub>ODH</sub>	-100	mA	Total for all display outputs
Low level output current	I <sub>OL</sub>	15	mA	Port 1
	I <sub>OLC</sub>	20	mA	Large current Port 1 * <sup>3</sup>
Low level total output current	∑I <sub>OL</sub>	100	mA	Total for all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> Specifies output current of general-purpose I/O ports.

\*<sup>3</sup> The large current drive transistor is the N-CH transistor of Port C (PC).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	High-speed mode Guaranteed operation range
		3.5	5.5		Low-speed mode Guaranteed operation range
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during stop
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*1
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input*2
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL*3
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*1
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input*2
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL*3
Operating temperature	Topr	-20	+75	°C	

\*1 Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PG, PH).

\*2 Value of the following pins:  $\overline{\text{RST}}$ ,  $\overline{\text{CINT}}$ ,  $\overline{\text{CS0}}$ ,  $\overline{\text{SCK0}}$ ,  $\overline{\text{SCK1}}$ ,  $\overline{\text{EC0/INT0}}$ ,  $\overline{\text{EC1/INT1}}$ , INT2, INT3/ $\overline{\text{NMI}}$ , RMC, CTL.

\*3 Specifies only during external clock input.

## Electrical Characteristics

## DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA, PB, PC, PE6, PE7, PG, PH	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V
Low level output voltage	V <sub>OL</sub>		V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA			0.6	V
Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5		40	μA
			V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-0.5		-40	μA
	I <sub>IHT</sub>	TEX	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.1		10	μA
			V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-0.1		-10	μA
	I <sub>ILR</sub>	RST*1	V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-1.5		-400	μA
Display output current	I <sub>OH</sub>	S0 to S23	V <sub>DD</sub> = 4.5V, V <sub>OH</sub> = V <sub>DD</sub> - 2.5V	-8			mA
		S24/T15 to S31/T8 T0 to T7		-20			mA
Open drain output leakage current (P-CH Tr in off state)	I <sub>LOL</sub>	S0 to S23 S24/T15 to S31/T8 T0 to T7	V <sub>DD</sub> = 5.5V V <sub>OL</sub> = V <sub>DD</sub> - 35V V <sub>FDP</sub> = V <sub>DD</sub> - 35V			-20	μA
Pull-down resistance*2	R <sub>L</sub>	S0 to S23 S24/T15 to S31/T8 T0 to T7	V <sub>DD</sub> = 5V V <sub>FDP</sub> = V <sub>DD</sub> - 35V	60	100	270	kΩ
I/O leakage current	I <sub>Iz</sub>	PA to PC, PE, PG, PH, RST*1	V <sub>DD</sub> = 5.5V V <sub>I</sub> = 0, 5.5V			±10	μA
Supply current*3	I <sub>DD1</sub>	V <sub>DD</sub>	High-speed mode operation (1/2 frequency demultiplier clock)	20	40		mA
			V <sub>DD</sub> = 5.5V, 10MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)				
	I <sub>DD2</sub>		V <sub>DD</sub> = 3V, 32kHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 47pF)	35	100		μA
	I <sub>DDs1</sub>		Sleep mode	1.2	8		mA
			V <sub>DD</sub> = 5.5V, 10MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)				
I <sub>DDs2</sub>	V <sub>DD</sub> = 3V, 32kHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 47pF)	9	30		μA		
I <sub>DDs3</sub>	Stop mode V <sub>DD</sub> = 5.5V, termination of 10MHz and 32kHz crystal oscillation				10	μA	
Input capacity	C <sub>IN</sub>	Pins other than S0 to S31, T0 to T7, PB7, PE6, PE7, AVREF, AVSS, VFDP, VDD, VSS	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

\*1 RST specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

\*2 When incorporated pull-down resistance has been selected through mask option.

\*3 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t <sub>CR</sub> , t <sub>CF</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{\text{EC0}}$ $\overline{\text{EC1}}$	Fig. 3	t <sub>sys</sub> + 50*1			ns
Event count input clock rise time, fall time	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{\text{EC0}}$ $\overline{\text{EC1}}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t <sub>TL</sub> , t <sub>TH</sub>	TEX	Fig. 3	10			μs
Event count input clock rise time,fall time	t <sub>TR</sub> , t <sub>TF</sub>	TEX	Fig. 3			20	ms

\*1 t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t<sub>sys</sub> [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

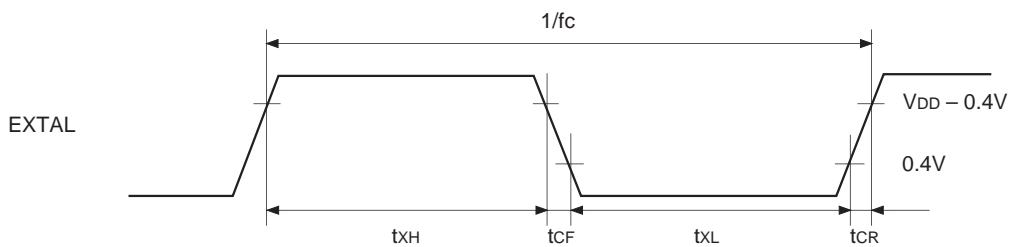


Fig. 1. Clock timing

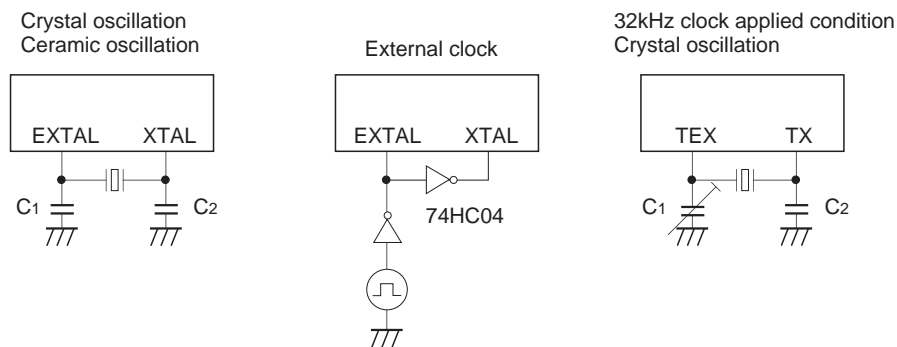


Fig. 2. Clock applied conditions

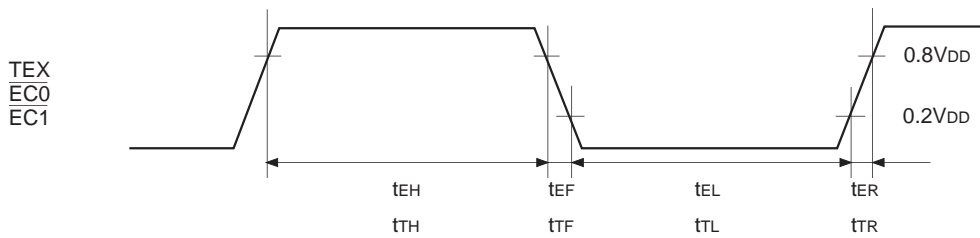


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t <sub>DCSK</sub>	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK0}$ = output mode)		t <sub>sys</sub> + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t <sub>DCSKF</sub>	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK0}$ = output mode)		t <sub>sys</sub> + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t <sub>DCSO</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t <sub>DCSOF</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{CS0}$ High level width	t <sub>WHCS</sub>	$\overline{CS0}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{SCK0}$ cycle time	t <sub>KCY</sub>	$\overline{SCK0}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t <sub>KH</sub> , t <sub>KL</sub>	$\overline{SCK0}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$ )	t <sub>SIK</sub>	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$ )	t <sub>KSI</sub>	SI0	$\overline{SCK0}$ input mode	t <sub>sys</sub> + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t <sub>KSO</sub>	SO0	$\overline{SCK0}$ input mode		t <sub>sys</sub> + 200	ns
			$\overline{SCK0}$ output mode		100	ns

**Note 1)** t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).  
 t<sub>sys</sub> [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

**Note 2)** The load condition for the  $\overline{SCK0}$  output mode, SO0 output delay time is 50pF + 1TTL.

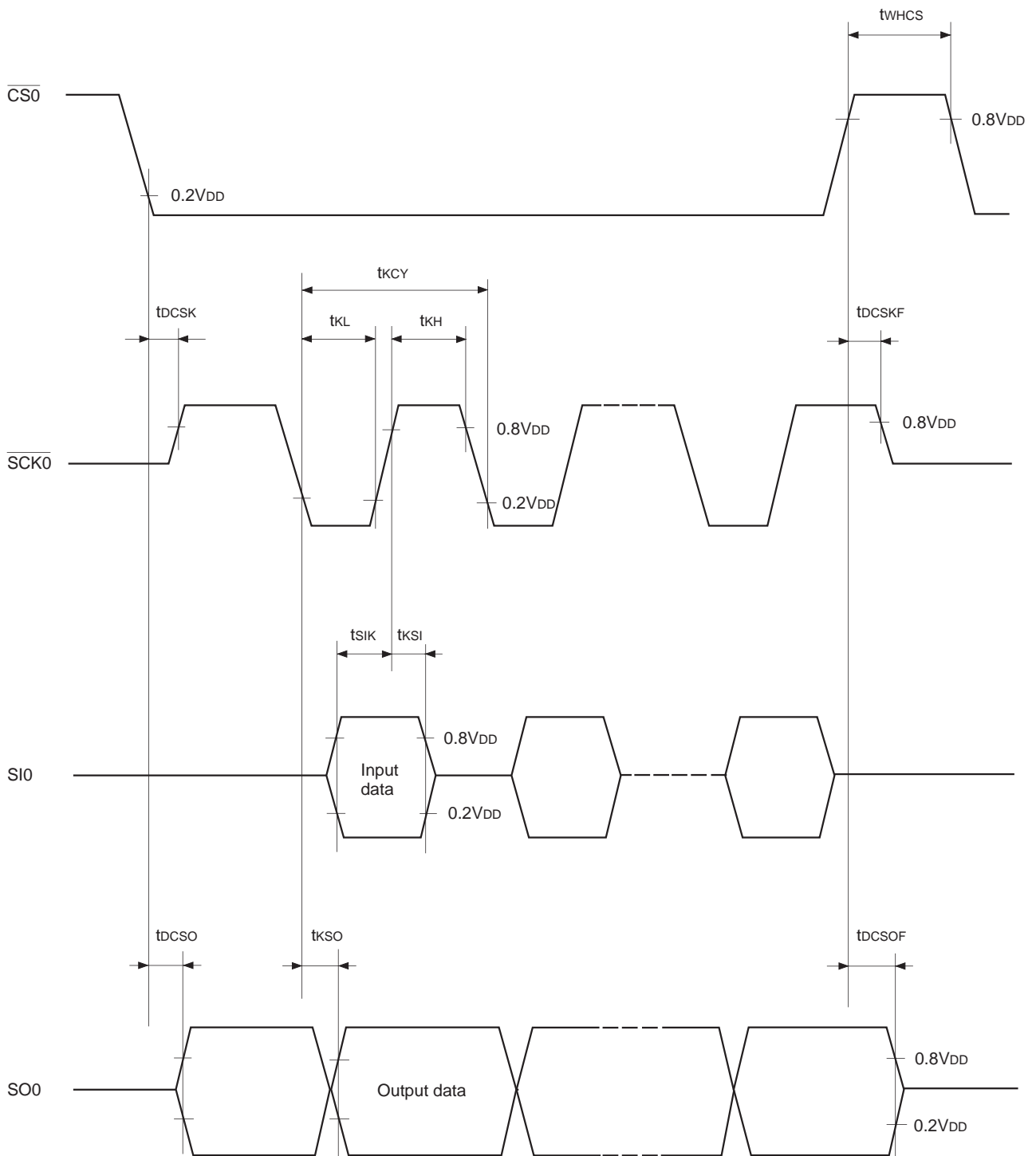


Fig. 4. Serial transfer CH0 timing

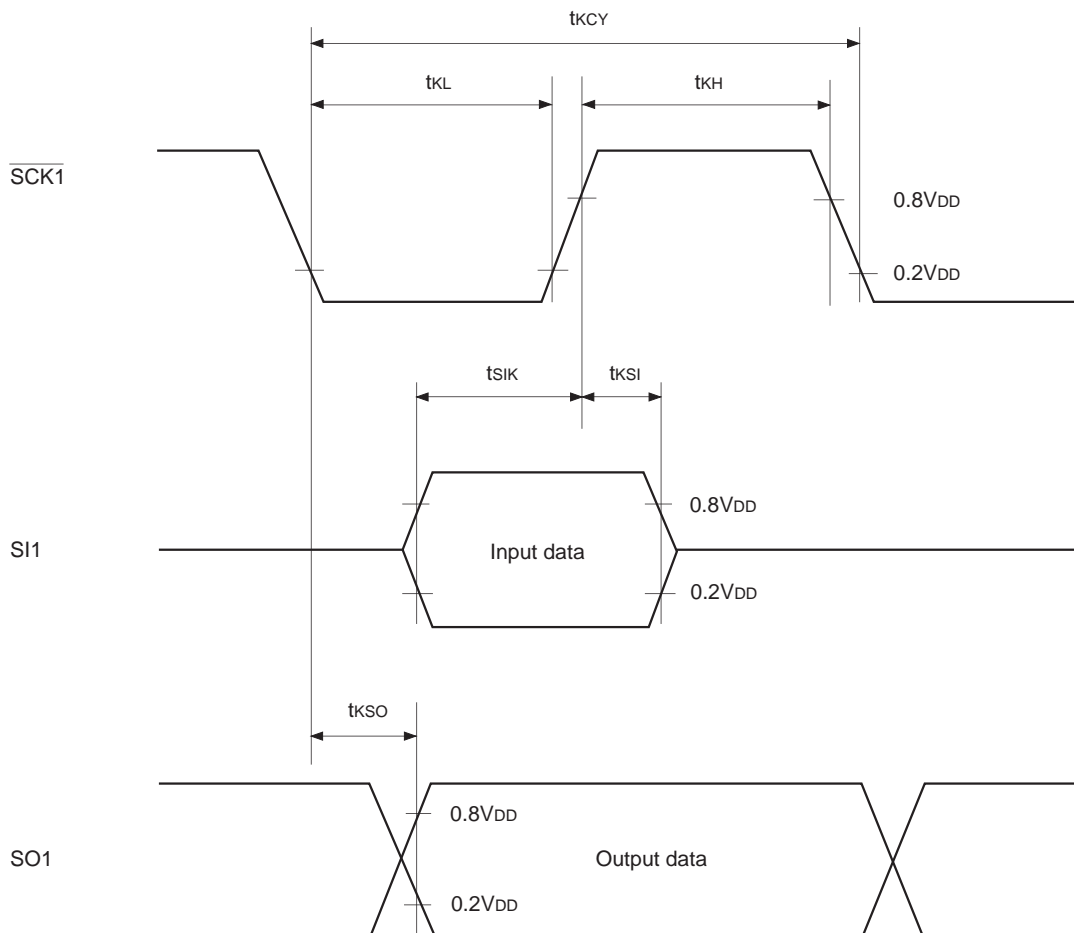


**Serial transfer (CH1)**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{CY}}$	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	$t_{\text{KH}}, t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note)** The load condition for the  $\overline{\text{SCK1}}$  output mode, SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

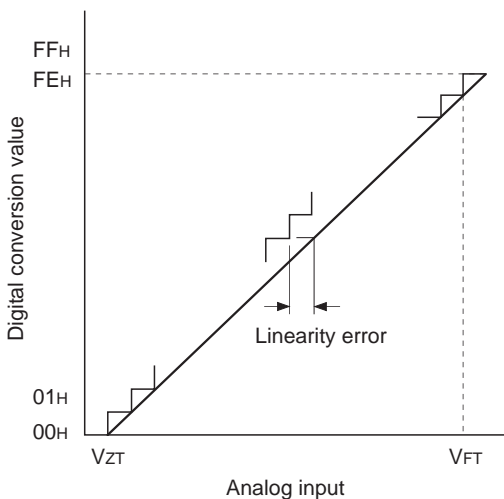


**Fig. 5. Serial transfer CH1 timing**

**(3) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						$\pm 5$	LSB
Zero transition voltage	$V_{ZT}^{*1}$		$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$	-10	70	150	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4930	5050	5120	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$		$V_{DD} - 0.5$		$V_{DD}$	V
Analog input voltage	$V_{IAN}$	$AN0$ to $AN7$		0		$AV_{REF}$	V
AVREF current	$I_{REF}$	$AV_{REF}$	Operation mode		0.6	1.0	mA
	$I_{REFS}$		Sleep mode Stop mode 32kHz operation mode			10	$\mu\text{A}$



\*1  $V_{ZT}$  : Value at which the digital conversion value changes from 00H to 01H and vice versa.

\*2  $V_{FT}$  : Value at which the digital conversion value changes from FEH to FFH and vice versa.

\*3  $f_{ADC}$  indicates the below values due to ADC operation clock selection (ADCS: Bit 6 of address 00F9H).

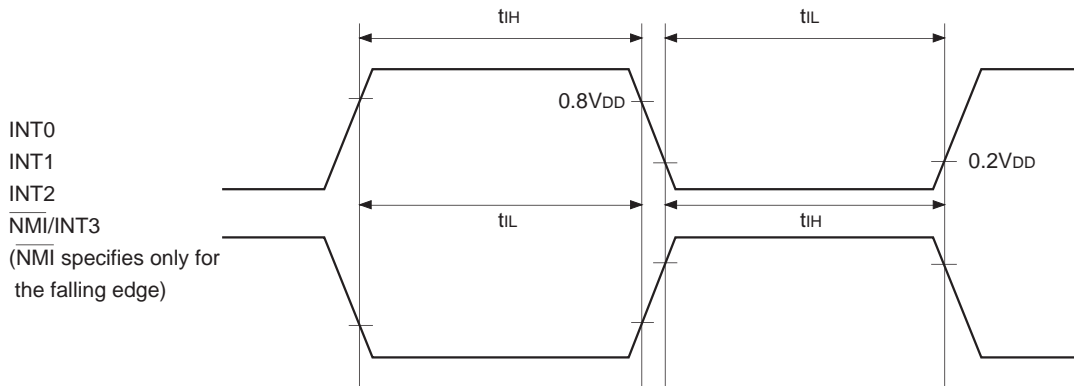
During PS2 selection,  $f_{ADC} = f_c/2$

During PS1 selection,  $f_{ADC} = f_c$

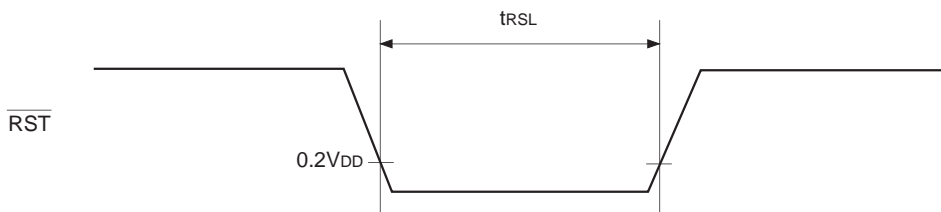
**Fig. 6. Definitions of A/D converter terms**

**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Condition	Min.	Max.	Unit
External interruption High, Low level width	t <sub>IH</sub> t <sub>IL</sub>	INT0 INT1 INT2 NMI/INT3		1		μs
Reset input Low level width	t <sub>RSL</sub>	RST		8/fc		μs



**Fig. 7. Interruption input timing**

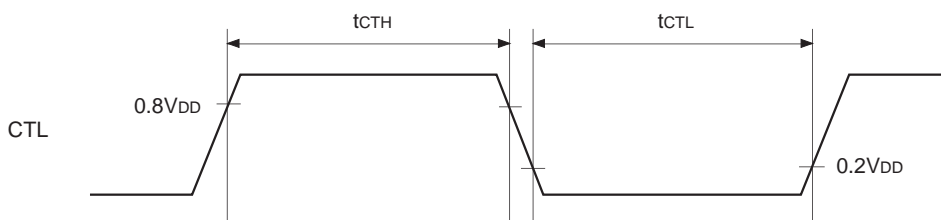


**Fig. 8. RST input timing**

**(5) Others**

(Ta = -20 to +75°C, VDD = 4.5 to 5.0V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CLK input High, Low level width	t <sub>CTH</sub> , t <sub>CTL</sub>	CTL	t <sub>sys</sub> = 2000/fc	t <sub>sys</sub> + 200		ns



**Fig. 9. Other timing**

Appendix

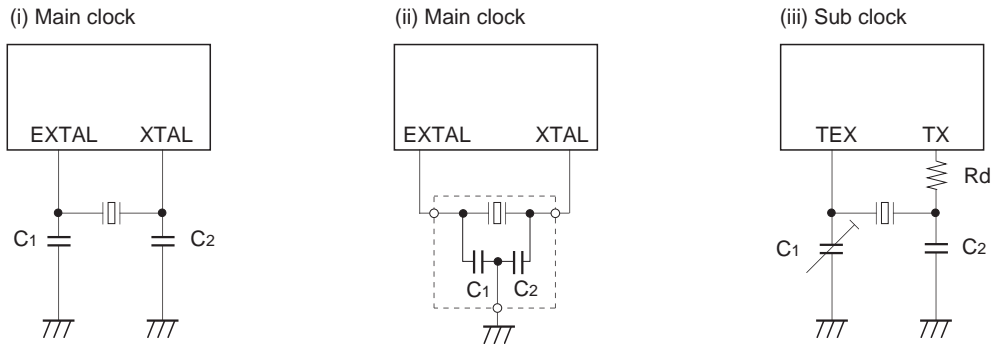


Fig. 10. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Circuit example
MURATA MFG CO., LTD	CSA4.19MG	4.19	30	30	(i)
	CSA8.00MG	8.00			
	CSA10.0MT	10.00			
	CST4.19MGW*	4.19			(ii)
	CST8.00MTW*	8.00			
	CST10.00MTW*	10.00			
RIVER ELETEC CORPORATION	HC-49/U03	4.19	15	15	(i)
		8.00			
		10.00			
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	
		8.00			
		10.00			

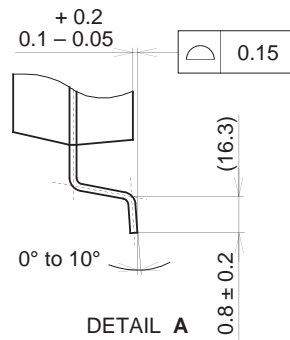
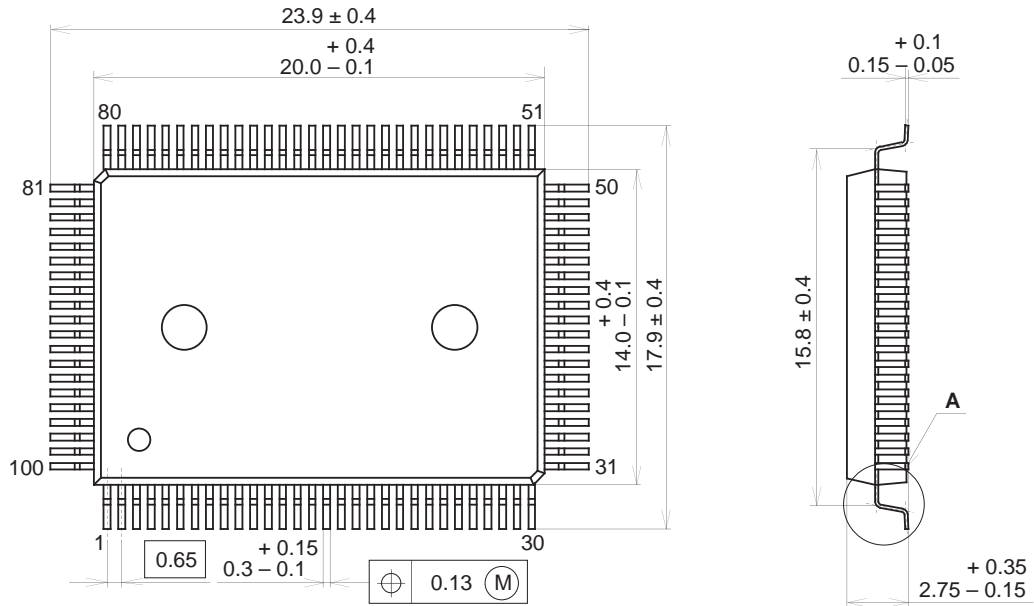
Those marked with an asterisk (\*) signify types with built-in ground capacitance (C1, C2).

Mask option table

Item	Contents	
Reset pin pull-up resistor	Non-existent	Existent
High voltage drive output port pull-down	Non-existent	Existent

Package Outline Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g