PRELIMINARY

THC63LVDM63A/THC63LVDF64A

85MHz LVDS 18 Bit COLOR HOST-LCD PANEL INTERFACE

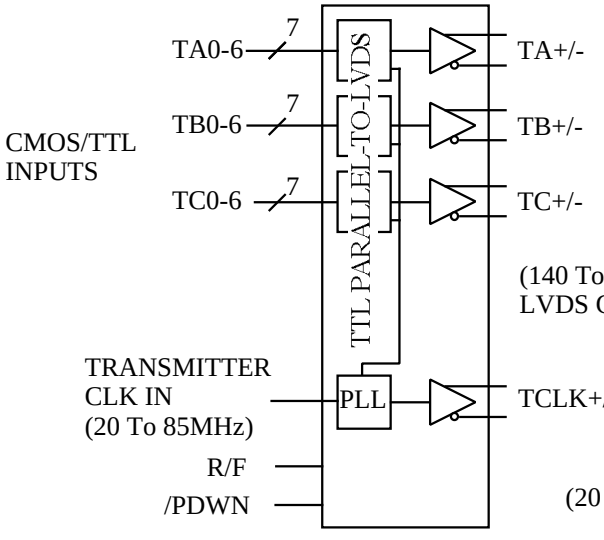
General Description

The THC63LVDM63A transmitter converts 21 bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. The THC63LVDM63A can be programmed for rising edge or falling edge clocks through a dedicated pin.
The THC63LVDF64A receiver convert the LVDS data streams back into 21 bits of CMOS/TTL data with falling edge clock. At a transmit clock frequency of 85MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (HSYNC, VSYNC, CNTL1) are transmitted at a rate of 595 Mbps per LVDS data channel.

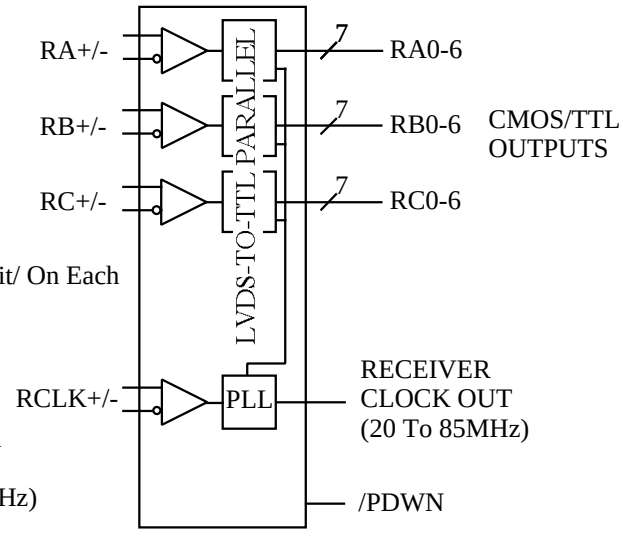
Features

- 21:3 Data channel compression at up to 223 Megabytes per sec throughput
- Wide Frequency Range: 20 - 85 MHz suited for VGA,SVGA,XGA and SXGA
- Narrow bus (8 lines) reduces cable size
- 345mV swing LVDS devices for Low EMI
- Supports Spread Spectrum Clock Generator
- On chip Input Jitter Filtering
- PLL requires No External Components
- Single 3.3V supply with 110mW(TYP)
- Low Power CMOS Design
- Power-Down Mode
- Low profile 48 Lead TSSOP Package
- Clock Edge Programmable for Transmitter
- Improved Replacement for the National DS90CF363/364

THC63LVDM63A



THC63LVDF64A



OPTIONS

CLOCK TRIGGERING	TRANSMITTER DEVICE	RECEIVER DEVICE
Falling Edge	**THC63LVDM63A(R/F pin=GND)**	**THC63LVDF64A**
Rising Edge	**THC63LVDM63A(R/F pin=Vcc)**	**----**

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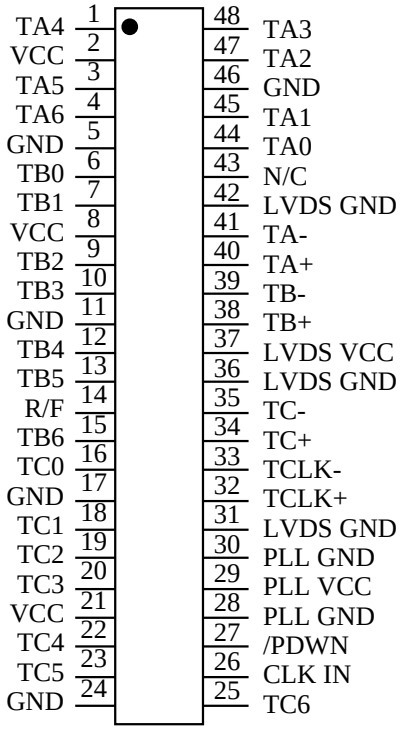
PIN OUT

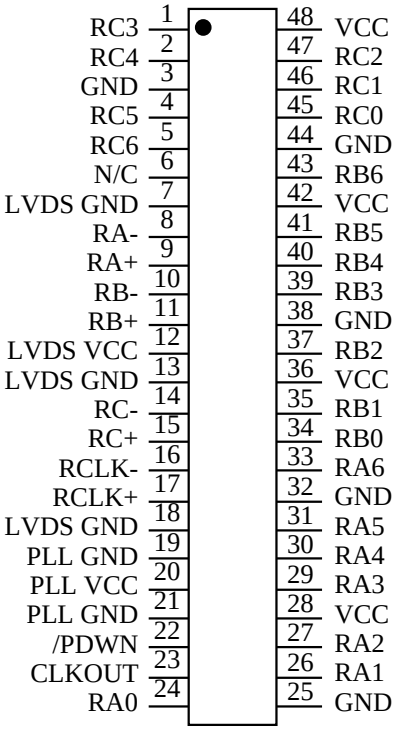
TRANSMITTER DEVICE

THC63LVDM63A



RECEIVER DEVICE

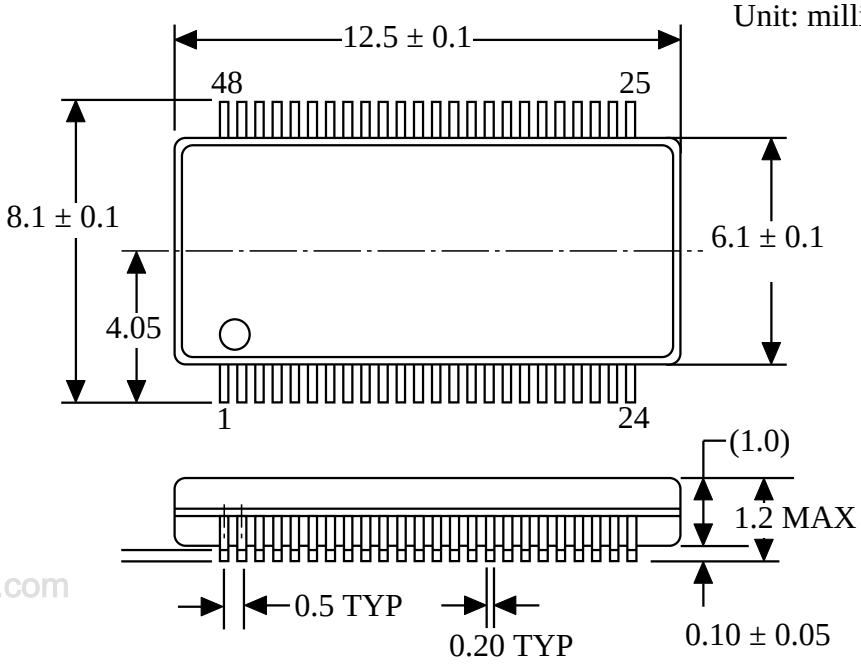
THC63LVDF64A



PACKAGE

48 Lead Molded Thin Shrink Small Outline Package, JEDEC

Unit: millimeters



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Electrical Characteristics

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level output Voltage	I_{OH}=-4mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}=4mA			0.4	V
I_{IN}	Input Current	$0V \leqq V_{IN} \leqq Vcc$			± 10	µA
I_{PD}	Pull Down Current	R/F pin,V_{IH}=Vcc			100	µA
I_{OS}	Output Short Circuit Current	V_{OUT}=0V			-50	µA
LVDS DRIVER DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	RL=100Ω	250	350	450	mV
ΔV_{OD}	Change in VOD between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in VOC between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=0V,RL=100Ω			-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=0V, V_{OUT}=0V to Vcc			±10	µA
LVDS RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential Input High Threshold	V_{OC}=+1.2V			+100	mV
V_{TL}	Differential Input low Threshold		-100			mV
I_{IN}	Input Current	V_{IN}=+2.4V/ 0V Vcc=3.6V			±10	µA

Absolute Maximum Ratings (Note 1)

Supply Voltage (Vcc)	-0.3 to +4V
CMOS/TTL Input Voltage	-0.3V to (Vcc + 0.3V)
CMOS/TTL Output Voltage	-0.3V to (Vcc + 0.3V)
LVDS Receiver Input Voltage	-0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage	-0.3V to (Vcc + 0.3V)
Output Short Circuit Duration	continuous
Junction Temperature	+150˚C
Storage Temperature Range	-65˚C to 150˚C
Lead Temperature(Soldering, 4 sec.)	+260˚C
Maximum Power Dissipation @25˚C	1.4W

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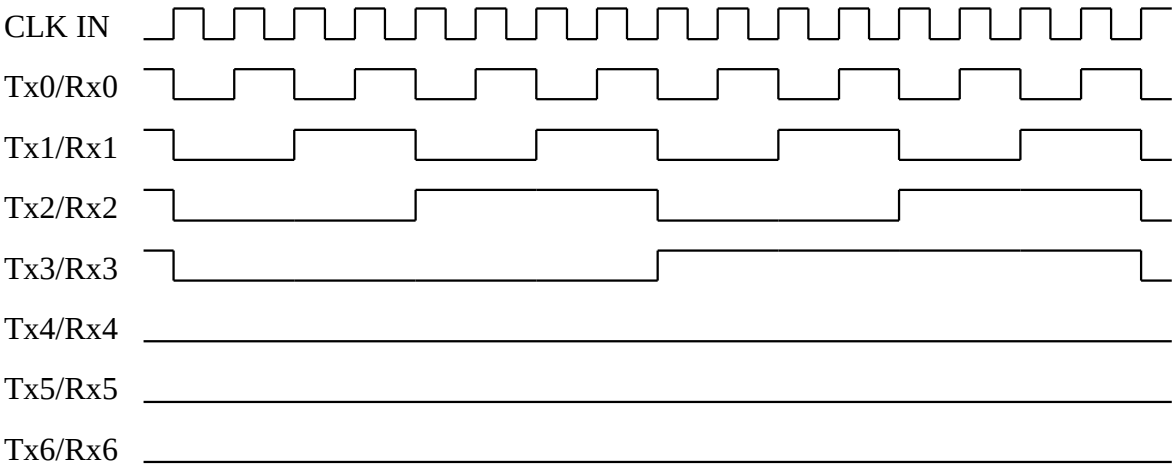
Note 1:"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not ment to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Supply Current

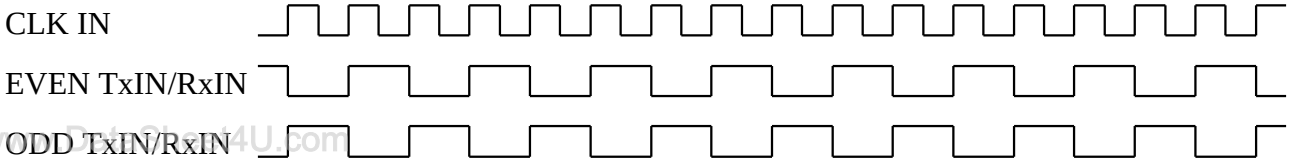
Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

SYMBOL	PARAMETER	CONDITIONS		TYP	MAX	UNITS
I_{TCCG}	Transmitter Supply Current	RL=100Ω,CL=5pF, Vcc=3.3V, 16 Grayscale Pattern	f=65MHz	33	41	mA
			f=85MHz	37	45	mA
I_{TCCW}	Transmitter Supply Current	RL=100Ω,CL=5pF, Vcc=3.3V, Worst Case Pattern	f=65MHz	35	43	mA
			f=85MHz	39	47	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN =0 V			10	µA
I_{RCCG}	Receiver Supply Current	CL=8pF, Vcc=3.3V, 16 Grayscale Pattern	f=65MHz	33	43	mA
			f=85MHz	44	54	mA
I_{RCCW}	Receiver Supply Current	CL=8pF, Vcc=3.3V, Worst Case Pattern	f=65MHz	58	75	mA
			f=85MHz	70	87	mA
I_{RCCS}	Receiver Power Down Supply Current	/PDWN =0 V			10	µA

16 Grayscale Pattern



Worst Case Pattern



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Switching Characteristics

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER					
t_{TCIT}	CLK IN Transition Time			5.0	ns
t_{TCP}	CLK IN Period	11.76	T	50.0	ns
t_{TCH}	CLK IN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLK IN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLK IN to TCLK+/- Delay		2T/7		ns
t_{TS}	TTL Data Setup to CLK IN	2.5			ns
t_{TH}	TTL Data Hold from CLK IN	2.5			ns
t_{LVT}	LVDS Transition Time		0.6	1.5	ns
t_{TOP1}	Output Data Position 0 (T=11.76ns)	-0.2	0.0	0.2	ns
t_{TOP0}	Output Data Position 1 (T=11.76ns)	T/7-0.2	T/7	T/7+0.2	ns
t_{TOP6}	Output Data Position 2 (T=11.76ns)	2T/7-0.2	2T/7	2T/7+0.2	ns
t_{TOP5}	Output Data Position 3 (T=11.76ns)	3T/7-0.2	3T/7	3T/7+0.2	ns
t_{TOP4}	Output Data Position 4 (T=11.76ns)	4T/7-0.2	4T/7	4T/7+0.2	ns
t_{TOP3}	Output Data Position 5 (T=11.76ns)	5T/7-0.2	5T/7	5T/7+0.2	ns
t_{TOP2}	Output Data Position 6 (T=11.76ns)	6T/7-0.2	6T/7	6T/7+0.2	ns
t_{TPLL}	Phase Lock Loop Set			10.0	ms
RECEIVER					
t_{RCP}	CLK OUT Period	11.76	T	50.0	ns
t_{RCH}	CLK OUT High Time		4T/7		ns
t_{RCL}	CLK OUT Low Time		3T/7		ns
t_{RCD}	RCLK+/- to CLK OUT Delay		5T/7		ns
t_{RS}	TTL Data Setup to CLK OUT	3T/7-2.5			ns
t_{RH}	TTL Data Hold from CLK OUT	4T/7-3.5			ns
t_{TLH}	TTL Low to High Transition Time		3.0	5.0	ns
t_{THL}	TTL High to Low Transition Time		3.0	5.0	ns
t_{RIP1}	Input Data Position 0 (T=11.76ns)	-0.4	0.0	0.4	ns
t_{RIP0}	Input Data Position 1 (T=11.76ns)	T/7-0.4	T/7	T/7+0.4	ns
t_{RIP6}	Input Data Position 2 (T=11.76ns)	2T/7-0.4	2T/7	2T/7+0.4	ns
t_{RIP5}	Input Data Position 3 (T=11.76ns)	3T/7-0.4	3T/7	3T/7+0.4	ns
t_{RIP4}	Input Data Position 4 (T=11.76ns)	4T/7-0.4	4T/7	4T/7+0.4	ns
t_{RIP3}	Input Data Position 5 (T=11.76ns)	5T/7-0.4	5T/7	5T/7+0.4	ns
t_{RIP2}	Input Data Position 6 (T=11.76ns)	6T/7-0.4	6T/7	6T/7+0.4	ns
t_{RPLL}	Phase Lock Loop Set			10	ms

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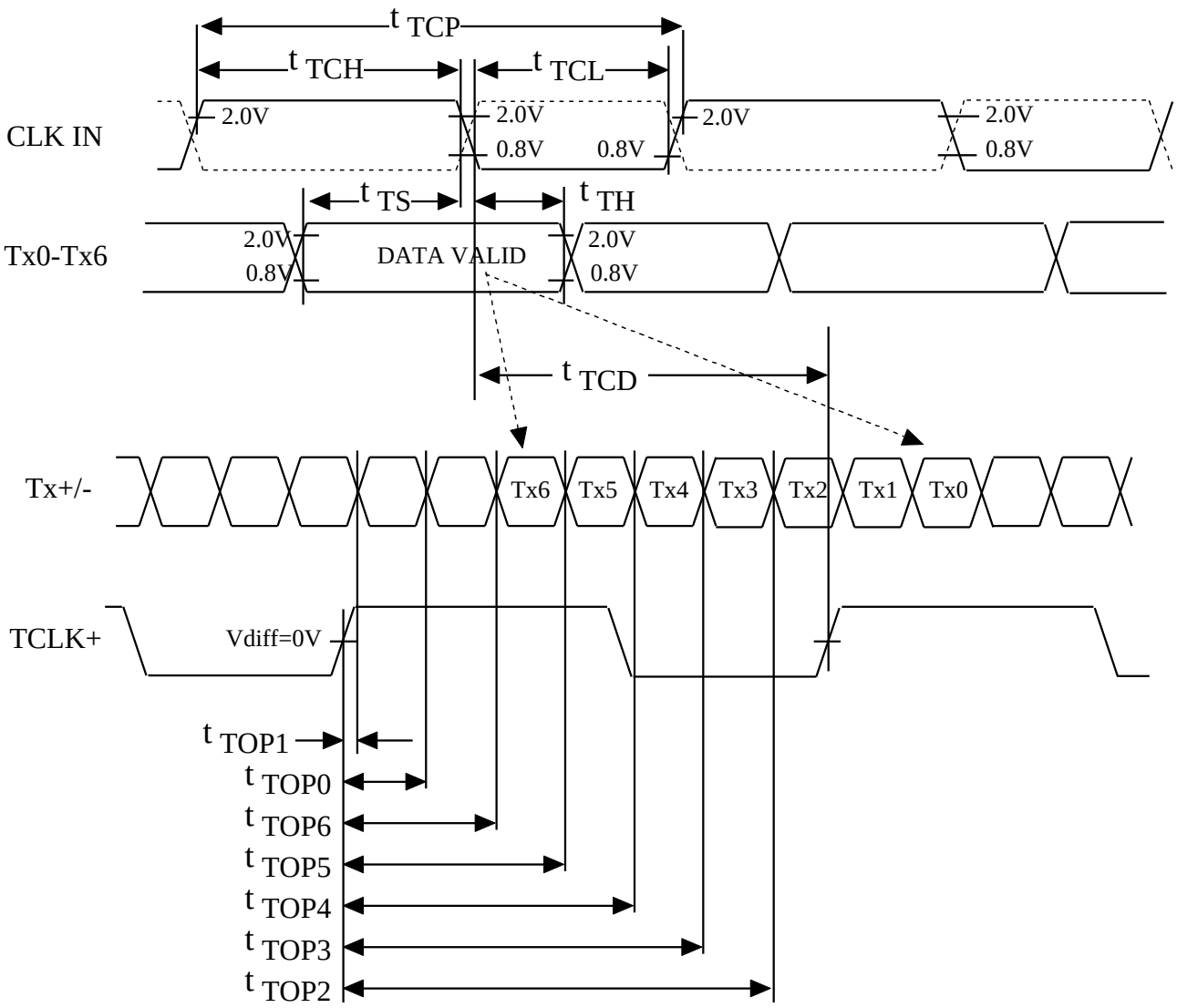
AC TIMING DIAGRAMS

TRANSMITTER DEVICE



Note:
1) CLK IN: for THC63LVDM63A(R/F=GND), denoted as solid line,
for THC63LVDM63A(R/F=Vcc), denoted as dashed line
2) Vdiff = (TA+) - (TA-), ... (TCLK+) - (TCLK-)

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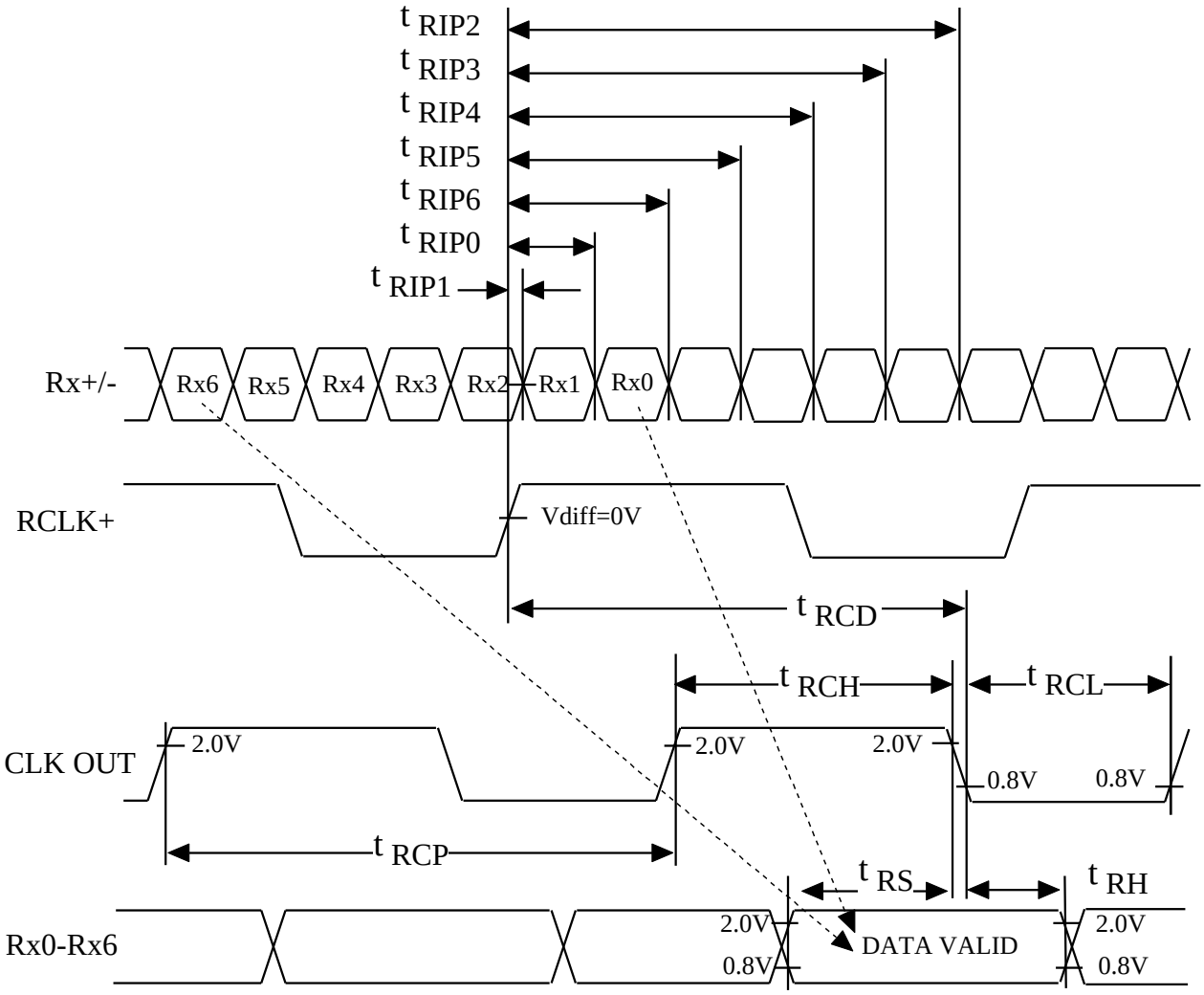
AC TIMING DIAGRAMS

RECEIVER DEVICE



Note:
1) Vdiff = (RA+) - (RA-), ... (RCLK+) - (RCLK-)

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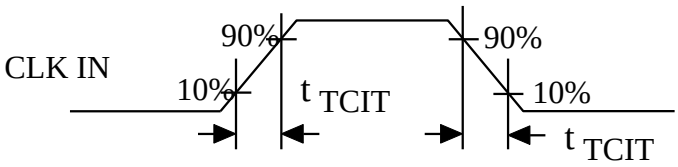
AC TIMING DIAGRAMS

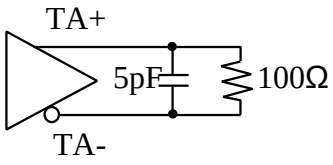
TRANSMITTER DEVICE TRANSITION TIMES

TTL Input

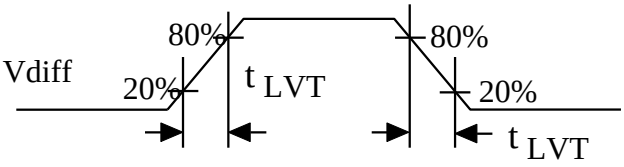


LVDS Output

Vdiff = (TA+)-(TA-)

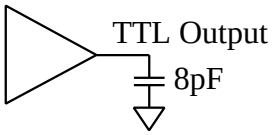


LVDS output load

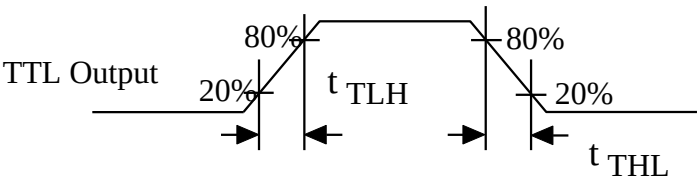


RECEIVER DEVICE TRANSITION TIMES

TTL Output

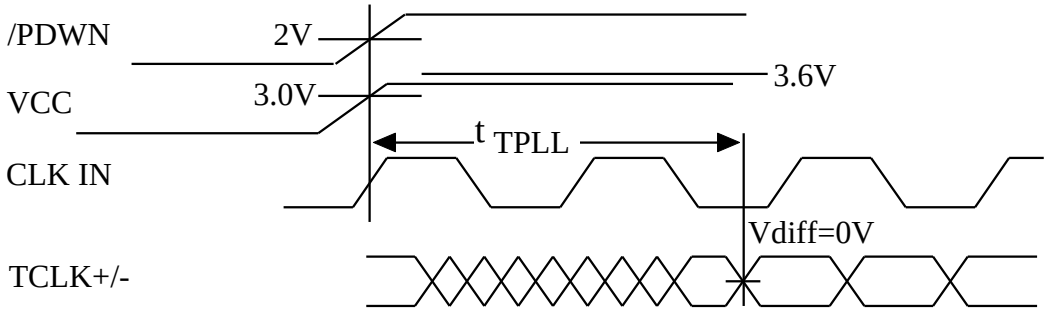


TTL output load

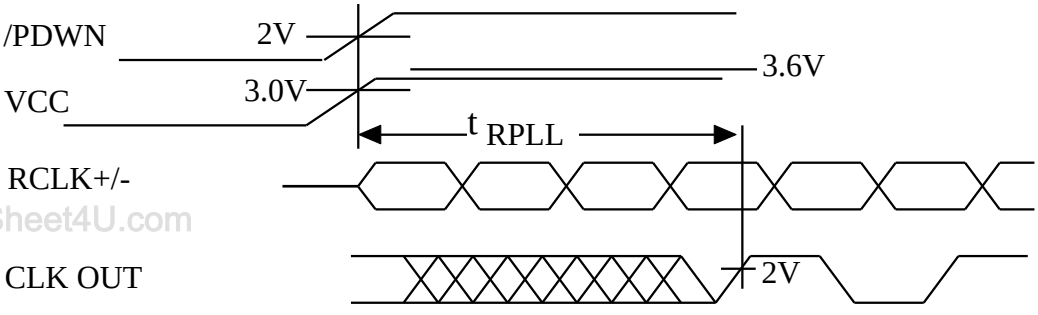


PHASE LOCK LOOP SET TIME

TRANSMITTER DEVICE



RECEIVER DEVICE



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