To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

DESCRIPTION

These are single-chip 16-bit microcomputers designed with high-performance CMOS silicon gate technology, including the internal flash memory and being packaged in 42-pin plastic molded SSOP or shrink plastic molded DIP. These microcomputers support the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set.

The CPU of these microcomputers is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of these microcomputers enhances the memory access efficiency to execute instructions fast. Therefore, these microcomputers are suitable for office, business, and industrial equipment controller that require high-speed processing of large data.

Also, they are suitable for motor-control equipment since each of them includes the motor control circuit.

For the internal flash memory, single-power-supply programming and erasure, using a PROM programmer or the control by the central processing unit (CPU), is supported. Also, each of these microcomputers has the memory area dedicated for storing a certain software which controls programming and erasure (reprogramming control software). Therefore, on these microcomputers, the program can easily be changed even after they are mounted on the board.

DISTINCTIVE FEATURES

<Microcomputer mode>

- Number of basic machine instructions 203
- Memory
  Flash memory (User ROM area) .... 60 Kbytes
  RAM ....3072 bytes
  Flash memory (Boot ROM area) .... 8 Kbytes
- Instruction execution time
  The fastest instruction at 20 MHz frequency .... 50 ns
- Single power supply .... 5 V ± 0.5 V
- Interrupts .... 5 external sources, 21 internal sources, 7 levels
- Multi-functional 16-bit timer .... 10 + 3
  (Three-phase motor drive waveform or Pulse motor drive waveform output is available.)
- Serial I/O (UART or Clock synchronous) 2
- 10-bit A-D converter .... 5-channel inputs
- 8-bit D-A converter .... 2-channel outputs
- 12-bit watchdog timer
- Programmable input/output (ports P1, P2, P5, P6, P7) 30

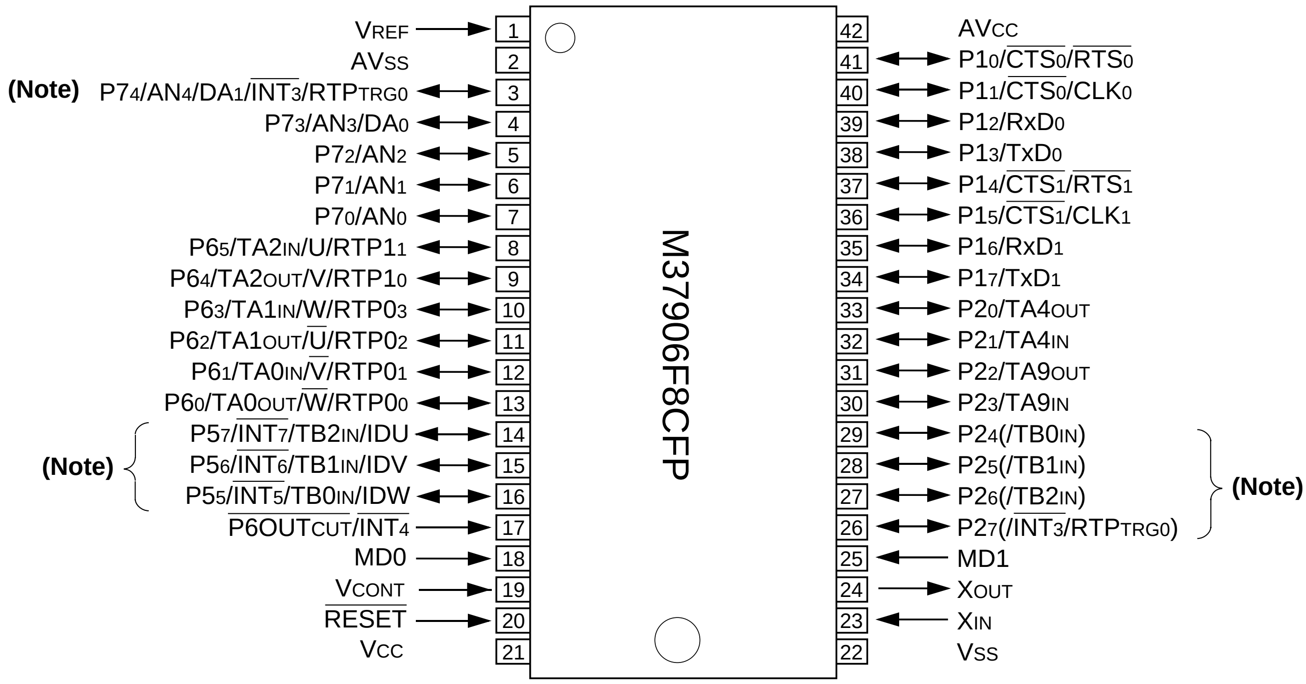
<Flash memory mode>

- Power supply voltage .... 5 V ± 0.5 V
- Programming/Erase voltage .... 5 V ± 0.5 V
- Programming method .... Programming in a unit of word
- Erase method .... Block erase or Total erase
  M37906F8CFP, M37906F8CSP
  .... 4 blocks (8 Kbytes × 2, 16 Kbytes × 1, 28 Kbytes × 1)
- Programming/Erase control by software command
- Maximum number of reprograms 100

APPLICATION

- Control devices for office equipment such as copiers and facsimiles
- Control devices for industrial equipment such as communication and measuring instruments
- Control devices for equipment, requiring motor control, such as inverter air conditioners and general-purpose inverters

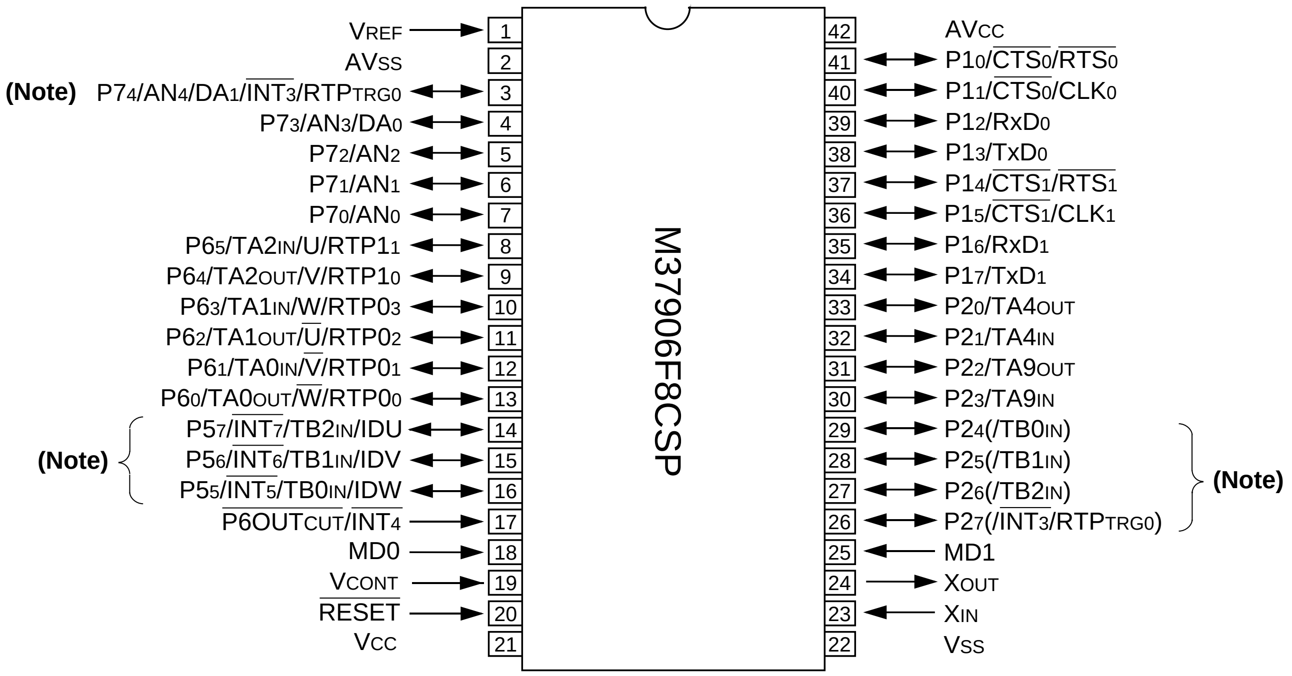
M37906F8CFP PIN CONFIGURATION (TOP VIEW)



Note: Allocation of pins $TB0_{IN}$ to $TB2_{IN}$ and $\overline{INT_3}$/RTP_{TRG0} can be switched by software.

Outline 42P2R-E

M37906F8CSP PIN CONFIGURATION (TOP VIEW)

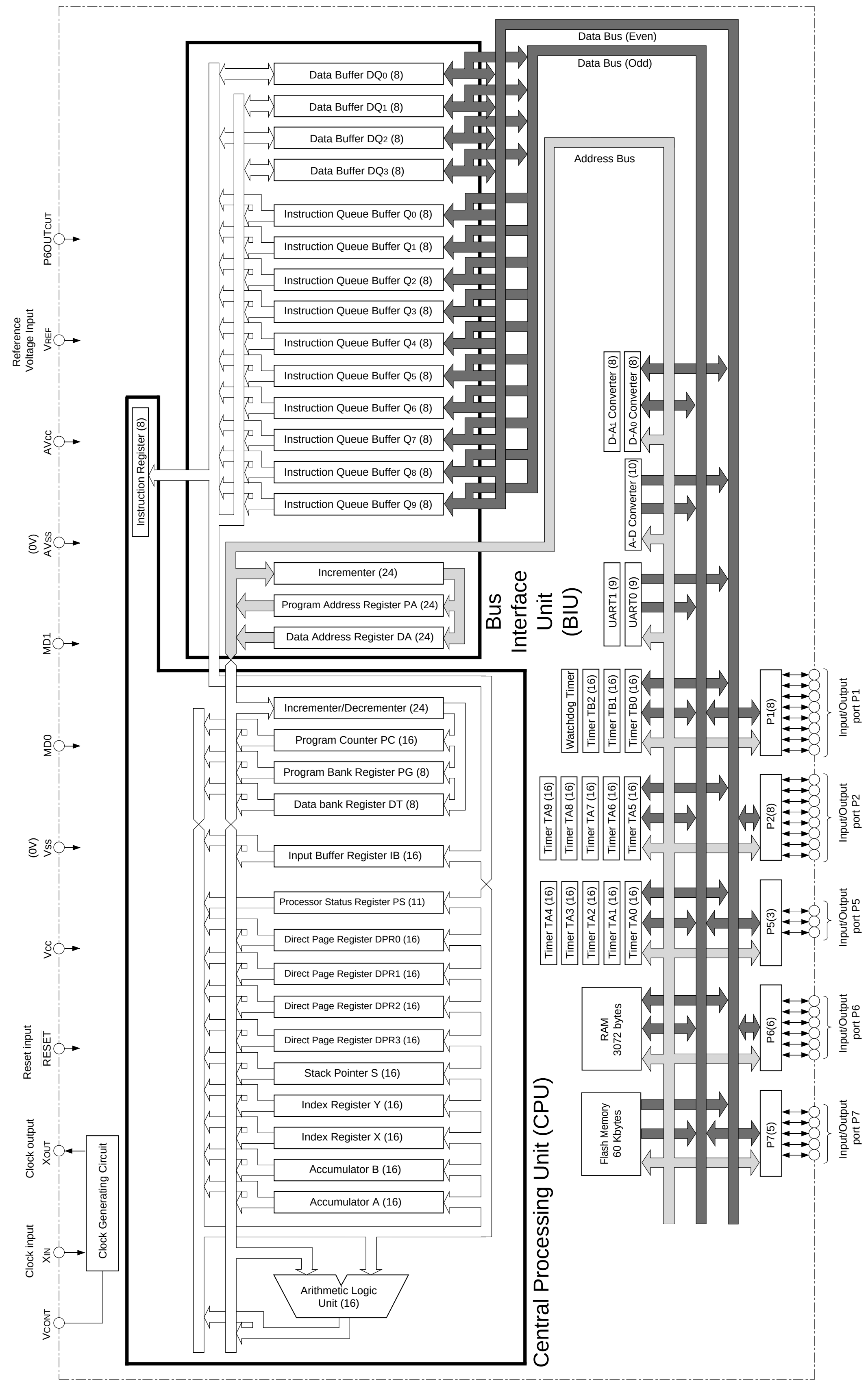


Note: Allocation of pins $TB0_{IN}$ to $TB2_{IN}$ and $\overline{INT3}$/RTP_{TRG0} can be switched by software.

Outline 42P4B

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

BLOCK DIAGRAM



RENESAS
Renesas Technology Corp.

FUNCTIONS (Microcomputer mode)

Parameter		Functions
Number of basic machine instructions		203
Instruction execution time		50 ns (the fastest instruction at f(f_{sys}) = 20 MHz)
External clock input frequency f(X_{IN})		20 MHz (Max.)
System clock input frequency f(f_{sys})		20 MHz (Max.)
Memory size	Flash memory (User ROM area)	60 Kbytes
	RAM	3072 bytes
	Flash memory (Boot ROM area)	8 Kbytes
Programmable input/output ports	P1, P2	8-bit × 2
	P5	3-bit × 1
	P6	6-bit × 1
	P7	5-bit × 1
Multi-functional timers	TA0–TA9	16-bit × 10
	TB0–TB2	16-bit × 3
Serial I/O	UART0 and UART1	(UART or Clock synchronous serial I/O) × 2
A-D converter		10-bit successive approximation method × 1 (5 channels)
D-A converter		8-bit × 2
Dead-time timer		8-bit × 3
Watchdog timer		12-bit × 1
Interrupts	Maskable interrups	5 external sources, 18 internal sources. Each interrupt can be set to a priority level within the range of 0–7 by software.
	Non-maskable interrups	3 internal sources
Clock generating circuit		Incorporated (externally connected to a ceramic resonator or quartz-crystal resonator).
PLL frequency multiplier		The following multiplication ratios are available: × 2, × 3, × 4
Power supply voltage		5 V±0.5 V
Power dissipation		125 mW (at f(f_{sys}) = 20 MHz, Typ.; the PLL frequency multiplier is inactive.)
Ports' input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Not available (single-chip mode only).
Operating ambient temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		**(Note)**

Note:

Packages	M37906F8CFP	42-pin plastic molded SSOP (42P2R-E)
	M37906F8CSP	42-pin shrink plastic molded DIP (42P4B)

FUNCTIONS (Flash memory mode)

Parameter		Functions
Power supply voltage		5 V±0.5 V
Programming/Erase voltage		5 V±0.5 V
Flash memory mode		3 modes: parallel I/O, serial I/O, and CPU reprogramming modes
Block division for erasure	User ROM area	4 blocks (8 Kbytes × 2, 16 Kbytes × 1, 28 Kbytes × 1); total of 60 Kbytes
	Boot ROM area	1 block (8 Kbytes × 1) **(Note)**
Programming method		Programmed per word
	Flash memory parallel I/O mode	User ROM area + Boot ROM area
	Flash memory serial I/O mode	User ROM area
	Flash memory CPU reprogramming mode	User ROM area
Erase method		Total erase/Block erase
	Flash memory parallel I/O mode	User ROM area + Boot ROM area
	Flash memory serial I/O mode	User ROM area
	Flash memory CPU reprogramming mode	User ROM area
Programming/Erase control		Programming/Erase control by software commands
Number of commands		6 commands
Maximum number of reprograms		100

Note: On shipment, our reprogramming control firmware for the flash memory serial I/O mode has been stored into the boot ROM area.

PIN DESCRIPTION (MICROCOMPUTER MODE)

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power supply input	—	Apply 5 V±0.5 V to Vcc, and 0 V to Vss.
MD0	MD0	Input	Connect this pin to VSS.
MD1	MD1	Input	Connect this pin to Vss.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when "L" level is applied to this pin.
XIN	Clock input	Input	These are input and output pins of the internal clock generating circuit. Connect a ceramic or quartz-crystal oscillator between the XIN and XOUT pins. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
VCONT	Filter circuit connection	—	When using the PLL frequency multiplier, connect this pin to the filter circuit. When not using the PLL frequency multiplier, this pin should be left open.
AVcc, AVss	Analog power supply input	—	Power supply input pins for the A-D converter and the D-A converter. Connect AVcc to Vcc, and AVss to Vss externally.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter and the D-A converter.
P10–P17	I/O port P1	I/O	Port P1 is an 8-bit I/O port. This port has an I/O direction register, and each pin can be programmed for input or output. These pins enter the input mode at reset. These pins also function as I/O port pins of UART0 and UART1.
P20–P27	I/O port P2	I/O	In addition to having the same functions as port P1, these pins also function as I/O pins for timers A4 and A9. By software setting, these pins also function as input pins for timers B0–B2, an input pin for $\overline{\text{INT}_3}$, and a trigger input pin in the pulse output port mode.
P50–P57	I/O port P5	I/O	In addition to having the same functions as port P1, these pins also function as input pins for $\overline{\text{INT}_5}$–$\overline{\text{INT}_7}$, input pins for timers B0–B2, and input pins for position-data-input pins in the three-phase waveform mode.
P60–P65	I/O port P6	I/O	In addition to having the same functions as port P1, these pins also function as I/O pins for timers A0–A2, and output pins for the motor drive waveform.
P70–P74	I/O port P7	I/O	In addition to having the same functions as port P1, these pins also function as input pins for the A-D converter. P73 functions as an output pin for the D-A converter; P74 functions as an output pin for the D-A converter, an input pin for $\overline{\text{INT}_3}$, and a trigger input pin in the pulse output port mode.
$\overline{\text{P6OUT}_{\text{CUT}}}$	$\overline{\text{P6OUT}_{\text{CUT}}}$ input	Input	This pin has the function to forcibly place port P6 pins in the input mode. Also, this pin functions as an input pin for $\overline{\text{INT}_4}$; and this pin is used to input a signal, which forcibly cuts off a motor drive waveform output.

PIN DESCRIPTION (FLASH MEMORY SERIAL I/O MODE)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply input	—	Apply 5 V ± 0.5 V to Vcc, and 0 V to Vss.
MD0	MD0	Input	Connect this pin to Vss.
MD1	MD1	Input	Connect this pin to Vss via a resistor of 10 kΩ to 100 kΩ.
$\overline{RESET}$	Reset input	Input	The reset input pin.
X_{IN}	Clock input	Input	Connect a ceramic oscillator between the X_{IN} and X_{OUT} pins, or input an external clock from the X_{IN} pin with the X_{OUT} pin left open.
X_{OUT}	Clock output	Output	
AVcc, AVss	Analog supply input	—	Connect AVcc to Vcc, and AVss to Vss.
V_{REF}	Reference voltage input	Input	Input an arbitrary level within the range of V_{SS}–V_{CC}. (This is not used in the flash memory serial I/O mode.)
$P1_0$–$P1_7$	Input port P1	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
$P2_0$–$P2_3$, $P2_7$	Input port P2	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
$P2_4$	SCLK input	Input	This is an input pin for a serial clock.
$P2_5$	SDA I/O	I/O	This is an I/O pin for serial data. Connect this pin to V_{CC} via a resistor (about 1 kΩ).
$P2_6$	BUSY output	Output	This is an output pin for the BUSY signal.
$\overline{P6OUT_{CUT}}$	$\overline{P6OUT_{CUT}}$ input	Input	Input “H”.
$P5_5$–$P5_7$	Input port P5	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
$P6_0$–$P6_5$	Input port P6	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
$P7_0$–$P7_4$	Input port P7	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
V_{CONT}	Filter circuit connection	—	Connect this pin to the filter circuit, or leave this pin open. (This is not used in the flash memory serial I/O mode.)

BASIC FUNCTION BLOCKS

Each of the M37906F8CFP and M37906F8CSP has the same function as that of the M37906M4C-XXXFP except for the following. Therefore, for details except for the following, refer to the datasheet of the M37906M4C-XXXFP.

- Flash memory size
- RAM size

MEMORY

Figure 1 shows the memory map.

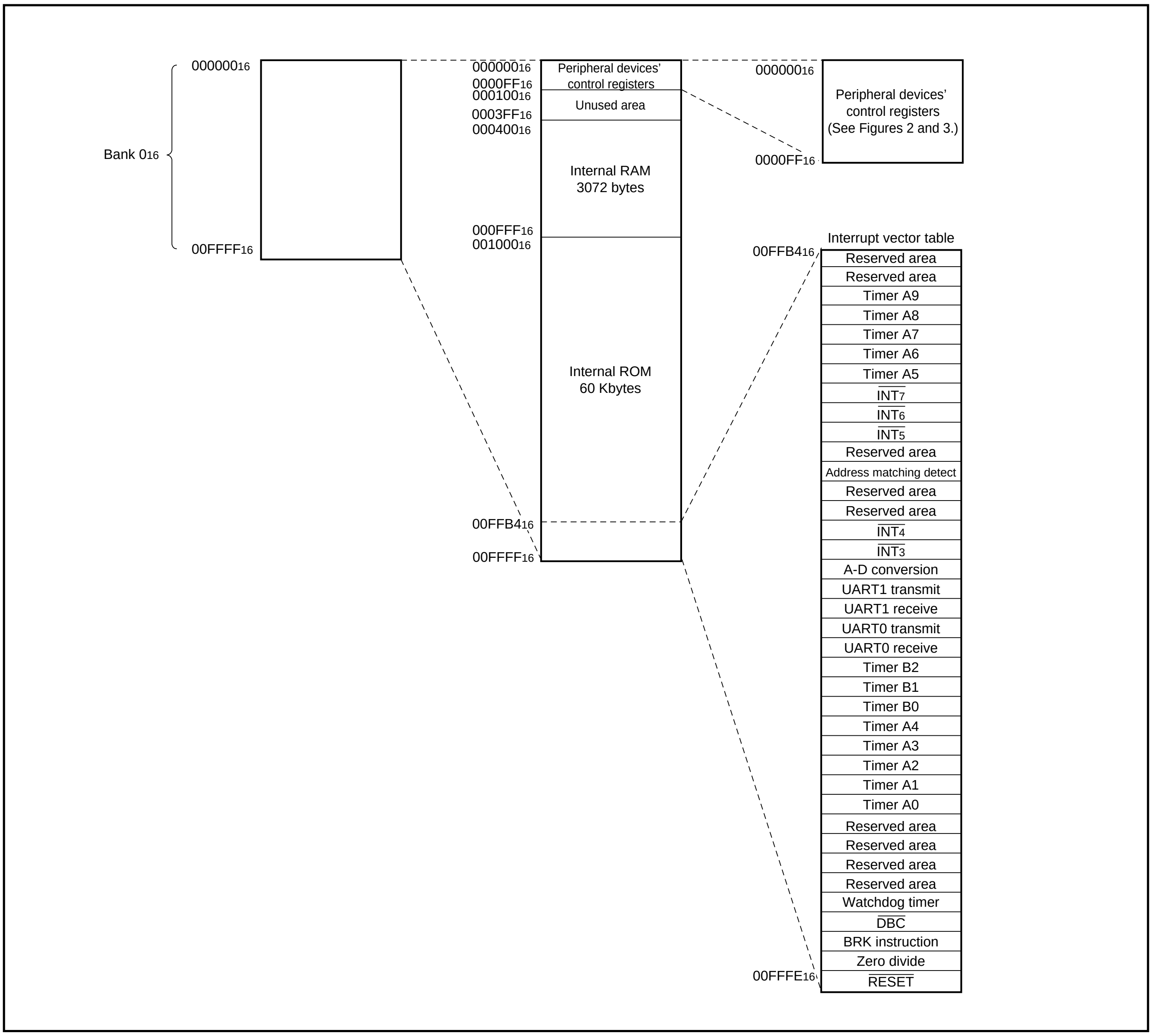


Fig. 1 Memory map of M37906F8CFP, M37906F8CSP (Single-chip mode)

Address (Hexadecimal notation)

000000$_{16}$	Reserved area **(Note)**
000001$_{16}$	Reserved area **(Note)**
000002$_{16}$	Reserved area **(Note)**
000003$_{16}$	Port P1 register
000004$_{16}$	Reserved area **(Note)**
000005$_{16}$	Port P1 direction register
000006$_{16}$	Port P2 register
000007$_{16}$	Reserved area **(Note)**
000008$_{16}$	Port P2 direction register
000009$_{16}$	Reserved area **(Note)**
00000A$_{16}$	Reserved area **(Note)**
00000B$_{16}$	Port P5 register
00000C$_{16}$	Reserved area **(Note)**
00000D$_{16}$	Port P5 direction register
00000E$_{16}$	Port P6 register
00000F$_{16}$	Port P7 register
000010$_{16}$	Port P6 direction register
000011$_{16}$	Port P7 direction register
000012$_{16}$	Reserved area **(Note)**
000013$_{16}$	
000014$_{16}$	Reserved area **(Note)**
000015$_{16}$	
000016$_{16}$	Reserved area **(Note)**
000017$_{16}$	Reserved area **(Note)**
000018$_{16}$	Reserved area **(Note)**
000019$_{16}$	Reserved area **(Note)**
00001A$_{16}$	
00001B$_{16}$	
00001C$_{16}$	
00001D$_{16}$	
00001E$_{16}$	A-D control register 0
00001F$_{16}$	A-D control register 1
000020$_{16}$ 000021$_{16}$	A-D register 0
000022$_{16}$ 000023$_{16}$	A-D register 1
000024$_{16}$ 000025$_{16}$	A-D register 2
000026$_{16}$ 000027$_{16}$	A-D register 3
000028$_{16}$ 000029$_{16}$	A-D register 4
00002A$_{16}$	Reserved area **(Note)**
00002B$_{16}$	Reserved area **(Note)**
00002C$_{16}$	Reserved area **(Note)**
00002D$_{16}$	Reserved area **(Note)**
00002E$_{16}$	Reserved area **(Note)**
00002F$_{16}$	Reserved area **(Note)**
000030$_{16}$	UART0 transmit/receive mode register
000031$_{16}$	UART0 baud rate register (BRG0)
000032$_{16}$ 000033$_{16}$	UART0 transmit buffer register
000034$_{16}$	UART0 transmit/receive control register 0
000035$_{16}$	UART0 transmit/receive control register 1
000036$_{16}$ 000037$_{16}$	UART0 receive buffer register
000038$_{16}$	UART1 transmit/receive mode register
000039$_{16}$	UART1 baud rate register (BRG1)
00003A$_{16}$ 00003B$_{16}$	UART1 transmit buffer register
00003C$_{16}$	UART1 transmit/receive control register 0
00003D$_{16}$	UART1 transmit/receive control register 1
00003E$_{16}$ 00003F$_{16}$	UART1 receive buffer register

Address (Hexadecimal notation)

000040$_{16}$	Count start register 0
000041$_{16}$	Count start register 1
000042$_{16}$	One-shot start register 0
000043$_{16}$	One-shot start register 1
000044$_{16}$	Up-down register 0
000045$_{16}$	Timer A clock division select register
000046$_{16}$ 000047$_{16}$	Timer A0 register
000048$_{16}$ 000049$_{16}$	Timer A1 register
00004A$_{16}$ 00004B$_{16}$	Timer A2 register
00004C$_{16}$ 00004D$_{16}$	Timer A3 register
00004E$_{16}$ 00004F$_{16}$	Timer A4 register
000050$_{16}$ 000051$_{16}$	Timer B0 register
000052$_{16}$ 000053$_{16}$	Timer B1 register
000054$_{16}$ 000055$_{16}$	Timer B2 register
000056$_{16}$	Timer A0 mode register
000057$_{16}$	Timer A1 mode register
000058$_{16}$	Timer A2 mode register
000059$_{16}$	Timer A3 mode register
00005A$_{16}$	Timer A4 mode register
00005B$_{16}$	Timer B0 mode register
00005C$_{16}$	Timer B1 mode register
00005D$_{16}$	Timer B2 mode register
00005E$_{16}$	Processor mode register 0
00005F$_{16}$	Processor mode register 1
000060$_{16}$	Watchdog timer register
000061$_{16}$	Watchdog timer frequency select register
000062$_{16}$	Particular function select register 0
000063$_{16}$	Particular function select register 1
000064$_{16}$	Particular function select register 2
000065$_{16}$	Reserved area **(Note)**
000066$_{16}$	Debug control register 0
000067$_{16}$	Debug control register 1
000068$_{16}$ 000069$_{16}$ 00006A$_{16}$	Address comparison register 0
00006B$_{16}$ 00006C$_{16}$ 00006D$_{16}$	Address comparison register 1
00006E$_{16}$	$\overline{\mathrm{INT}}_3$ interrupt control register
00006F$_{16}$	$\overline{\mathrm{INT}}_4$ interrupt control register
000070$_{16}$	A-D conversion interrupt control register
000071$_{16}$	UART0 transmit interrupt control register
000072$_{16}$	UART0 receive interrupt control register
000073$_{16}$	UART1 transmit interrupt control register
000074$_{16}$	UART1 receive interrupt control register
000075$_{16}$	Timer A0 interrupt control register
000076$_{16}$	Timer A1 interrupt control register
000077$_{16}$	Timer A2 interrupt control register
000078$_{16}$	Timer A3 interrupt control register
000079$_{16}$	Timer A4 interrupt control register
00007A$_{16}$	Timer B0 interrupt control register
00007B$_{16}$	Timer B1 interrupt control register
00007C$_{16}$	Timer B2 interrupt control register
00007D$_{16}$	Reserved area **(Note)**
00007E$_{16}$	Reserved area **(Note)**
00007F$_{16}$	Reserved area **(Note)**

Note: Do not write to this address.

Fig. 2 Location of SFRs (1)

Address (Hexadecimal notation)	
000080$_{16}$	Reserved area **(Note)**
000081$_{16}$	Reserved area **(Note)**
000082$_{16}$	Reserved area **(Note)**
000083$_{16}$	Reserved area **(Note)**
000084$_{16}$	Reserved area **(Note)**
000085$_{16}$	Reserved area **(Note)**
000086$_{16}$	Reserved area **(Note)**
000087$_{16}$	Reserved area **(Note)**
000088$_{16}$	
000089$_{16}$	
00008A$_{16}$	Reserved area **(Note)**
00008B$_{16}$	
00008C$_{16}$	Reserved area **(Note)**
00008D$_{16}$	
00008E$_{16}$	Reserved area **(Note)**
00008F$_{16}$	
000090$_{16}$	Reserved area **(Note)**
000091$_{16}$	
000092$_{16}$	Reserved area **(Note)**
000093$_{16}$	
000094$_{16}$	
000095$_{16}$	External interrupt input read-out register
000096$_{16}$	D-A control register
000097$_{16}$	
000098$_{16}$	D-A register 0
000099$_{16}$	D-A register 1
00009A$_{16}$	
00009B$_{16}$	
00009C$_{16}$	Reserved area **(Note)**
00009D$_{16}$	Reserved area **(Note)**
00009E$_{16}$	Flash memory control register
00009F$_{16}$	
0000A0$_{16}$	Reserved area **(Note)**
0000A1$_{16}$	
0000A2$_{16}$	Reserved area **(Note)**
0000A3$_{16}$	
0000A4$_{16}$	Reserved area **(Note)**
0000A5$_{16}$	
0000A6$_{16}$	Waveform output mode register
0000A7$_{16}$	Dead-time timer
0000A8$_{16}$	Three-phase output data register 0
0000A9$_{16}$	Three-phase output data register 1
0000AA$_{16}$	Position-data-retain function control register
0000AB$_{16}$	
0000AC$_{16}$	Serial I/O pin control register
0000AD$_{16}$	
0000AE$_{16}$	Port P2 pin function control register
0000AF$_{16}$	
0000B0$_{16}$	Reserved area **(Note)**
0000B1$_{16}$	Reserved area **(Note)**
0000B2$_{16}$	Reserved area **(Note)**
0000B3$_{16}$	Reserved area **(Note)**
0000B4$_{16}$	Reserved area **(Note)**
0000B5$_{16}$	Reserved area **(Note)**
0000B6$_{16}$	Reserved area **(Note)**
0000B7$_{16}$	Reserved area **(Note)**
0000B8$_{16}$	Reserved area **(Note)**
0000B9$_{16}$	
0000BA$_{16}$	Reserved area **(Note)**
0000BB$_{16}$	Reserved area **(Note)**
0000BC$_{16}$	Clock control register 0
0000BD$_{16}$	Reserved area **(Note)**
0000BE$_{16}$	Reserved area **(Note)**
0000BF$_{16}$	Reserved area **(Note)**

Address (Hexadecimal notation)	
0000C0$_{16}$	
0000C1$_{16}$	
0000C2$_{16}$	
0000C3$_{16}$	
0000C4$_{16}$	Up-down register 1
0000C5$_{16}$	
0000C6$_{16}$	Timer A5 register
0000C7$_{16}$	
0000C8$_{16}$	Timer A6 register
0000C9$_{16}$	
0000CA$_{16}$	Timer A7 register
0000CB$_{16}$	
0000CC$_{16}$	Timer A8 register
0000CD$_{16}$	
0000CE$_{16}$	Timer A9 register
0000CF$_{16}$	
0000D0$_{16}$	Timer A0$_1$ register
0000D1$_{16}$	
0000D2$_{16}$	Timer A1$_1$ register
0000D3$_{16}$	
0000D4$_{16}$	Timer A2$_1$ register
0000D5$_{16}$	
0000D6$_{16}$	Timer A5 mode register
0000D7$_{16}$	Timer A6 mode register
0000D8$_{16}$	Timer A7 mode register
0000D9$_{16}$	Timer A8 mode register
0000DA$_{16}$	Timer A9 mode register
0000DB$_{16}$	Reserved area **(Note)**
0000DC$_{16}$	Comparator function select register 0
0000DD$_{16}$	Reserved area **(Note)**
0000DE$_{16}$	Comparator result register 0
0000DF$_{16}$	Reserved area **(Note)**
0000E0$_{16}$	Reserved area **(Note)**
0000E1$_{16}$	Reserved area **(Note)**
0000E2$_{16}$	Reserved area **(Note)**
0000E3$_{16}$	Reserved area **(Note)**
0000E4$_{16}$	Reserved area **(Note)**
0000E5$_{16}$	Reserved area **(Note)**
0000E6$_{16}$	Reserved area **(Note)**
0000E7$_{16}$	Reserved area **(Note)**
0000E8$_{16}$	Reserved area **(Note)**
0000E9$_{16}$	Reserved area **(Note)**
0000EA$_{16}$	Reserved area **(Note)**
0000EB$_{16}$	Reserved area **(Note)**
0000EC$_{16}$	Reserved area **(Note)**
0000ED$_{16}$	Reserved area **(Note)**
0000EE$_{16}$	Reserved area **(Note)**
0000EF$_{16}$	Reserved area **(Note)**
0000F0$_{16}$	
0000F1$_{16}$	Reserved area **(Note)**
0000F2$_{16}$	Reserved area **(Note)**
0000F3$_{16}$	
0000F4$_{16}$	
0000F5$_{16}$	Timer A5 interrupt control register
0000F6$_{16}$	Timer A6 interrupt control register
0000F7$_{16}$	Timer A7 interrupt control register
0000F8$_{16}$	Timer A8 interrupt control register
0000F9$_{16}$	Timer A9 interrupt control register
0000FA$_{16}$	
0000FB$_{16}$	
0000FC$_{16}$	
0000FD$_{16}$	$\overline{\mathrm{INT}}_5$ interrupt control register
0000FE$_{16}$	$\overline{\mathrm{INT}}_6$ interrupt control register
0000FF$_{16}$	$\overline{\mathrm{INT}}_7$ interrupt control register

Note: Do not write to this address.

Fig. 3 Location of SFRs (2)

FLASH MEMORY MODE

These microcomputers contain the flash memory; and single-power-supply reprogramming is available to this. These microcomputers have the following three modes, enabling reading/programming/erasure for the flash memory:

- Flash memory parallel I/O mode and Flash memory serial I/O mode, where the flash memory is handled by using an external programmer.
- CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU).

As shown in Figure 4, the flash memory is divided into several blocks, and erasure per block is possible.

This internal flash memory has the boot ROM area storing the reprogramming control software for reprogramming in the CPU reprogramming mode and flash memory serial I/O mode, as well as the user ROM area storing a certain control software for the normal operation in the microcomputer mode.

Although our reprogramming control firmware for the flash memory serial I/O mode has been stored into this boot ROM area on shipment, the user-original reprogramming control software which is more appropriate for the user's system is reprogrammable into this area, instead. Note that the reprogramming for the boot ROM area is enabled only in the flash memory parallel I/O mode.

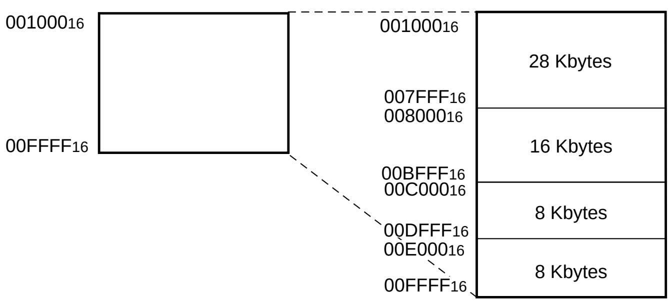


Fig. 4 M37906F8CFP, M37906F8CSP: block configuration of internal flash memory

Flash Memory Parallel I/O Mode

The flash memory parallel I/O mode is used to manipulate the internal flash memory with a parallel programmer. This parallel programmer uses the software commands listed in Table 1 to do the flash memory manipulations, such as read/programming/erase operations.

Table 1. Software commands (flash memory parallel I/O mode)

Software Command
Read Array
Read Status Register
Clear Status Register
Programming
Block Erase
Erase All Block

Addresses $FF90_{16}$ to $FF9F_{16}$ are the reserved area for the parallel programmer. Therefore, when the user uses the flash memory parallel I/O mode, do not program to this area.

User ROM Area and Boot ROM Area

The user ROM area and boot ROM area can be reprogrammed in the flash memory parallel I/O mode.
The programming and block erase operations can be performed only to these areas.
The boot ROM area, 8 Kbytes in size, is assigned to addresses 0000_{16}–$1FFF_{16}$, so that programming and block erase operations can be performed only to this area. (Access to any address out of this area is prohibited).
The erasable block in the boot ROM area is only one block, consisting of 8 Kbytes. The reprogramming control firmware to be used in the flash memory serial I/O mode has been stored to this boot ROM area on our shipment. Therefore, do not reprogram the boot ROM area if the user uses the flash memory serial I/O mode.
Do not program to addresses $FF90_{16}$ to $FF9F_{16}$ because this area is the reserved area for the programmer.
Note that, when the boot ROM area is read out from the CPU in the CPU reprogramming mode, described later, its addresses will be shifted to $E000_{16}$—$FFFF_{16}$.

Flash Memory Serial I/O Mode

In the flash memory serial I/O mode, addresses, data, and software commands, which are required to read/program/erase the internal flash memory, are serially input and output with a fewer pins and the dedicated serial programmer.

In this mode, being different from the flash memory parallel I/O mode, the CPU controls reprogramming of the flash memory (using the CPU reprogramming mode), serial input of the reprogramming data, etc.

The reprogramming control firmware for the flash memory serial I/O mode has been stored in the boot ROM area on shipment of the product from us. Note that, then, the flash memory serial I/O mode will become unavailable if the boot ROM area has been reprogrammed in the flash memory parallel I/O mode.

Note that, also, this reprogramming control firmware for the flash memory serial I/O mode is subject to change.

Figures 5 and 6 show the pin connections in the flash memory serial I/O mode.

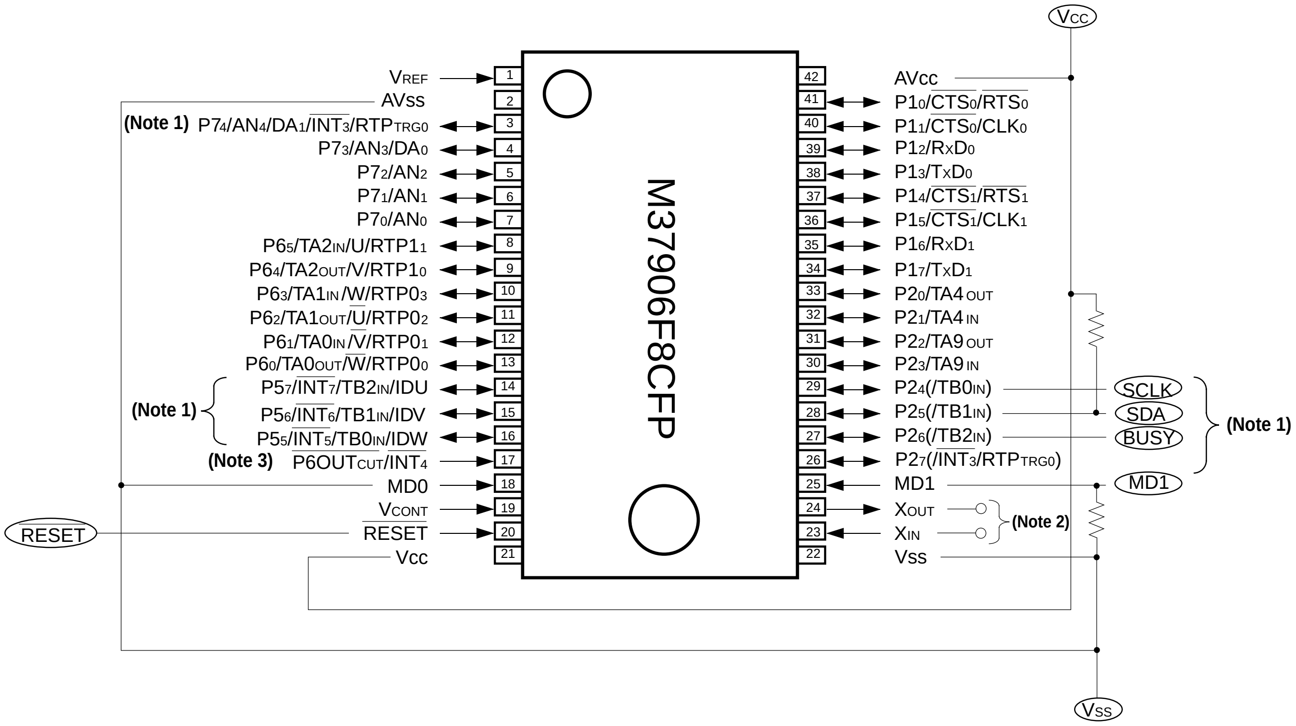
The three pins, SCLK, SDA, and BUSY, are used to input and output serial data.

The SCLK pin is the input pin of external transfer clocks. The SDA pin is the I/O pin of transmit and receive data, and its output acts as the N-channel open-drain output. To the SDA pin, connect an external pullup resistor (about 1 kΩ). The BUSY pin is the output pin of the BUSY flag (CMOS output) and goes “H” during BUSY periods owing to a certain operation, such as transmit, receive, erase, programming, etc.

Transmit and receive data are serially transferred 8 bits at a time.

In the flash memory serial I/O mode, only the user ROM area can be reprogrammed; the boot ROM area is not accessible.

Addresses $FF90_{16}$ to $FF9F_{16}$ are the reserved area for the serial programmer. Therefore, when the user uses the flash memory serial I/O mode, do not program to this area.



Notes 1: Allocation of pins TB0IN to TB2IN and INT3/RTPTRG0 can be switched by software.
2: Connected to the oscillation circuit.
3: Recommended to be connected with VCC via a resistor.

: Connected to a serial programmer.

Outline 42P2R-E

Fig. 5 Pin connection of M37906F8CFP in flash memory serial I/O mode (outline: 42P2R-E)

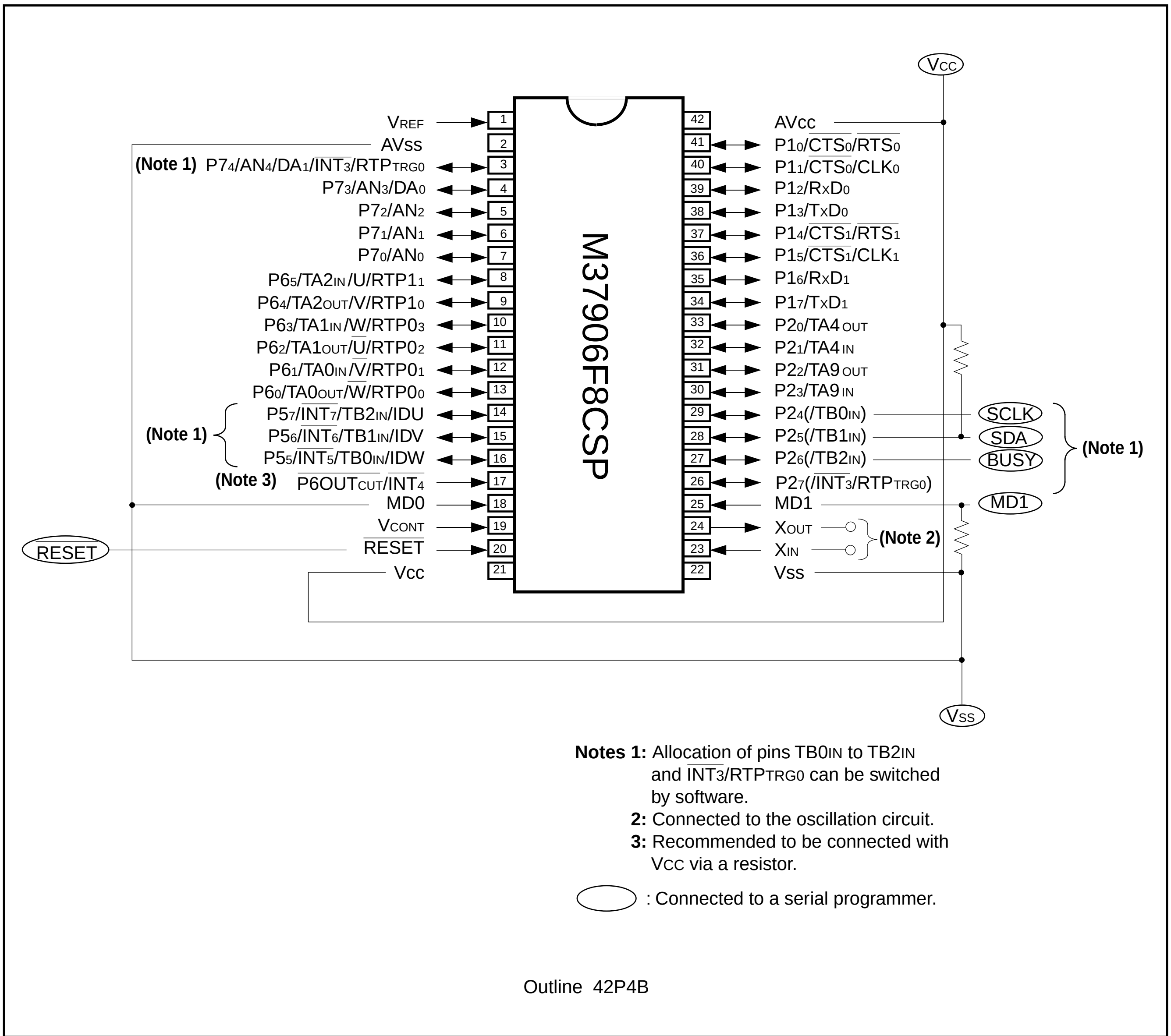


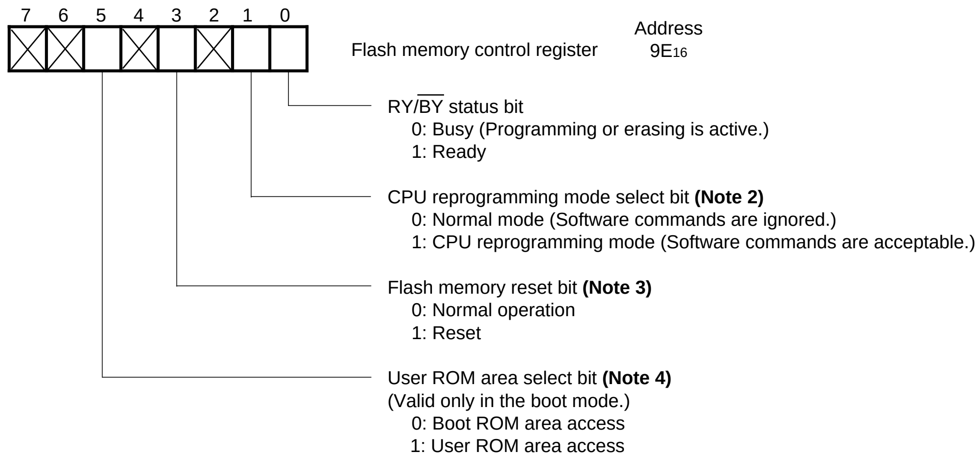
Fig. 6 Pin connection of M37906F8CSP in flash memory serial I/O mode (outline: 42P4B)

CPU Reprogramming Mode

The CPU reprogramming mode is used to perform the operations for the internal flash memory (reading, programming, erasing) under control of the CPU.
In this mode, only the user ROM area can be reprogrammed; the boot ROM area cannot be reprogrammed.
The user-original reprogramming control software for the CPU reprogramming mode can be stored in either the user ROM area or the boot ROM area.
Because the CPU cannot read out the flash memory in the CPU reprogramming mode, the above software must be transferred to the internal RAM in advance to be executed.

Boot Mode

The user-original reprogramming control software for the CPU reprogramming mode must be stored into the user ROM area or the boot ROM area in the flash memory parallel I/O mode in advance. (If this program has been stored into the boot ROM area, the flash memory serial I/O mode will become unavailable).
Note that addresses of the boot ROM area depend on the accessing ways to the boot ROM area, When accessing in the flash memory parallel I/O mode, these addresses will be shifted to 0000_{16} to $1FFF_{16}$. On the other hand, when accessing with the CPU, these addresses will be shifted to $E000_{16}$ to $FFFF_{16}$.
Reset removal with both of the MD0 and MD1 pins held "L" invokes the normal microcomputer mode, and the CPU operates using the control software stored in the user ROM area. In this case, the boot ROM area is not accessible.
Removing reset with the MD0 pin held "L" and the MD1 pin "H", the CPU starts its operation using the reprogramming control software stored in the boot ROM area. This mode is called the boot mode. The reprogramming control software in the boot ROM area can also reprogram the user ROM area.
After reset removal, be sure not to change the status at pins MD0 and MD1.



Notes 1: The contents of the flash memory control register after reset is removed are "XX000001".
2: To set "1", writing of "0" to bit 1 and subsequent writing of "1" to bit 1 are necessary. Writing to bit 1 must be performed by the user-original reprogramming control software in the internal RAM.
3: This bit is valid only when bit 1 = "1". Before setting this bit to "0", be sure to confirm that bit 0 = "1" after setting this bit to "1" (reset). This bit 3 must be controlled with bit 1 = "1".
4: Writing to bit 5 must be performed by the user-original reprogramming control software in the internal RAM.

Fig. 7 Bit configuration of flash memory control register

Function overview (CPU reprogramming mode)

The CPU reprogramming mode is available in the single-chip mode, memory expansion mode, and boot mode to reprogram the user ROM area only.

In the CPU reprogramming mode, the CPU erases, programs, and reads the internal flash memory by writing software commands. Note that the user-original reprogramming control software must be transferred to the internal RAM in advance to be executed.

The CPU reprogramming mode becomes active when "1" is written into the flash memory control register's bit 1 (the CPU reprogramming mode select bit) shown in Figure 7, and software commands become acceptable.

In the CPU reprogramming mode, software commands and data are all written to and read from even addresses (Note that address A_0 in byte addresses = "0".) 16 bits at a time. Therefore, a software command consisting of 8 bits must be written to an even address; therefore, any command written to an odd address will be invalid. Since the write data at the 2nd cycle of a programming command consists of 16 bits, this data must be written to even and odd addresses.

The seaquencer in the flash memory controls the erase and programming operations. What the status of the seaquencer operation is and whether the programming or erase operation has been completed normally or terminated by an error can be examined by reading the flash memory control register.

Figure 7 shows the bit configuration of the flash memory control register.

Bit 0 (the RY/$\overline{BY}$ status bit) is a read-only bit for indicating the seaquencer operation. This bit goes to "0" (BUSY) while the automatic programming/erase operation is active and goes to "1" (READY) during the other operations.

Bit 1 serves as the CPU reprogramming mode select bit. Writing of "1" to this bit selects the CPU reprogramming mode, and software commands will be acceptable. Because the CPU cannot directly access the internal flash memory in the CPU reprogramming mode, writing to this bit 1 must be performed by the user-original reprogramming control software which has been transferred to the internal RAM in advance. To set bit 1 to "1", it is necessary to write "0" and "1" to this bit 1 successively. On the other hand, to clear this bit to "0", it is sufficient only to write "0".

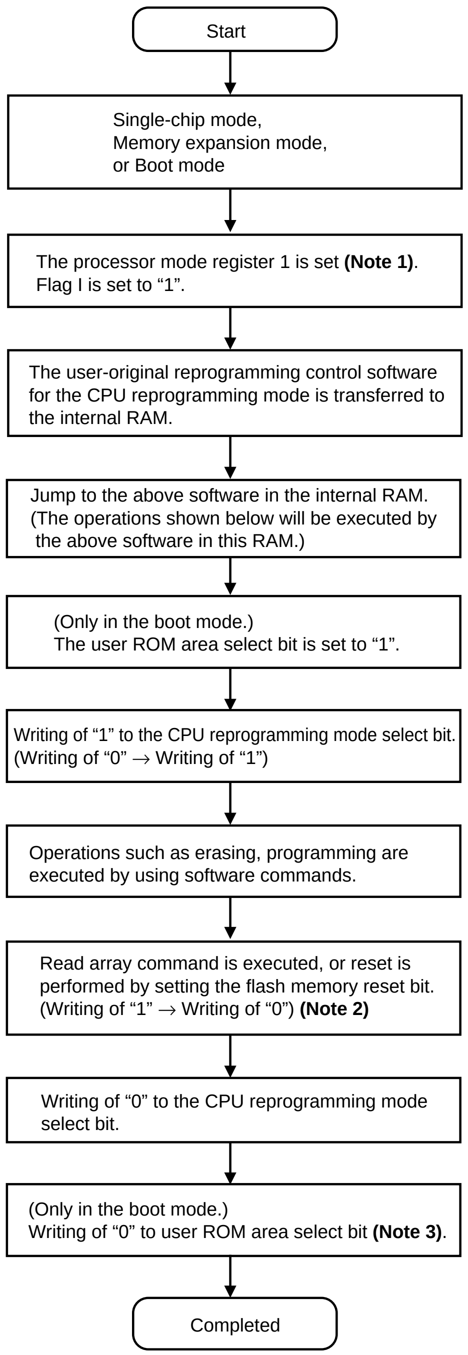
Bit 3 (the flash memory reset bit) resets the control circuit of the internal flash memory and is used when the CPU reprogramming mode is terminated or when an abnormal access to the flash memory happens. Writing of "1" to bit 3 with the CPU reprogramming mode select bit = "1" preforms the reset operation. To remove the reset, write "0" to bit 3 after confirming bit 0 (the RY/$\overline{BY}$ status bit) becomes "1".

Bit 5 serves as the user ROM area select bit and is valid only in the boot mode. Setting this bit to "1" in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU reprogramming mode in the boot mode, set this bit to "1". Note that when the microcomputer is booted up in the user ROM area, only the user ROM area is accessible and bit 5 is invalid; on the other hand, when the microcomputer is in the boot mode, bit 5 is valid independent of the CPU reprogramming mode. To rewrite bit 5, execute the user-original reprogramming control software transferred to the internal RAM in advance.

Figure 8 shows the CPU reprogramming mode set/termination flowchart, and be sure to follow this flowchart. As shown in Note 1 of Figure 8, before selecting the CPU reprogramming mode, set "0" to the processor mode register 1's bit 7 (the internal ROM bus cycle select bit) and set flag I to "1" to avoid an interrupt request input.

When a watchdog timer interrupt request is generated in the CPU reprogramming mode, when an input to the $\overline{RESET}$ pin is "L", or when the software reset is performed, the flash memory control circuit and flash memory control register will be reset.

When the flash memory is reset during the erase or programming operation, this operation is cancelled and the target block's data will be invalid. Just before writing a software command related to the erase/programming operation, be sure to write to the watchdog timer. In the CPU reprogramming mode, be sure not to use the **STP** and **WIT** instructions.



Notes 1: The processor mode register 1’s bit 7 (address $5F_{16}$, the internal ROM bus cycle select bit) must be “0” (bus cycle = 3ϕ).
2: To terminate the CPU reprogramming mode after the erase and programming operations have been completed, be sure to execute the read array command or perform the flash memory reset operation.
3: This bit may remain “1”. However, if this bit is “1”, the user ROM area access is specified.

Fig. 8 CPU reprogramming mode set/termination flowchart

Software Commands

Table 2 lists the software commands.
By writing a software command after the CPU reprogramming mode select bit has been set to “1”, erasing, programming, etc. can be specified. Note that, at software commands’ input, the high-order byte (D_8–D_{15}) is ignored. (Except for the write data at the 2nd cycle of a programming command.)
Software commands are explained as below.

Read Array Command (FF_{16})

By writing command code “FF_{16}” at the 1st bus cycle, the microcomputer enters the read array mode. If an address to be read is input in the next or the following bus cycles, the contents at the specified address are output to the data bus (D_0 to D_{15}) in a unit of 16 bits.
The read array mode is maintained until writing of another software command.

Read Status Register Command (70_{16})

Writing command code “70_{16}” at the 1st bus cycle outputs the contents of the status register to the data bus (D_0-D_7) by a read at the 2nd bus cycle.
The status register is explained later.

Clear Status Register Command (50_{16})

This command clears two status bits (SR.4, 5) each of which is set to “1” to indicate that the operation has been terminated by an error. To clear these bits, write command code “50_{16}” at the 1st bus cycle.

Programming Command (40_{16})

This command facilitates programming of 1 word (2 bytes) at a time. To initiate programming, write command code “40_{16}” at the 1st bus cycle; when write data is written in a unit of 16 bits at the 2nd bus cycle, the address is specified at the same time. Upon completion of data writing, automatic programming (data programming and verification) operation is started.
The completion of the automatic programming operation is confirmed by a read of the flash memory control register. The RY/$\overline{BY}$ status bit of the flash memory control register goes “0” during the automatic programming operation; and also, it goes “1” after the end of it.
Before execution of the next command, be sure to confirm that the RY/$\overline{BY}$ status bit is set to “1” (READY). During the automatic programming operation, writing of commands and access to the flash memory must not be performed.
When programming continuously, the programming command can be executed with the read status register mode kept if there is no programming error. Simultaneously with start of the automatic programming, the read status register mode is automatically active. In this case, the read status register mode is retained until the next read array command (FF_{16}) is written or until the reset is performed by using the flash memory reset bit.
Reading out the status register after the automatic programming operation is completed reports the result of it. For details, refer to the section on the status register.
Figure 9 shows an example of the programming flowchart.
Additional programming to any word that has already been programmed is prohibited.

Table 2. Software commands (CPU reprogramming mode)

Command	1st cycle			2nd cycle		
	Mode	Address	Data (D_0 to D_7)	Mode	Address	Data
Read Array	Write	X **(Note 2)**	FF_{16}	—	—	—
Read Status Register	Write	X	70_{16}	Read	X	SRD **(Note 3)**
Clear Status Register	Write	X	50_{16}	—	—	—
Programming	Write	X	40_{16}	Write	WA **(Note 4)**	WD **(Note 4)**
Block Erase	Write	X	20_{16}	Write	BA **(Note 5)**	$D0_{16}$
Erase All Block	Write	X	20_{16}	Write	X	20_{16}

Notes 1: At software commands' input, the high-order byte of data (D_8–D_{15}) is ignored.
2: X = An arbitrary address in the user ROM area. (Note that A_0 = "0".)
3: SRD = Status Register Data
4: WA = Write Address, WD = Write Data (16 bits).
5: Block address: the maximum address of each block must be input. Note that address A_0 = "0".

Block Erase Command (20_{16}/$D0_{16}$)

Writing command code "20_{16}" at the 1st bus cycle and writing confirmation command code "$D0_{16}$" and the maximum address of the block (Note that address A_0 = "0".) at the subsequent 2nd bus cycle initiate the automatic erase (erasing and erase verification) operation for the specified block.
The completion of the automatic erase operation is confirmed by a read of the flash memory control register. The RY/$\overline{BY}$ status bit of the flash memory control register goes "0" simultaneously with start of the automatic erase operation; and also, it goes "1" simultaneously with completion of it.
Before execution of the next command, be sure to confirm that the RY/$\overline{BY}$ status bit is set to "1" (READY). During the automatic erase operation, writing of commands and access to the flash memory must not be performed.
Simultaneously with start of the automatic erase, the read status register mode is automatically active. In this case, the read status register mode is retained until the next read array command (FF_{16}) is written or until the reset is performed by using the flash memory reset bit.
Reading out the status register after the automatic erase operation is completed reports the result of it. For details, refer to the section on the status register.
Figure 10 shows an example of the block erase flowchart.

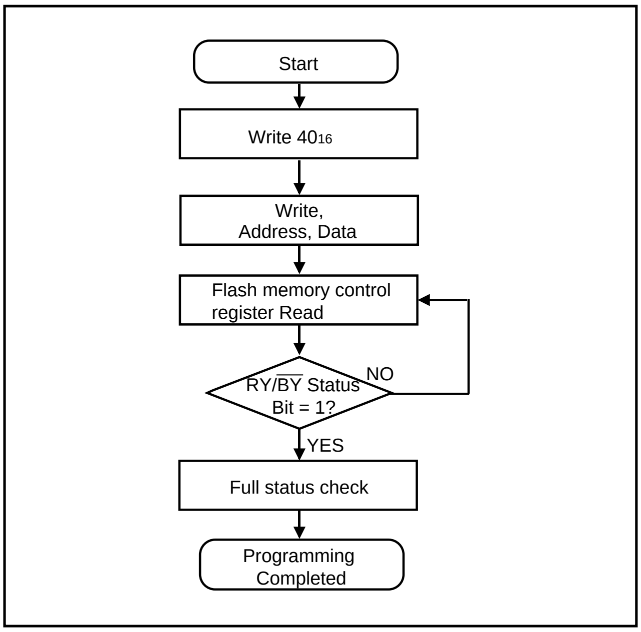


Fig. 9 Programming flowchart

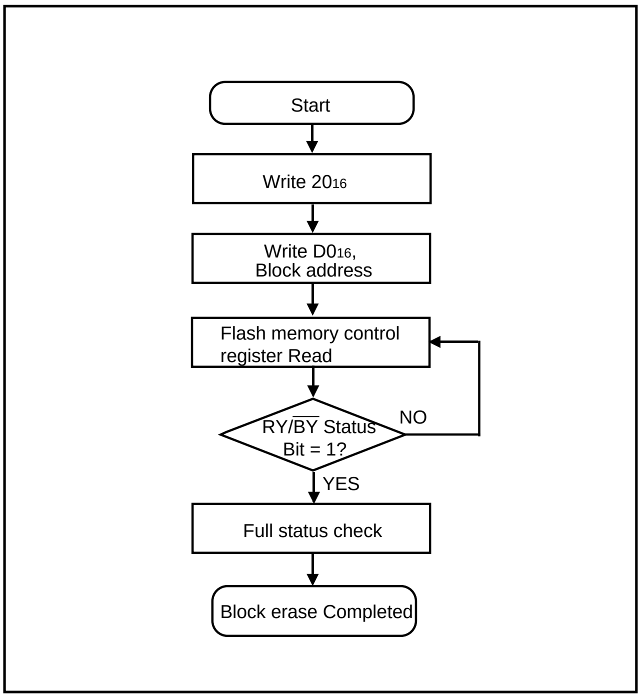


Fig. 10 Block erase flowchart

Erase All Block Command (20_{16}/20_{16})

Writing command code "20_{16}" at the 1st bus cycle and writing command code "20_{16}" at the subsequent 2nd bus cycle initiate the continuous block erase (chip erase) operations for all the blocks.
The completion of the chip erase operation, as well as of the block erase operation, is confirmed by a read of the flash memory control register. The result of the automatic erase operation is also reported by a read of the status register.
During the automatic erase operation (when the RY/$\overline{BY}$ status bit = "0"), writing of commands and access to the flash memory must not be performed.

Status Register

The status register is used to indicate whether the programming/erase operation has been completed normally or terminated by an error. By writing the read status register command (70_{16}), the contents of the status register can be read out; by writing the clear status register command (50_{16}), the contents of the status register can be cleared.
Table 3 lists the definition of each bit of the status register.
The status register outputs "80_{16}" after reset is removed.
The status of each bit is described below.

Erase Status Bit (SR.5)

This bit reports the status of the automatic erase operation. This bit is set to “1” if an erase error occurs and returns to “0” if the clear status register command (50_{16}) is written.

Programming Status Bit (SR.4)

This bit reports the status of the automatic programming operation. This bit is set to “1” if a programming error occurs and returns to “0” if the clear status register command (50_{16}) is written.

Under the condition that any of SR.5, SR.4 = “1”, none of the programming, block erase, and erase all block commands can be accepted. Before execution of these commands, execute the clear status register command (50_{16}), in advance, to clear these status bits.

Both of SR.4, SR.5 are set to “1” under the following conditions (Command Sequence Error):

(1) when data other than “$D0_{16}$” and “FF_{16}” is written to the data in the 2nd bus cycle of the block erase command (20_{16}/$D0_{16}$)

(2) when data other than “20_{16}” and “FF_{16}” is written to the data in the 2nd bus cycle of the erase all block command (20_{16}/20_{16})

Note that, writing of “FF_{16}” forces the microcomputer into the read array mode. Simultaneously with this, the command written in the 1st bus cycle will be canceled.

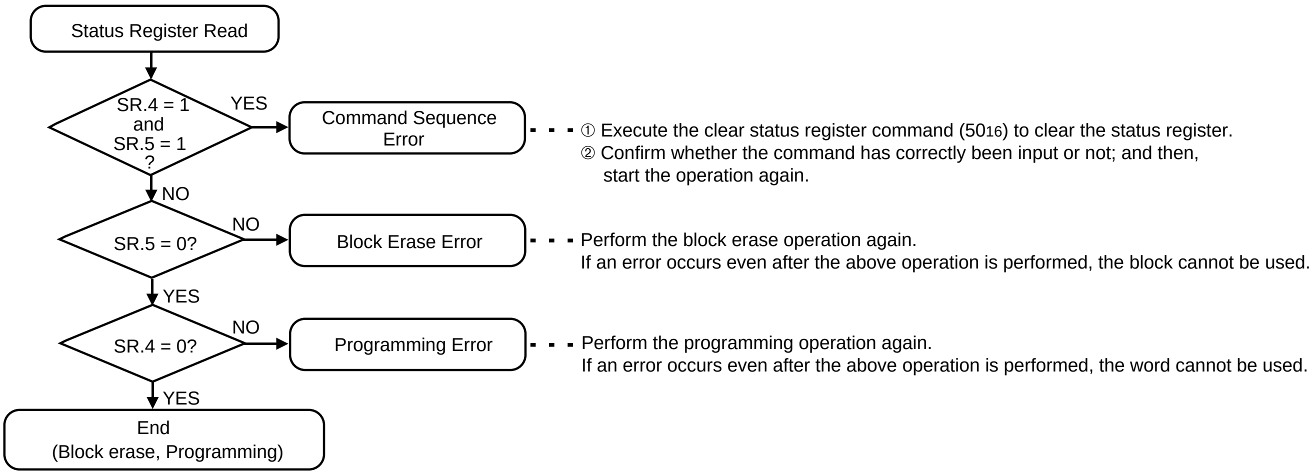
Full Status Check

The full status check reports the results of the erase or programming operation.

Figure 11 shows the full status check flowchart and actions to be taken if an error has occurred.

Table 3. Bit definition of status register

Symbol	Status	Definition	
		“1”	“0”
SR.7 (D_7)	Reserved	—	—
SR.6 (D_6)	Reserved	—	—
SR.5 (D_5)	Erase Status	Terminated by error.	Terminated normally.
SR.4 (D_4)	Programming Status	Terminated by error.	Terminated normally.
SR.3 (D_3)	Reserved	—	—
SR.2 (D_2)	Reserved	—	—
SR.1 (D_1)	Reserved	—	—
SR.0 (D_0)	Reserved	—	—



Note: Under the condition that any of SR.5 and SR.4 = “1”, none of the programming, block erase, and erase all block commands can be accepted. Before execution of these commands, execute the clear status register command (50_{16}) in advance.

Fig. 11 Full status check flowchart and actions to be taken if an error has ocurred

DC Electrical Characteristics (V_{CC} = 5 V ± 0.5 V, Ta = 0 to 60 °C, f(f_{sys}) = 20 MHz (Note))

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
I_{CC1}	V_{CC} power source current (at read)		30	48	mA
I_{CC2}	V_{CC} power source current (at write)			48	mA
I_{CC3}	V_{CC} power source current (at programming)			54	mA
I_{CC4}	V_{CC} power source current (at erasing)			54	mA

Limits of V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, and I_{IL} for each pin are the same as those in the microcomputer mode.
Note: f(f_{sys}) indicates the system clcok (fsys) frequency.

AC Electrical Characteristics (V_{CC} = 5 V ± 0.5 V, Ta = 0 to 60 °C, f(f_{sys}) = 20 MHz (Note))

Parameter	Limits			Unit
	Min.	Typ.	Max.	
256-byte programming time		4	40	ms
Block erase time		0.6	8	s
Erase all block time		0.6 × n	8 × n	s

n = Number of blocks to be erased

The limits of parameters other than the above are same as those in the microcomputer mode.

Note: f(f_{sys}) indicates the system clock (fsys) frequency.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Power source voltage	–0.3 to 6.5	V
AV_{CC}	Analog power source voltage	–0.3 to 6.5	V
V_I	Input voltage P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P6₀–P6₅, P7₀–P7₄, $\overline{\text{P6OUT}_{CUT}}$, V_{CONT}, V_{REF}, X_{IN}, $\overline{\text{RESET}}$, BYTE, MD0, MD1	–0.3 to V_{CC}+0.3	V
V_O	Output voltage P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P6₀–P6₅, P7₀–P7₄, X_{OUT}	–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	300	mW
T_{opr}	Operating ambient temperature	–20 to 85	°C
T_{stg}	Storage temerature	–40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (Vcc = 5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage	4.5	5.0	5.5	V
AV_{CC}	Analog power source voltage		V_{CC}		V
V_{SS}	Power source voltage		0		V
AV_{SS}	Analog power source voltage		0		V
V_{IH}	High-level input voltage P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P6₀–P6₅, P7₀–P7₄, $\overline{\text{P6OUT}_{CUT}}$, X_{IN}, $\overline{\text{RESET}}$, MD0, MD1	0.8 Vcc		Vcc	V
V_{IL}	Low-level input voltage P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P6₀–P6₅, P7₀–P7₄, $\overline{\text{P6OUT}_{CUT}}$, X_{IN}, $\overline{\text{RESET}}$, MD0, MD1	0		0.2 V_{CC}	V
$I_{OH(peak)}$	High-level peak output current P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P6₀–P6₅, P7₀–P7₄			–10	mA
$I_{OH(avg)}$	High-level average output current P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P6₀–P6₅, P7₀–P7₄			–5	mA
$I_{OL(peak)}$	Low-level peak output current P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P7₀–P7₄			10	mA
$I_{OL(peak)}$	Low-level peak output current P6₀–P6₅			20	mA
$I_{OL(avg)}$	Low-level average output current P1₀–P1₇, P2₀–P2₇, P5₅–P5₇, P7₀–P7₄			5	mA
$I_{OL(avg)}$	Low-level average output current P6₀–P6₅			15	mA
$f(X_{IN})$	External clock input frequency **(Note 1)**			20	MHz
$f(f_{sys})$	System clock frequency			20	MHz

Notes 1: When using the PLL frequency multiplier, be sure that $f(f_{sys})$ = 20 MHz or less.
2: The average output current is the average value of an interval of 100 ms.
3: The sum of $I_{OL(peak)}$ must be 110 mA or less, the sum of $I_{OH(peak)}$ must be 80 mA or less.

DC ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, f(f_{sys}) = 20 MHz)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High-level output voltage $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P5_5$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_4$	I_{OH} = –10 mA		3			V
V_{OL}	Low-level output voltage $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P5_5$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_4$	I_{OL} = 10 mA				2	V
V_{T+} —V_{T-}	Hysteresis $TA0_{IN}$–$TA2_{IN}$, $TA4_{IN}$, $TA9_{IN}$, $TA0_{OUT}$–$TA2_{OUT}$, $\overline{TA4_{OUT}}$, $\overline{TA9_{OUT}}$, $\overline{TB0_{IN}}$–$TB2_{IN}$, $\overline{INT_3}$–$\overline{INT_7}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1, RxD_0, RxD_1, RTP_{TRG0}, $\overline{P6OUT_{CUT}}$			0.4		1	V
V_{T+} —V_{T-}	Hysteresis $\overline{RESET}$			0.5		1.5	V
V_{T+} —V_{T-}	Hysteresis X_{IN}			0.1		0.3	V
I_{IH}	High-level input current $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P5_5$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_4$, $\overline{P6OUT_{CUT}}$, X_{IN}, $\overline{RESET}$, MD0, MD1	V_I = 5.0 V				5	µA
I_{IL}	Low-level input current $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P5_5$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_4$, $\overline{P6OUT_{CUT}}$, X_{IN}, $\overline{RESET}$, MD0, MD1	V_I = 0 V				–5	µA
V_{RAM}	RAM hold voltage	When clock is inactive.		2			V
I_{CC}	Power source current	Output-only pins are open, and the other pins are connected to Vss or Vcc. An external square-waveform clock is input. (Pin X_{OUT} is open.) The PLL frequency multiplier is inactive.	f(f_{sys}) = 20 MHz. CPU is active.		25	50	mA
			Ta = 25 °C when clock is inactive.			1	µA
			Ta = 85 °C when clock is inactive.			20	

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5 V ± 0.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
———	Resolution	V_{REF} = V_{CC}	A-D converter			10	Bits
			Comparator			$\frac{1}{256}V_{REF}$	V
———	Absolute accuracy	V_{REF} = V_{CC}	10-bit resolution mode			± 3	LSB
			8-bit resolution mode			± 2	LSB
			Comparater			± 40	mV
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}		5			kΩ
t_{CONV}	Conversion time	f(f_{sys}) ≤ 20 MHz	10-bit resolution mode	5.9			µs
			8-bit resolution mode	2.45 **(Note)**			
			Comparater	0.7 **(Note)**			
V_{REF}	Reference voltage			2.7		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{REF}	V

Note: This is applied when A-D conversion freguency (ϕ_{AD}) = f_1 (ϕ).

D-A CONVERTER CHARACTERISTICS

(V_{CC} = 5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 5 V, T_a = –20 to 85 °C, unless otherwise noted)

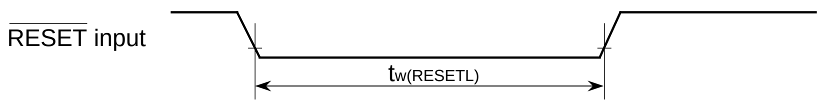
Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
——	Resolution				8	Bits
——	Absolute accuracy				± 1.0	%
t_{su}	Set time				3	µs
R_O	Output resistance		2	3.5	4.5	kΩ
I_{VREF}	Reference power source input current	**(Note)**			3.2	mA

Note: The test conditions are as follows:
- One D-A converter is used.
- The D-A register value of the unused D-A converter is "00_{16}."
- The reference power source input current for the ladder resistance of the A-D converter is excluded.

RESET INPUT

Reset input timing requirements (V_{CC} = 5 V ± 0.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{w(RESETL)}$	$\overline{RESET}$ input low-level pulse width	10			µs



PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(V_{CC} = 5 V±0.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, $f(f_{sys})$ = 20 MHz unless otherwise noted)

∗ For limits depending on $f(f_{sys})$, their calculation formulas are shown below. Also, the values at $f(f_{sys})$ = 20 MHz are shown in ( ).

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{c(TA)}$	TAiIN input cycle time	80		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter		Limits Min.	Limits Max.	Unit
$t_{c(TA)}$	TAiIN input cycle time	$f(f_{sys}) \le 20$ MHz	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	$f(f_{sys}) \le 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	$f(f_{sys}) \le 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

Note : The TAiIN input cycle time requires 4 or more cycles of a count source. The TAiIN input high-level pulse width and the TAiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(f_{sys}) \le 20$ MHz.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter		Limits Min.	Limits Max.	Unit
$t_{c(TA)}$	TAiIN input cycle time	$f(f_{sys}) \le 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width		80		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{w(TAH)}$	TAiIN input high-level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	80		ns

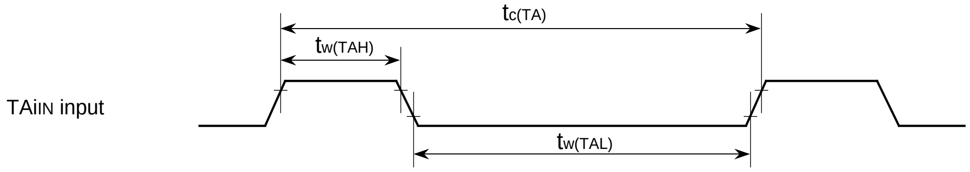
Timer A input (Up-down input and Count input in event counter mode)

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high-level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low-level pulse width	1000		ns
$t_{su(UP-T_{IN})}$	TAiOUT input setup time	400		ns
$t_{h(T_{IN}-UP)}$	TAiOUT input hold time	400		ns

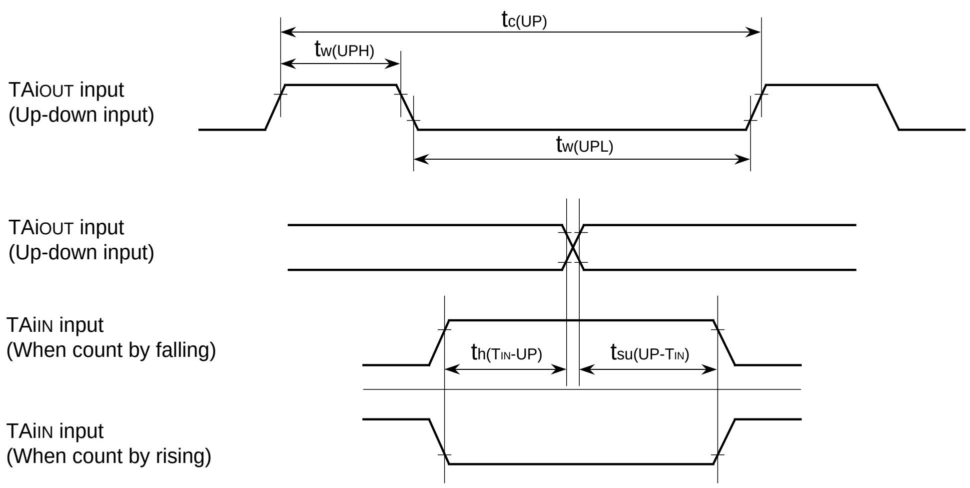
Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAj$_{IN}$ input cycle time	800		ns
$t_{su(TAj_{IN}-TAj_{OUT})}$	TAj$_{IN}$ input setup time	200		ns
$t_{su(TAj_{OUT}-TAj_{IN})}$	TAj$_{OUT}$ input setup time	200		ns

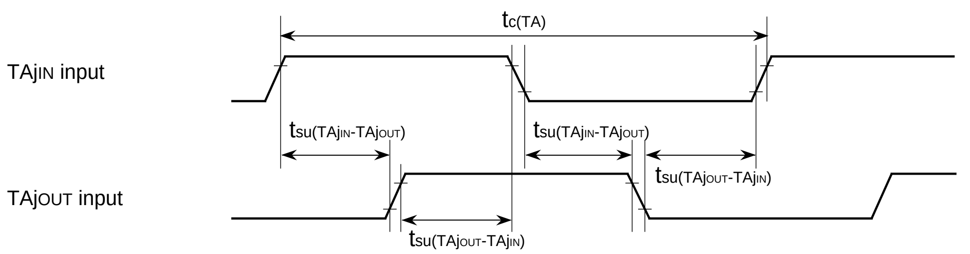
- Gating input in timer mode
- Count input in event counter mode
- External trigger input in one-shot pulse mode
- External trigger input in pulse width modulation mode



- Up-down and Count input in event counter mode



- Two-phase pulse input in event counter mode



Test conditions
- V_{CC} = 5 V ± 0.5 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 1.0 V, VIH = 4.0 V

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (both edge count)	160		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (both edge count)	80		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (both edge count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$f(f_{sys}) \leq 20$ MHz	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(f_{sys}) \leq 20$ MHz.

Timer B input (Pulse width measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$f(f_{sys}) \leq 20$ MHz	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

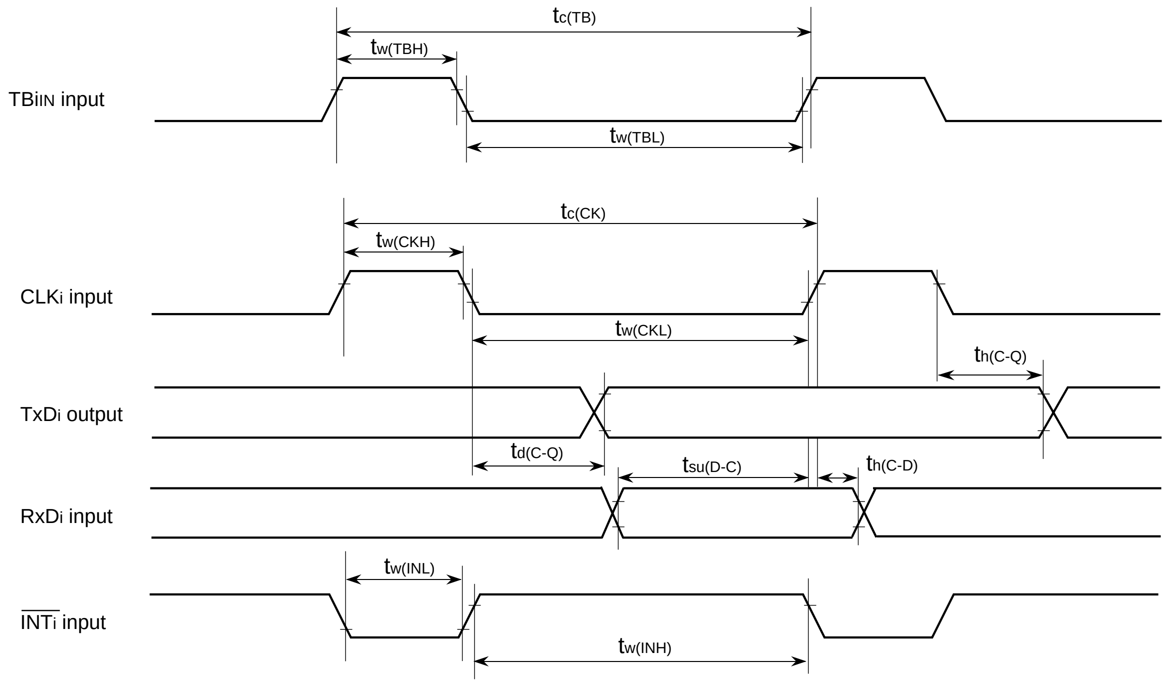
Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(f_{sys}) \leq 20$ MHz.

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	100		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	20		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

External interrupt ($\overline{INT_i}$) input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns



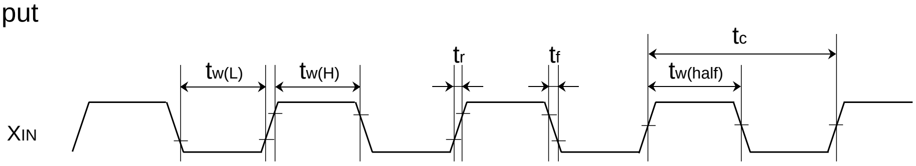
Test conditions
- V_{CC} = 5 V ± 0.5 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF

External clock input

Timing Requirements (V_{CC} = 5 V±0.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(half)}$	External clock input pulse width with half input-volage	0.45 tc	0.55 tc	ns
$t_{w(H)}$	External clock input high-level pulse width	0.5 t_c – 8		ns
$t_{w(L)}$	External clock input low-level pulse width	0.5 t_c – 8		ns
t_r	External clock input rise time		8	ns
t_f	External clock input fall time		8	ns

External clock input



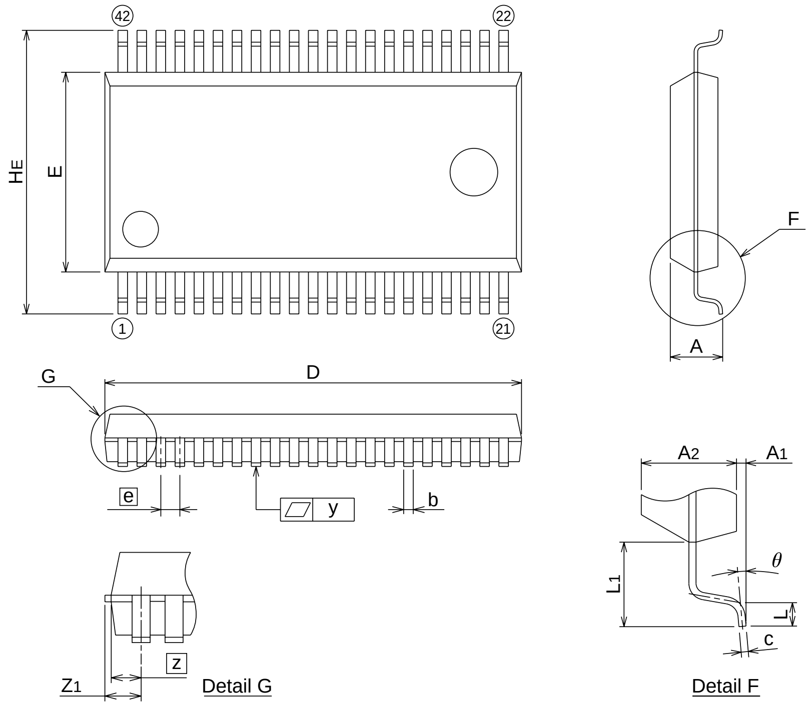
Test conditions
- Vcc = 5 V ± 0.5 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V ($t_{w(H)}$, $t_{w(L)}$, t_r, t_f)
- Input timing voltage : 2.5 V (t_c, $t_{w(half)}$)

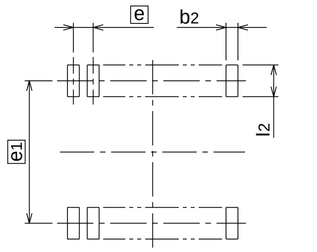
PACKAGE OUTLINE

42P2R-E

Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	0.63	Alloy 42/Cu Alloy





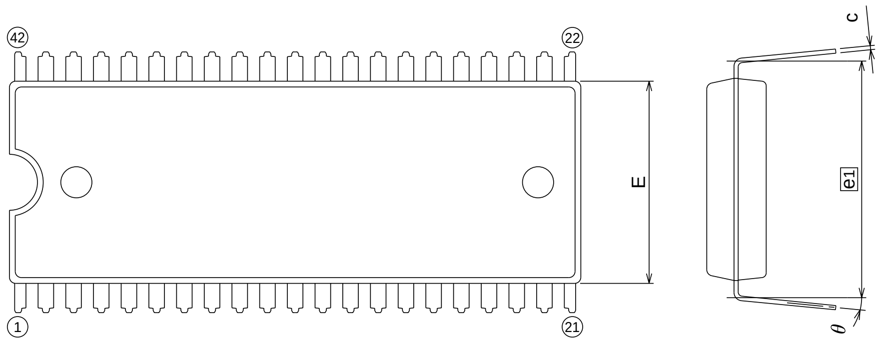
Recommended Mount Pad

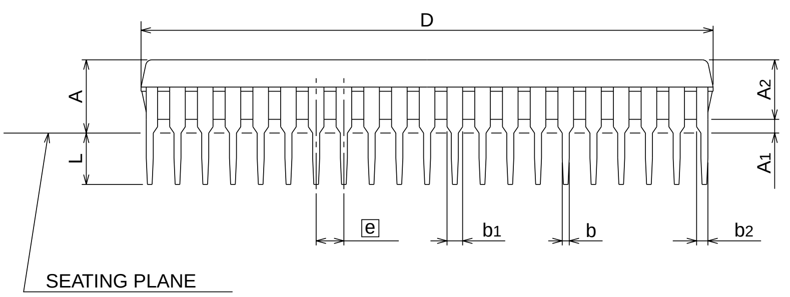
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
z	–	0.75	–
Z_1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
e_1	–	11.43	–
I_2	1.27	–	–

42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
e_1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

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Rev.	Date	Description	
		Page	Summary
1.0	3/02/01	—	First Edition
2.0	6/26/01	— 1 17 19 23	Some English expressions and the following are corrected: •DESCRIPTION; line 3 <Error> •••• silicon gate technology, being packaged •••• <Correction> •••• silicon gate technology, including the internal flash memory and being packaged •••• •Figure 7; Note 3 <Error> •••• after setting this bit to “1” (reset). <Correction> •••• after setting this bit to “1” (reset). This bit 3 must be controlled with bit 1 = “1”. •Programming Command (40_{16}); lines 18,19 <Error> •••• be executed with the read status register mode kept. •••• <Correction> •••• be executed with the read status register mode kept if there is no programming error. •••• •Figure 11 <Error> Status Register Error <Correction> Status Register Read