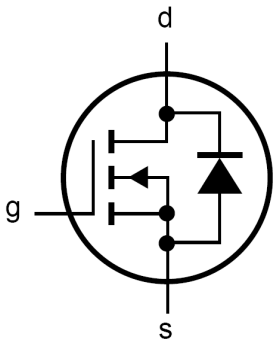
BLV7002 N-channel Enhancement Mode Vertical D-MOS Transistor Chip

Description

N-channel enhancement mode field-effect transistor



Features

Very fast switching
Logic level compatible

Applications

Relay driver
High speed line driver
Logic level translator.

structure

Planar type
Electrodes: Aluminum alloy
Backside metal: Au alloy

Size

Chip size: 495μm ×490μm
Chip thickness: 220±20μm.
Scribe street width: 50μm
Pad size: 90μm x90μm
Die per wafer: 25800

ABSOLUTE MAXIMUM RATING

Symbol	*Parameter*	Min.	Max.	Unit
V_{DS}	Drain – source voltage (DC)	-	60	V
V_{GS}	Gate – source voltage (DC)	-	±20	V
I_D	Drain current (DC)	-	115	mA
I_{DM}	Peak drain current	-	0.46	A
P_{tot}	Total power dissipation	-	0.2	W
T_{STG}	Storage temperature	-55	+150	^oC
T_j	Junction temperature	-	150	^oC

CHARACTERISTICS

T_j = 25°C unless otherwise specified

Symbol	*Parameter*	Test conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source breakdown voltage	V_{GS}=0V,I_D=250u A	60	73	-	V
I_{DSS}	Drain-source leakage current	V_{DS}=60V, V_{GS}=0V	-	1	500	nA
I_{GSS}	Gate-source leakage current	V_{GS}=±20V, V_{DS}=0V	-	1	±100	nA
V_{GSth}	Gate-source threshold voltage	V_{DS}=2.5V, I_D=250uA	1	-	2.5	V
R_{DSon}	Drain-source on-state resistance	V_{GS}=10V,I_D=100mA	-	1.3	5	Ω
C_{iss}	Input capacitance	V_{DS}=25V， V_{GS}=0V f =1MHz	-	-	50	pF
C_{oss}	Output capacitance		-	-	25	pF
C_{rss}	Reverse transfer capacitance		-	-	5	pF
t_{on}	Turn-On time	V_{DD}=30V, I_D=200mA V_{GS}=0-10V	-	-	30	ns
t_{off}	Turn-Off time		-	-	30	ns

PATTERN DRAWING