DCR680N85

Phase Control Thyristor

Preliminary Information

DS5935-1.0 September 2008 (LN 26350)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- Medium Voltage Soft Starts
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR680N85* DCR680N80 DCR680N75 DCR680N70	8500 8000 7500 7000	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 200mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.
8200V @ -40^0 C, 8500V @ 0^0 C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

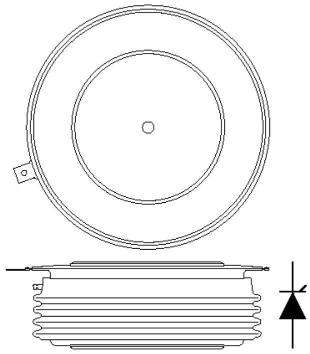
DCR680N85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	**8500V**
$I_{T(AV)}$	**677A**
I_{TSM}	**9800A**
dV/dt*	**1500V/µs**
dI/dt	**200A/µs**

*** Higher dV/dt selections available**



Outline type code: N

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	677	A
$I_{T(RMS)}$	RMS value	-	1063	A
I_T	Continuous (direct) on-state current	-	1013	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	9.8	kA
I^2t	I^2t for fusing	$V_R = 0$	0.48	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0221	°C/W
		Single side cooled	Anode DC	-	0.041	°C/W
			Cathode DC	-	0.0516	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 23 kN	Double side	-	0.004	°C/W
		(with mounting compound)	Single side	-	0.008	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			20.0	25.0	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	100	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	200	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	100A to 500A at T_{case} = 125°C		-	1.03	V
	Threshold voltage – High level	500A to 2500A at T_{case} = 125°C		-	1.3	V
r_T	On-state slope resistance – Low level	100A to 500A at T_{case} = 125°C		-	2.06	mΩ
	On-state slope resistance – High level	500A to 2500A at T_{case} = 125°C		-	1.542	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω, t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	T_j = 125°C, I_{peak} = 1000A, t_p = 1000us, V_{RM} = 100V, dI/dt = -5A/µs, dV_{DR}/dt = 20V/µs linear to 2500V		-	1200	µs
I_{RR}	Reverse recovery current	I_T = 1000A, t_p = 1000us, T_j = 125°C, dI/dt = - 5A/µs, V_R = 100V		95	118	A
Q_S	Stored charge			3000	4000	µC
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	250	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	15	mA

CURVES

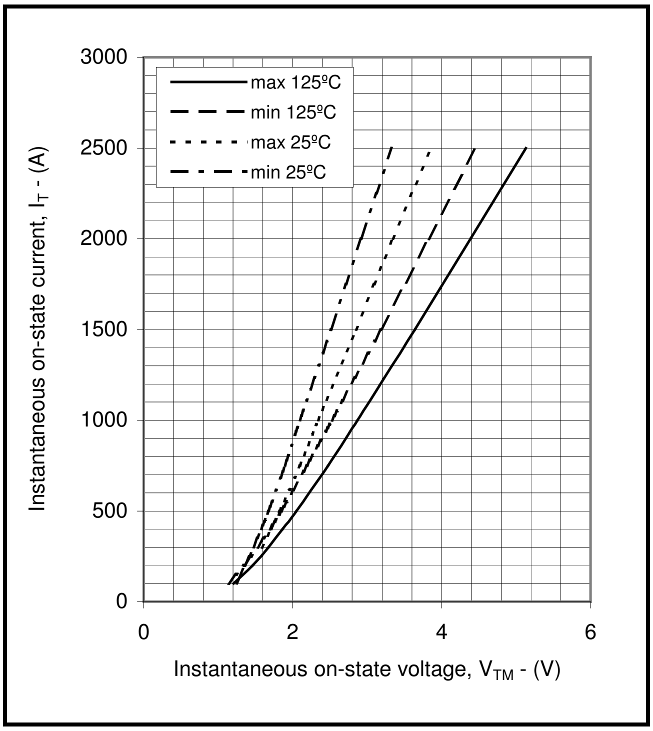


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.454245
B = 0.106933
C = 0.001271
D = 0.013218

these values are valid for T_j = 125°C for I_T 100A to 3000A

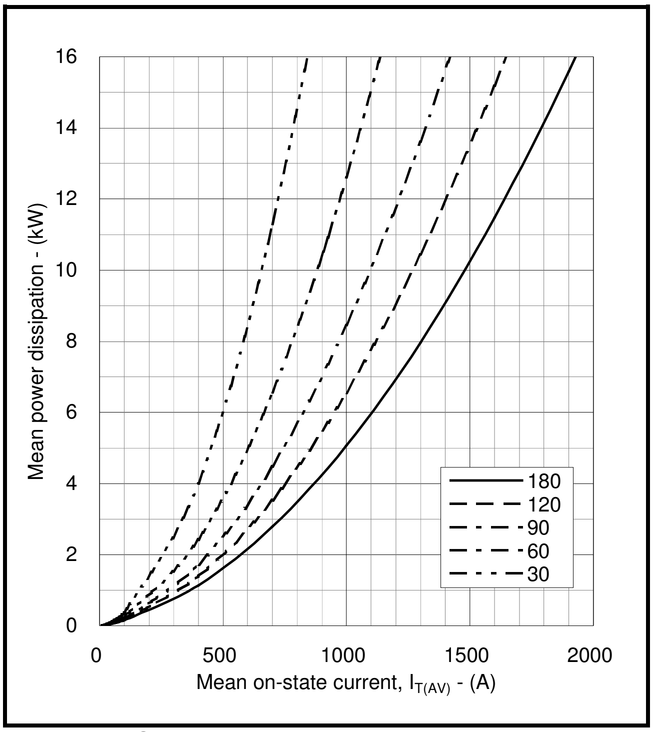


Fig.3 On-state power dissipation – sine wave

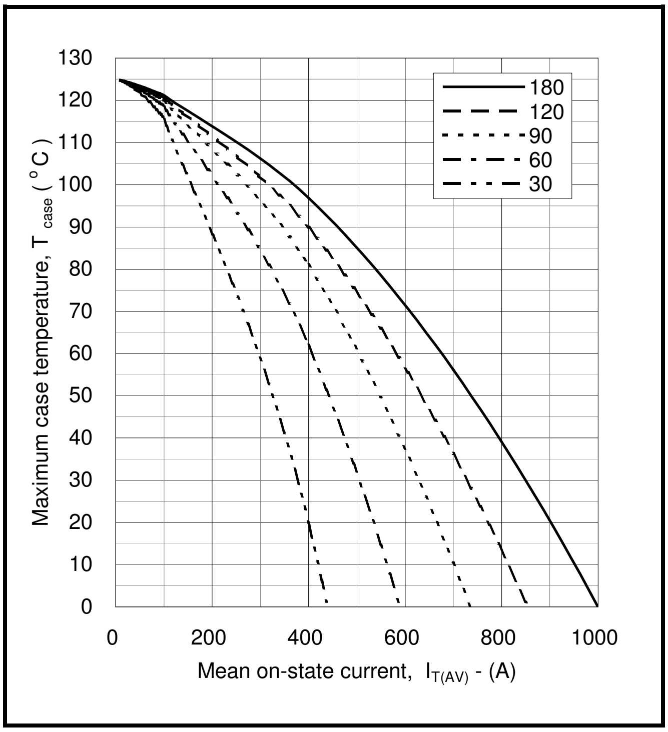


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

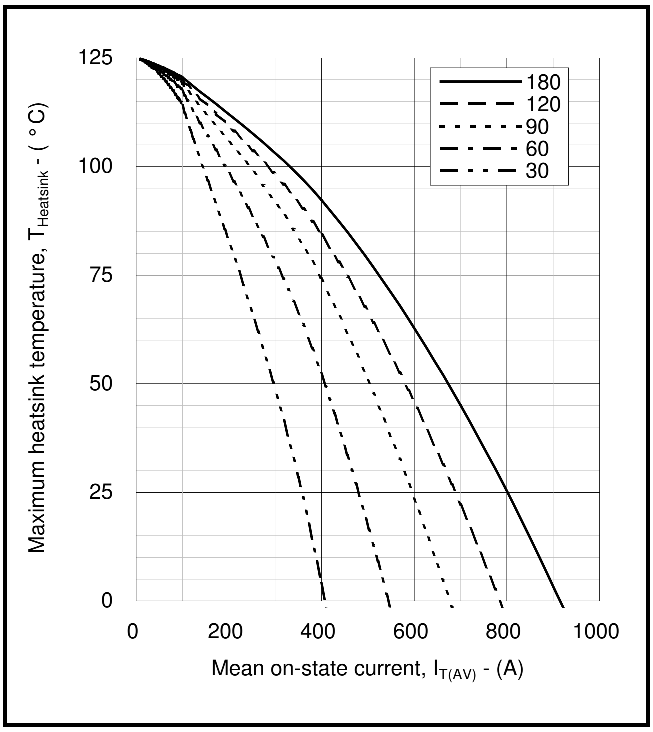


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

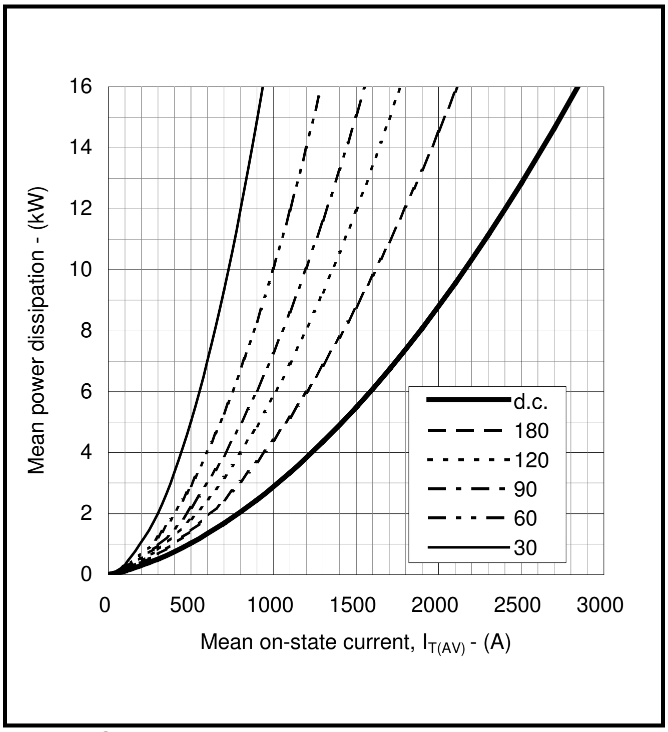


Fig.6 On-state power dissipation – rectangular wave

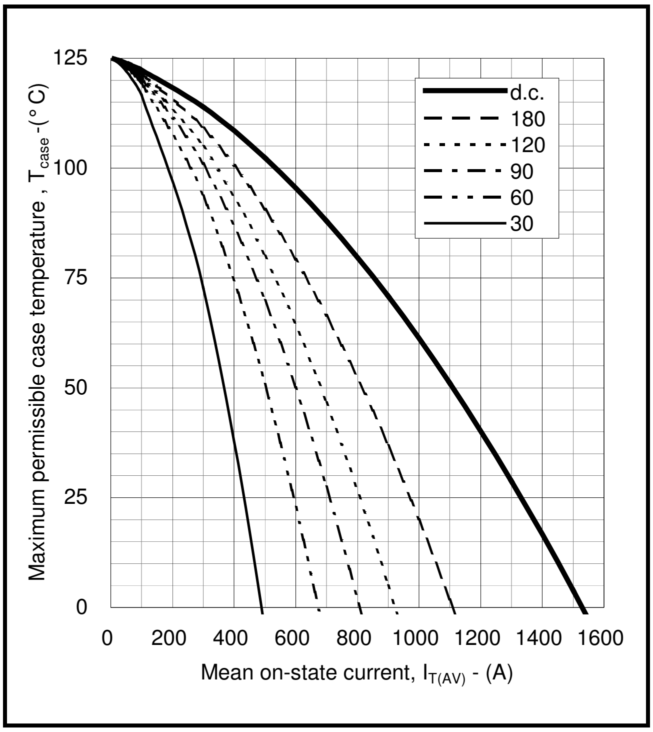


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

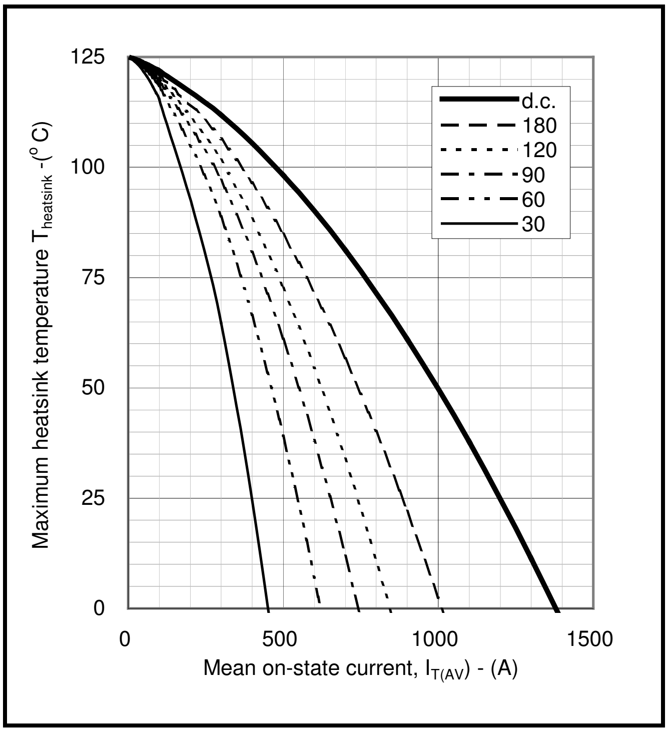
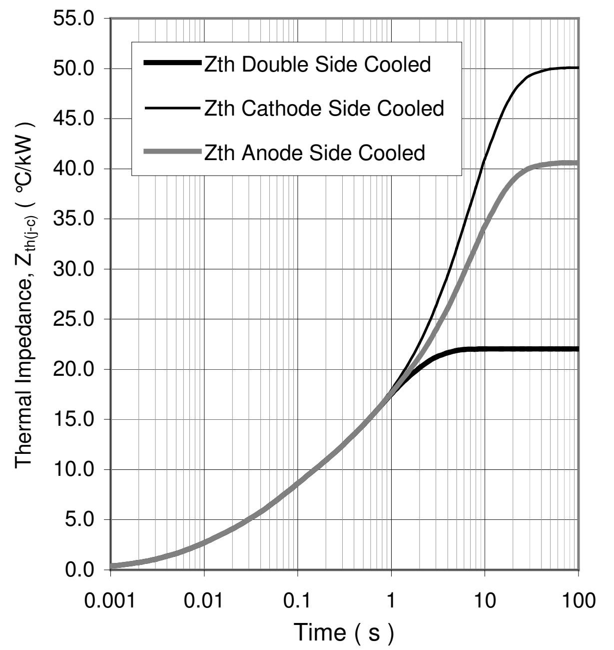


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (°C/kW)	3.4733	4.9047	9.1463	4.5220
	T_i (s)	0.1457	0.0166	1.2832	0.3767
Anode side cooled	R_i (°C/kW)	7.6674	5.0530	9.7355	27.5992
	T_i (s)	0.2241	0.0169	4.0566	8.2780
Cathode side cooled	R_i (°C/kW)	6.0393	4.2782	5.1301	25.0874
	T_i (s)	0.1356	0.0143	0.6594	7.2358

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T / T_i)]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	3.03	2.07
120	3.49	2.95
90	3.99	3.43
60	4.43	3.94
30	4.77	4.49
15	4.92	4.77

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	3.03	2.07
120	3.49	2.95
90	3.99	3.43
60	4.43	3.94
30	4.76	4.48
15	4.92	4.77

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	3.12	2.12
120	3.61	3.04
90	4.13	3.54
60	4.60	4.08
30	4.96	4.66
15	5.13	4.97

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

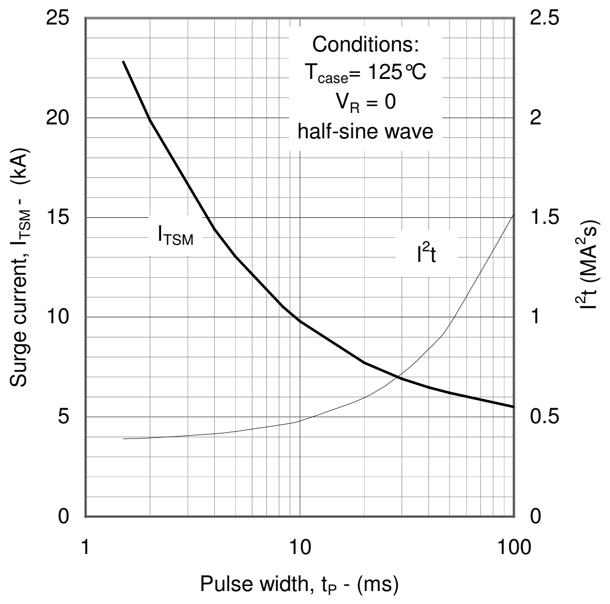


Fig.10 Single-cycle surge current

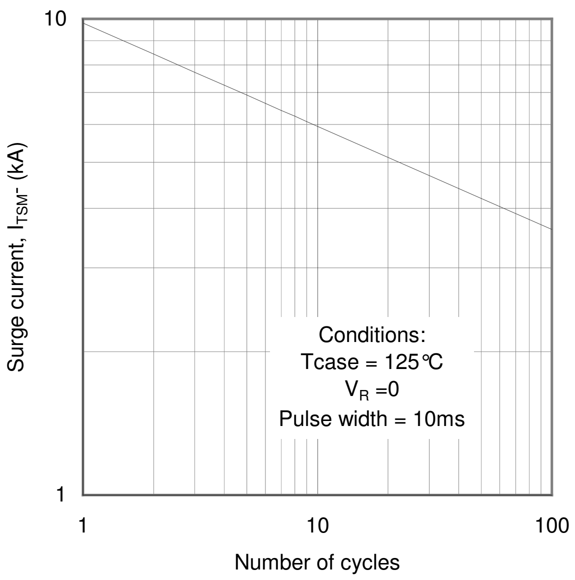


Fig.11 Multi-cycle surge current

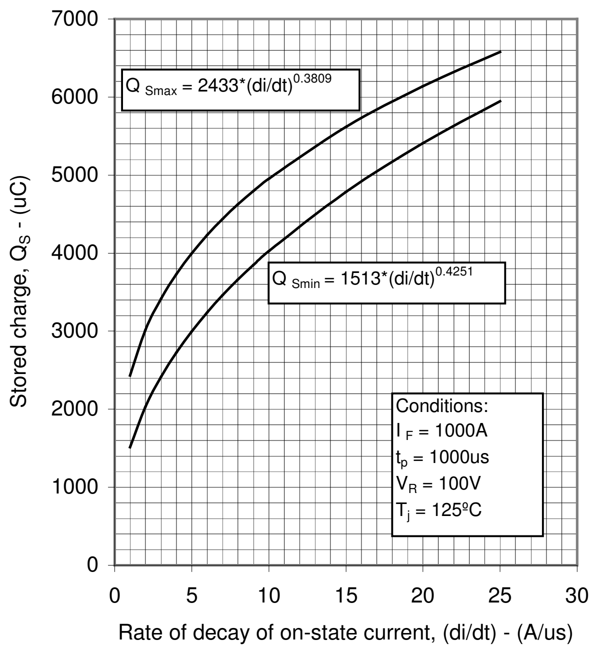


Fig.12 Stored charge

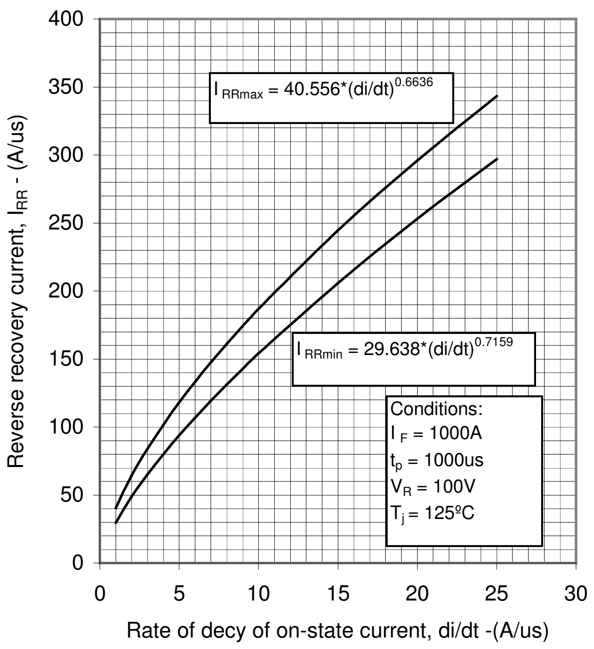
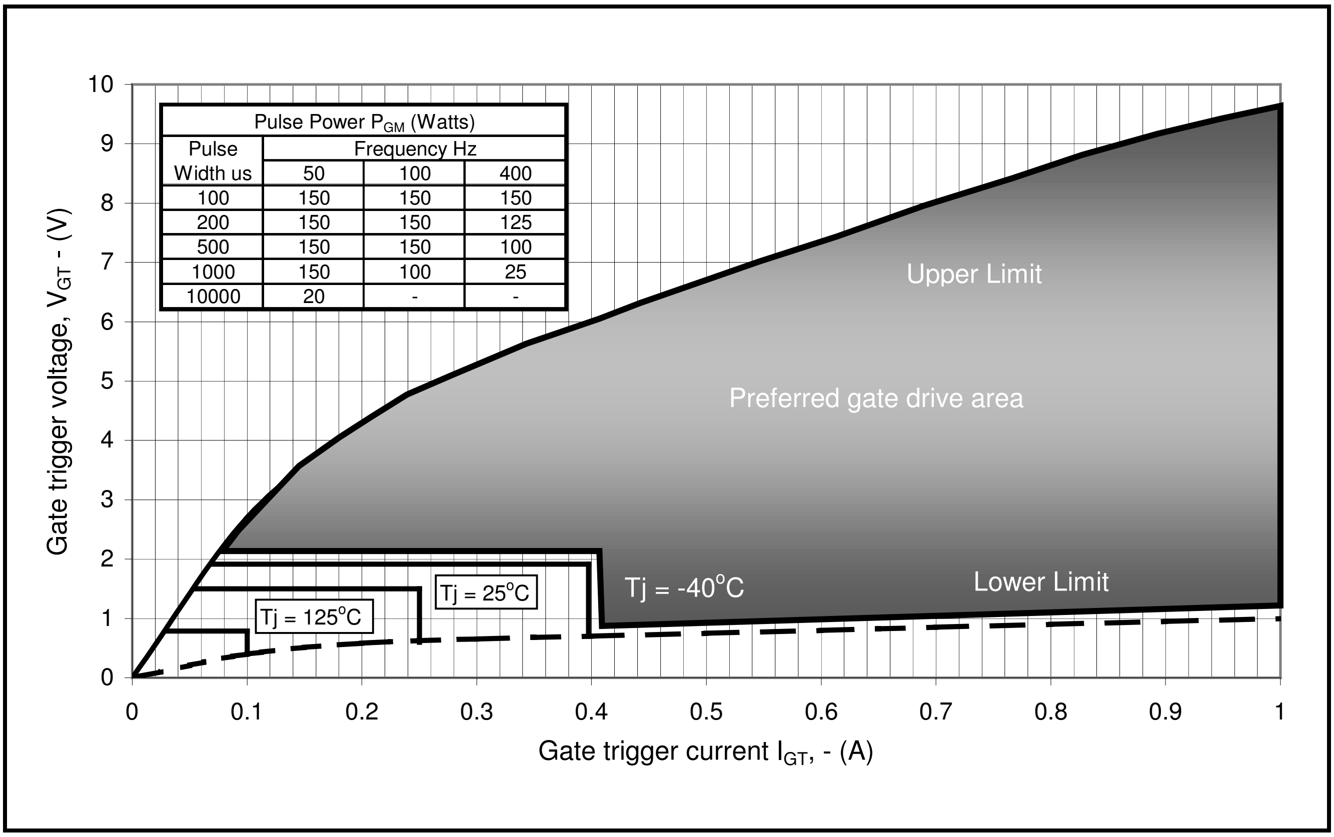


Fig.13 Reverse recovery current



Pulse Power P_{GM} (Watts)			
Pulse Width us	Frequency Hz		
	50	100	400
100	150	150	150
200	150	150	125
500	150	150	100
1000	150	100	25
10000	20	-	-

Fig14 Gate Characteristics

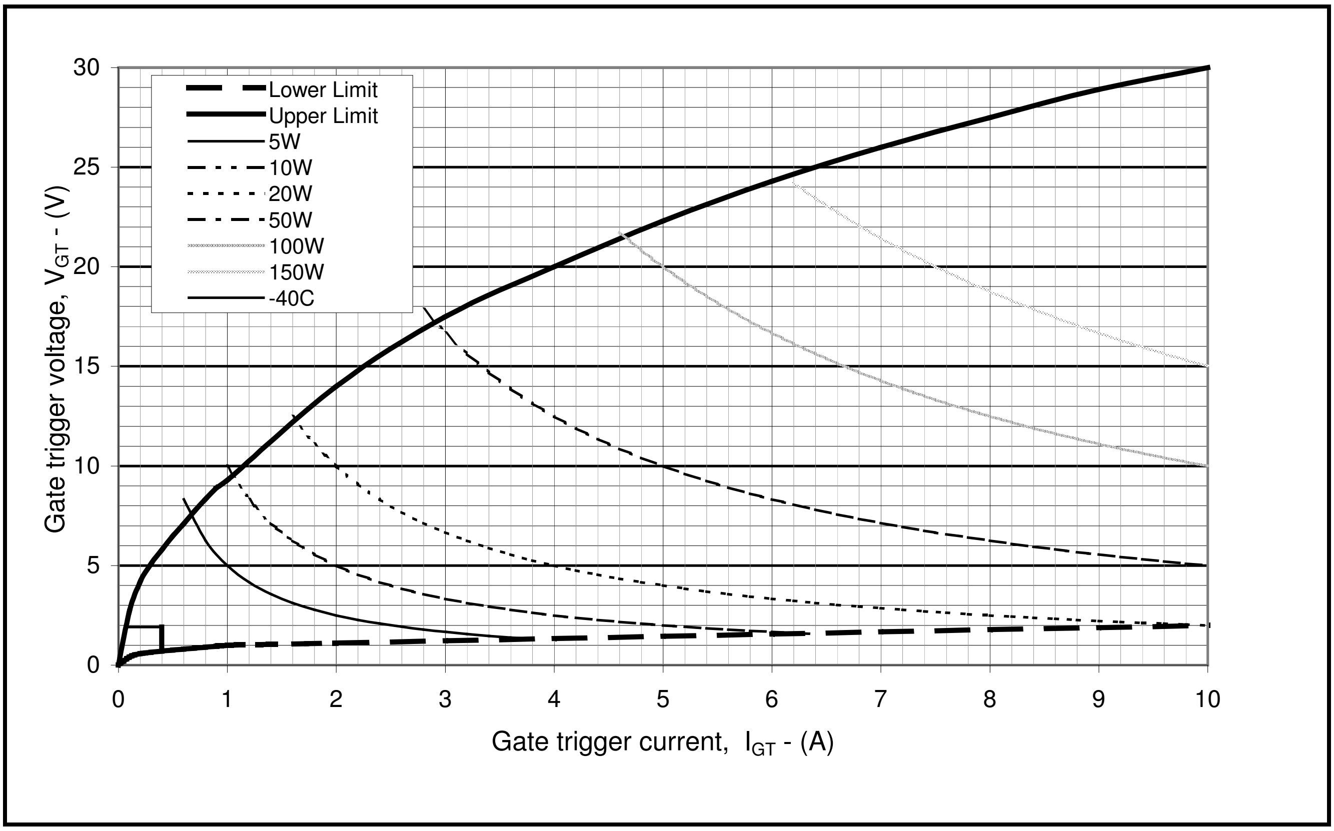


Fig. 15 Gate characteristics

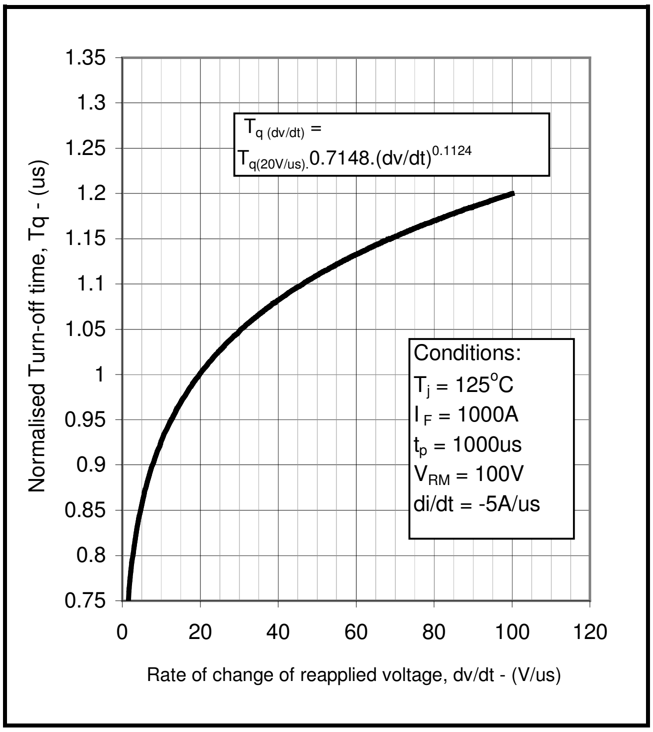
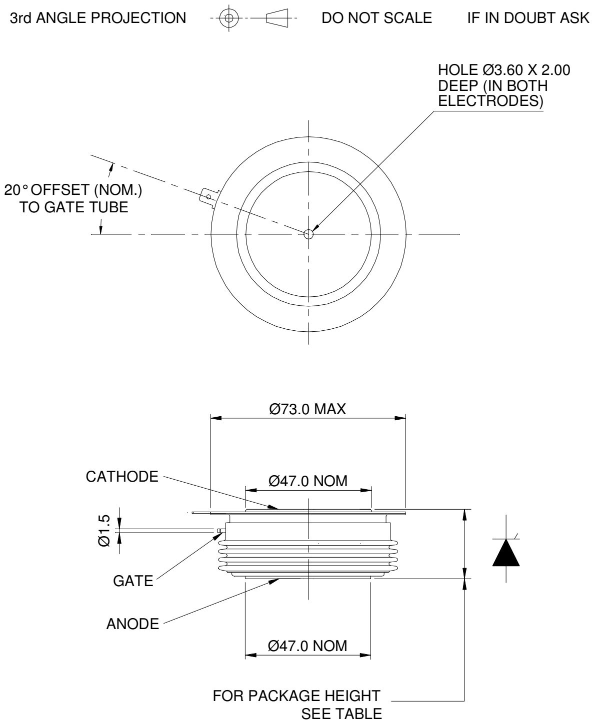


Fig.16 Turn-off time

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR1110N52	34.89	34.34
DCR1260N42	34.77	34.22
DCR1470N28	34.54	33.99
DCR1530N28	34.54	33.99
DCR1710N22	34.465	33.915
DCR680N85	**35.51**	**34.96**
DCR760N85	35.51	34.96
DCR820N65	35.15	34.6
DCR890N65	35.15	34.6

Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: N

Fig.17 Package outline

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

http://www.dynexsemi.com

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